**Motivation**

The ATLAS Tile Calorimeter will undergo a complete redesign and replacement of both its on- and off-detector electronics for the high luminosity LHC (HL-LHC). Advances in FPGAs, ASICs, component radiation hardness and data throughput will greatly benefit this upgrade. New levels of reliability and redundancy have been introduced to improve durability and to reduce maintenance. A Hybrid demonstrator will be used to test the new architecture while providing compatibility with current legacy systems.

**ATLAS Tile Calorimeter**

- Central hadronic calorimeter of the ATLAS experiment
- Composed of 4 barrel sections, each containing 64 azimuthal slices
- Slices contain alternating layers of steel plates and scintillating tiles
- A total of 5000 cells are each readout by two PMTs using WLS fibres
- Provides precise measurements of hadrons, jets, taus and missing transverse energy

### Old Architecture

#### Level 1 Trigger Signals:
- Pipeline Memory: Readout Modularity: HV Modularity:
- 1 + 1 (redundant) links, 48 PMTs
- 1 Unit, 48 PMTs
- 2 Units, 48 PMTs

#### Limited Analog Information
- On Detector
- 24-channel 12-bit 40 Mb/s ADCs
- Low Voltage control
- Control of CIS and Cesium calibrations

#### New Architecture

#### Fully Digitized Signal
- Off Detector
- 16 + 16 links, 6 PMTs
- 4 + 4 Units, 12 PMTs
- 4 + 4 Units, 12 PMTs

### TileCal Demonstrator Design

#### Front End Boards (FEB)
- Processes PMT signals
- Slow integration for Cesium calibration
- Charge Injection Calibration (CIS)

#### Mainboard & DaughterBoard
- Interface between 12 3-IN-1 boards and Daughterboard
- 24-channel 12-bit 40 Mb/s ADCs
- Low Voltage control
- Control of CIS and Cesium calibrations

#### Daughterboard:
- Minidrawer Control and Configuration
- Data serialisation and transfer, 8 data links (10.24 Gbs/each)
- On-board clock synchronisation through GBTx
- Dual QSF+/links to PPr (redundancy)

### Status of the Hybrid Demonstrator

#### Hybrid Demonstrator
- is fully compatible with current ATLAS hardware and is essential for the validation of the new read-out architecture.
- During the next LHC shut down it will be installed into a slice of the TileCal. The hardware is currently undergoing extensive testing and calibration before it will be ready for installation.

#### Radiation tests
- Majority of components passed for Run II luminosities
- Multiple levels of redundancy within FPGAs

#### Phase II Interface
- Increased control of configuration, calibration, and readout – to a single PMT
- New mobile testbench, Prometheus, under development
- Prometheus Web Interface eases control and recording of data

#### DCS
- Legacy control of HV + LVPS
- Legacy monitoring of voltages, currents, and temperatures
- Power consumption less than expected
- Temperatures satisfactory

#### Calibration Infrastructure
- Legacy software used for Charge Injection, Laser, and Cesium Calibrations
- Legacy mobile testbench, Mobidick, successfully interfaced for use in the detector

### Summary and Conclusion:

The Tile Calorimeter Phase II upgrade is far into its development and a demonstrator module has been produced. Component and design revisions are ongoing in order to improve performance. Control and calibrations tests have proved successful in the demonstrator, all legacy systems have been interfaced. The test beam was during two weeks in October 2015. We will have two more test beam campaigns in summer and fall 2016.