Upgrade of Tile Calorimeter of the ATLAS detector for the High Luminosity LHC.


Eduardo Valdes Santurio (on behalf of the ATLAS Tile Calorimeter System...)

Phone: +46 855378699
EMail: eduardo.valdes@fysik.su.se, eduardo.valdes@cern.ch
Upgrade of Tile Calorimeter of the ATLAS detector for the High Luminosity LHC.

Introduction…
Upgrade of Tile Calorimeter of the ATLAS detector for the High Luminosity LHC.

From present to phase II...

Timeline: $\frac{3}{21}$

**Introduction...**

**Upgrade...**

LVPS + HV OPTO...

1'3 in 1 + MB...

FATALIC...

QIE...

Daughterboard...

Tile Preprocessor...

Radiation Tolerance...

Conclusions...

**Present**

**Phase II**

**Legend:**
- ROD: Read Out Driver
- TTC: Trigger Timing and Control
- LVPS: Low Voltage Power Supply
- DCS: Detector Control System
- L1Calo: Level 1 Calorimeter trigger
- sLX: super Level X calorimeter trigger
- HV: High Voltage
- CAN: Controlled Area Network
- $\sum$: Summation Cards
- FELIX: Front-End Link eXchange

**Total data rate**

**Present**
- Number of links: 256
- Data rate per link: 640 Mb/s
- Links per super-drawer: 1 (+1)
- Data rate per super-drawer: 640 Mb/s

**Phase II**
- Number of links: 8192
- Data rate per link: 10 Gb/s
- Links per super-drawer: 4x4 (+4x4)
- Data rate per super-drawer: 160 Gb/s

**Tiles:**
- Tile Preprocessor
- ROD: Read Out Driver
- TTC: Trigger Timing and Control
- LVPS: Low Voltage Power Supply
- DCS: Detector Control System
- L1Calo: Level 1 Calorimeter trigger
- sLX: super Level X calorimeter trigger
- HV: High Voltage
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- FELIX: Front-End Link eXchange
Upgrade of Tile Calorimeter of the ATLAS detector for the High Luminosity LHC.

From present to phase II...

- Complete replacement of on-detector and off-detector electronics
- New readout strategy to provide digital trigger information at low latency for L0/L1
- Pipelines, derandomizers, DCS&TTC interface moved off-detector
- Improve reliability: reducing interconnections and stack of boards, implementing redundancy
- Minimize impact of failures with smaller DAQ elements: 1 super drawer is split in 4 independent mini-drawers with full redundant data path and powering.

<table>
<thead>
<tr>
<th>Up link only</th>
<th>Present</th>
<th>Upgrade</th>
</tr>
</thead>
<tbody>
<tr>
<td>Total BW</td>
<td>~ 165 Gbps</td>
<td>~80 Tbps</td>
</tr>
<tr>
<td>Nb fibers</td>
<td>256</td>
<td>8192</td>
</tr>
<tr>
<td>Fiber BW</td>
<td>640 Mbp</td>
<td>10 Gbps</td>
</tr>
<tr>
<td>Nb RODs</td>
<td>32</td>
<td>32?</td>
</tr>
<tr>
<td>ROD Crates</td>
<td>4</td>
<td>4</td>
</tr>
<tr>
<td>In BW/ROD</td>
<td>5 Gbps</td>
<td>2 Tbps</td>
</tr>
<tr>
<td>Out BW/ROD DAQ</td>
<td>2.56 Gbps</td>
<td>~ 20 Gbps</td>
</tr>
<tr>
<td>Out BW/ROD</td>
<td>Analog FE</td>
<td>&lt; 80 Gbps</td>
</tr>
</tbody>
</table>

Timeline (4/21)

Introduction...
Upgrade...
LVPS + HV OPTO...
'3 in 1 + MB...
FATALIC...
QIE...
Daughterboard...
Tile Preprocessor...
Radiation Tolerance...
Conclusions...

<table>
<thead>
<tr>
<th>ROD: Read Out Driver</th>
</tr>
</thead>
<tbody>
<tr>
<td>TTC: Trigger Timing and Control</td>
</tr>
<tr>
<td>LVPS: Low Voltage Power Supply</td>
</tr>
<tr>
<td>DCS: Detector Control System</td>
</tr>
<tr>
<td>L1Calo: Level 1 Calorimeter trigger</td>
</tr>
<tr>
<td>L1A: Level 1 Acceptance (from the ATLAS level 1 Central Trigger).</td>
</tr>
<tr>
<td>sLX: super Level X calorimeter trigger</td>
</tr>
<tr>
<td>HV: High Voltage</td>
</tr>
<tr>
<td>CAN: Controlled Area Network.</td>
</tr>
<tr>
<td>∑: Summation Cards</td>
</tr>
<tr>
<td>FELIX: Front-End Link exchange</td>
</tr>
</tbody>
</table>
Upgrade of Tile Calorimeter of the ATLAS detector for the High Luminosity LHC.

Hybrid drawer for the insertion in the current ATLAS detector...

- Compatibility of on detector and off-detector electronics with the current system (Hybrid drawer).
- Possibility of insertion in ATLAS for testing the performance of the upgrade system without compromising the present data taking.
Upgrade of Tile Calorimeter of the ATLAS detector for the High Luminosity LHC.

Demonstrator…

- New LVPS

- 2 different HVPS are proposed

- 3 different front end solutions are proposed
  - Modified 3 in 1 cards + mainboard
  - QIE + mainboard
  - FATALIC + mainboard

- A common control “daughterboard” compatible with the 3 front end solutions.

- One off detector tile preprocessor that will communicate with the on detector electronics and make the system compatible with the current tilecal electronics.
Low Voltage Power Supply and HV OPTO briefly…

- New LVPS and HVPS with double redundant design.
- Two High Voltage solutions are proposed with local or remote source.
3 in 1 Front end cards + Mainboard...

- Current design with modern components and improved performance
- Better linearity.
- Successful radiation tests.
- Shape the PMT signal to a stable pulse with 27 ns width.
- Bi-gain system with gain ratio 32.
- 17 bit dynamic range.
- Injects calibration pulses
- 5-gain selectable amplifier for the slow current integrator
3 in 1 Front end cards + Mainboard…

- interfaces the front end cards to the Daughter Board.
- two independent symmetric parts.
- each part reading out all cells.
- Supply low voltage levels to frontend cards and Daughter Board.
- Digitize fast and slow signals, and send parallel streams to the Daughter Board.
- Set gains on 3-in-1 frontend cards.
- Control DAC for charge injection calibration.
Upgrade of Tile Calorimeter of the ATLAS detector for the High Luminosity LHC.

3 in 1 Front end cards + Mainboard... Better performance than current electronics...

Timeline (10/21)

Introduction...
Upgrade...
LVPS + HV OPTO...
3 in 1 + MB...
FATALIC...
QIE...
Daughterboard...
Tile Preprocessor...
Radiation Tolerance...
Conclusions...
Front-end ATLAS tile Integrated Circuit (FATALIC)

- Potentially low noise chip.
- Most functionality in ASIC.
- 3 signal paths for analog processing.
- 3 embedded 12-bits ADCs
- Auto Gain Selection (Medium + (High or Low))
- 2 x12 bits data output (2 gains)
Upgrade of Tile Calorimeter of the ATLAS detector for the High Luminosity LHC.

Calibration tests... Pulse Analysis...

Timeline (12/21)

Introduction...
Upgrade...
LVPS + HV OPTO...
3 in 1 + MB...
FATALIC...
QIE...
Daughterboard...
Tile Preprocessor...
Radiation Tolerance...
Conclusions...
QIE Front End Board

- “Current Splitter” with gated integrator
- 4-range Charge Integrator
- 17 bits of dynamic range
- 5 bits Internal TDC -> 1 ns resolution
- (4) 16-bit DACs for calibration
- No Pulse Shaping
- Dead-timeless Digitization at 40 MHz
- Pipelined operation
- Radiation tolerant (SiGe for TID; SEU-tolerant design)
Tests and calibration...
Upgrade of Tile Calorimeter of the ATLAS detector for the High Luminosity LHC.

Daughterboard (r4)...

- Control and communication of the front end with back end.
  - Mainboards
  - HV Opto
  - Cesium Calibration System

- Common front end and read out interface for all the alternatives.
- System Clock recovery and distribution to the front end.
- Daughterboard current and temperature monitoring.
- High Speed communication: uplink (4x 9.6Gbps) and downlink (4x 4.8Gbps) with back end via one of the two QSFP (including additional 2 fold redundancy).

Timeline (15/21)

- Introduction...
- Upgrade...
- LVPS + HV OPTO...
- '3 in 1 + MB...
- 2FATALIC...
- QIE...
- Daughterboard...
- Tile Preprocessor...
- Radiation Tolerance...
- Conclusions...

FPGA: Field Programmable Array
TTC: Trigger Timing and Control
QSFP: Quad Small Form-factor Pluggable
HV: High Voltage
GBTx: radiation tolerant chip with 3.2-4.48 Gbps communication via bidirectional optic links for High Energy Physics.

Eduardo Valdes S... PhD
Tile Preprocessor Prototype (Off Detector)...

- Readout data coming from the detector
  - 4 Mini-Drawers
  - Up to 48 PMTs
- TTC distribution to the front-end electronics
  - Clock distribution for sync
- Communication with the Detector Control System (DCS)
  - Front-end electronics monitoring and configuration commands
- Keeps backward compatibility with the present DAQ system
  - G-Link to Legacy System
  - TTC decoding and clock recovery
- Real time data processing
  - Reconstruction algorithms: energy, time and quality factor
- Communication with the L0/L1 trigger system
  - Sending preprocessed data for L0/L1 trigger decision
Upgrade of Tile Calorimeter of the ATLAS detector for the High Luminosity LHC.

Tile Preprocessor Prototype (Off Detector)...

- **Jitter cleaners**
  - TI CDC62005
  - Low jitter (< 1 ps)
  - Clean recovery clocks for GTX
  - Unify clock domains

- **Xilinx Spartan 6**
  - Slow control
  - Clock management
  - Read module status
  - Read temp. sensors

- **Xilinx Kintex 7 FPGA**
  - XC7K420T
  - 28 GTX transceiver @ 10 Gbps

- **MiniPOD TX**
  - 12 x 10 Gbps
  - L0/L1 trigger comm.

- **SFP module**
  - TTC reception
  - Communication with current DAQ system
  - 4 x QSFP modules
    - FE communication
    - Each module at 40 Gbps
    - Total max. BW: 160 Gbps

- **ADN2814**
  - Clock/data recovery from TTC

**Timeline (17/21)**

- Introduction...
- Upgrade...
- LVPS + HV OPTO...
- '3 in 1 + MB...
- 2FATALIC...
- 3QIE...
- Daughterboard...
- Tile Preprocessor...
- Radiation Tolerance...
- Conclusions...

**Abbreviations**

- **FPGA**: Field Programmable Array
- **TTC**: Trigger Timing and Control
- **LX**: Level X trigger
- **QSFP**: Quad Small Form-factor Pluggable
- **SFP**: Small Form-factor Pluggable
- **PMT**: Photomultiplier Tube
- **FMC**: FPGA Mezzanine Card
- **GTX**: Gb Transceivers
Latest configuration in action…Reliability…

- 48 Hours continuous test including CRC checking and communication stability with no effective errors.
Upgrade of Tile Calorimeter of the ATLAS detector for the High Luminosity LHC.

Linearity tests...

Timeline (19/21)

Introduction...
Upgrade...
LVPS + HV OPTO...
13 in 1 + MB...
FATALIC...
QIE...
Daughterboard...
Tile Preprocessor...
Radiation Tolerance...
Conclusions...

Channel 0
Channel 1
Channel 2
Channel 3
Channel 4
Channel 5
Channel 7
Channel 8
Channel 9
Channel 10
Channel 11
Channel 12
Some words about Radiation Tolerance…

- Perform radiation tests to the system parts.
- Double Redundancy in the electronic design.
- Use of Radiation Tolerant components.
- Use of triple redundancy mode (TMR) in the FPGAs.
- Link Redundancy.
- Upstream Data Protection: CRC.
- Downstream Data Protection: GBT with FEC.

<table>
<thead>
<tr>
<th>Component</th>
<th>TID</th>
<th>NIEL</th>
<th>SEE</th>
<th>Status</th>
</tr>
</thead>
<tbody>
<tr>
<td>COTS regulators</td>
<td>Done - OK</td>
<td>Not done</td>
<td>Not done</td>
<td>Need different -5V</td>
</tr>
<tr>
<td>3-in-1</td>
<td>Preliminary</td>
<td>Pending</td>
<td>Preliminary</td>
<td>More testing needed</td>
</tr>
<tr>
<td>Main board</td>
<td>Not done</td>
<td>Pending</td>
<td>Not done</td>
<td>Size limitations</td>
</tr>
<tr>
<td>Daughter board</td>
<td>Not done</td>
<td>Pending</td>
<td>Done - OK</td>
<td>More testing needed</td>
</tr>
<tr>
<td>Modulator</td>
<td>Done - OK</td>
<td>Pending</td>
<td>Done - OK</td>
<td>Good to go</td>
</tr>
<tr>
<td>HV_Opto</td>
<td>Done - OK</td>
<td>Done - OK</td>
<td>Done - OK</td>
<td>Good to go</td>
</tr>
<tr>
<td>LVPS</td>
<td>Done (v7.5)</td>
<td>Done (v7.5)</td>
<td>Done (v7.5)</td>
<td>Needs full testing</td>
</tr>
<tr>
<td>Adders</td>
<td>Not needed</td>
<td>Not needed</td>
<td>Not needed</td>
<td>Testing not needed</td>
</tr>
<tr>
<td>Active bases</td>
<td>Done</td>
<td>Done</td>
<td>Not needed</td>
<td>Good to go</td>
</tr>
<tr>
<td>FATALIC</td>
<td>Not done</td>
<td>Not done</td>
<td>Not done</td>
<td>Not started</td>
</tr>
<tr>
<td>QIE</td>
<td>Not done</td>
<td>Not done</td>
<td>Not done</td>
<td>Not started</td>
</tr>
<tr>
<td>Scintillators</td>
<td>Preliminary</td>
<td>Not done</td>
<td>Not done</td>
<td>More tests needed</td>
</tr>
</tbody>
</table>

**Timeline (20/21)**

- Introduction...
- Upgrade...
- LVPS + HV OPTO...
- '3 in 1 + MB...
- FATALIC...
- QIE...
- Daughterboard...
- Tile Preprocessor...
- Radiation Tolerance...
- Conclusions...

**Terminology**

- **TID**: Total Ionizing Dose
- **SEE**: Single Event Effects
- **NIEL**: Non ionizing energy loss
- **TMR**: Triple Mode redundancy
- **CRC**: Cyclic Redundancy Check
- **GBT**: GigaBit Transceiver data transmission protocol
- **FEC**: Forward Error Correction
- **LVPS**: Low Voltage Power Supply
Conclusions and Questions...

— Better reliability have been achieved with the current version of the demonstrator comparing it to the previous prototypes.

— Validation of front ends alternatives will take place soon in the coming test beams.

— Radiation tests are needed to validate the radiation tolerance of the different parts of the Demonstrator

— A hybrid demonstrator drawer will be ready soon!