ATLAS ITk Strip Tracker R&D

Ingrid-Maria Gregor, DESY
on behalf of the ATLAS Collaboration

3rd ECFA High Luminosity LHC Experiments Workshop
Aix-les-Bains, France
3rd-6th October 2016
ATLAS ITk Strips

Central barrel segment:
- 4 barrel layers
- $R = 405 - 1000\text{mm}$ & $z = -1400 - 1400\text{mm}$
- short strips (24.1mm) in inner-layers
- long (48.2mm) strips outer-layer

Outer end-caps on each side
- 6 end cap disks on each side
- Covers $z = \pm 3\text{m}$ & up to $\eta = 2.5$
- Disks made of 6 rings
- Strip lengths and pitches vary to accommodate geometry and occupancy

- With TDR to be submitted at the end of year
- R&D about to be concluded
Challenges

Radiation levels (incl. safety factor 1.5):

<table>
<thead>
<tr>
<th></th>
<th>Fluence [1/cm²/collision]</th>
<th>Dose [kGy]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Long strips</td>
<td>4.2 E14</td>
<td>107</td>
</tr>
<tr>
<td>Short strips</td>
<td>8.1 E14</td>
<td>351</td>
</tr>
<tr>
<td>End-cap</td>
<td>1.2 E15</td>
<td>504</td>
</tr>
</tbody>
</table>

- Occupancy
  - Need to keep the occupancy below 1%

- Material budget
  - Need to reduce significantly compared to current inner tracker.

- Size
  - 160m² of modules is a new logistical problem for ATLAS
**Stave and Petal Concept**

- Provide mechanical support, cooling and readout of active modules with minimal material budget and good performance.
- Silicon modules directly bonded to a cooled carbon fibre plate.
- Sandwich construction for high structural rigidity with low mass.
- Services integrated into plate including power control and data transmission.
- Early integration.

- Extensive R&D on thermo-mechanical performance, producibility and handling.
- Optimisation of glue process.
- Semi-automatic module loading.
Module Concept

- Silicon strip sensor
- Hybrid
  - Kapton circuit board
  - FE-ASICs
  - Power board (DC-DC)
Sensor parameters defined: **n-in-p with p-stop isolation**
- Collects electrons like current n-in-n pixels -> Faster signal, reduced charge trapping
- Always depletes from the segmented side: good signal even under-depleted

**Extensive R&D programme:**
- Bulk damage
- Surface damage
- Effects on inter-strip capacitance etc.
- Behaviour of large sensors
  - ....
Planar Silicon R&D

Inter-strip resistance versus TID

Inter-strip resistance versus fluence

Non irradiated sample in magnetic field

- Nicely shown that performance at end of lifetime is still within specifications.
- Full size sensor also being studies.

Four papers published at Hiroshima 2016

Lorentz Angle Measurement on Non-irradiated Sensors

<table>
<thead>
<tr>
<th>Sensor 1</th>
<th>Incidence Angle (degrees)</th>
<th>Cluster Size</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>-20</td>
<td>1.8</td>
</tr>
<tr>
<td></td>
<td>-15</td>
<td>2</td>
</tr>
<tr>
<td></td>
<td>-10</td>
<td>2.2</td>
</tr>
<tr>
<td></td>
<td>-5</td>
<td>2.4</td>
</tr>
<tr>
<td></td>
<td>0</td>
<td>2.6</td>
</tr>
<tr>
<td></td>
<td>5</td>
<td>2.8</td>
</tr>
<tr>
<td></td>
<td>10</td>
<td>3</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Sensor 2</th>
<th>Incidence Angle (degrees)</th>
<th>Cluster Size</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>-20</td>
<td>1.8</td>
</tr>
<tr>
<td></td>
<td>-15</td>
<td>2</td>
</tr>
<tr>
<td></td>
<td>-10</td>
<td>2.2</td>
</tr>
<tr>
<td></td>
<td>-5</td>
<td>2.4</td>
</tr>
<tr>
<td></td>
<td>0</td>
<td>2.6</td>
</tr>
<tr>
<td></td>
<td>5</td>
<td>2.8</td>
</tr>
<tr>
<td></td>
<td>10</td>
<td>3</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Magnetic Field (T)</th>
<th>Lorentz Angle (LA)</th>
</tr>
</thead>
<tbody>
<tr>
<td>B = 1.00</td>
<td>LA = -3.30 +/- 0.06</td>
</tr>
<tr>
<td>B = 0.75</td>
<td>LA = -2.24 +/- 0.03</td>
</tr>
<tr>
<td>B = 0.50</td>
<td>LA = -1.70 +/- 0.05</td>
</tr>
<tr>
<td>B = 0.00</td>
<td>LA = -0.05 +/- 0.03</td>
</tr>
</tbody>
</table>
Common Sensor Market Survey

Market Survey has three phases:
- Step 1: Collection of responses ("Questionnaire"): 4 weeks
- Step 2: Collection of free samples from prior work: 4 weeks
- Step 3: Order and tests of samples to our specifications: 9 months

Market Survey common with CMS issued in April 2016

Step 1:
- Received responses from six vendors
- Evaluation of responses with interaction with companies throughout July
- Selection of companies to proceed with step 2 was taken and will be published by CERN

Step 2 and Step 3:
- Free samples and subsequently wafer orders based on our specs ongoing
- Organisation of test and irradiation campaign started
- Many institutes will repeat their studies with the new samples under the same conditions
HV/HR-CMOS Strips Developments

- Evaluation program for HV/HR-CMOS
- Possibility of several significant improvements:
  - Less material, better hit resolution in r-\(\phi\) and z
  - Very competitive cost
  - Faster construction: a lot fewer wire-bonds, faster fabrication
- Signal/noise ratio different from planar sensors: need to be carefully evaluated.
- Project evaluated with simple CHESS-1 chip.
- Results fed into design of reticle-sized CHESS-2 chip
  - Just came back from fabrication.
  - Features three large arrays, along with numerous test structures.
- Four different resistivities will be studied, from the nominal 20 \(\Omega\)-cm to \(~1\) k\(\Omega\)-cm to boost the signal level across the range of expected fluences.
**Module Concept**

- Silicon strip sensor
- Hybrid
  - Kapton circuit board
  - FE-ASICs
  - Power board (DC-DC)

---

The diagram illustrates the components of the module concept, including:

- **DC-DC converter**
- **Power board**
- **ABC130**
- **HCC**
- **Multiplexing ASIC**
- **Wire-bonds**
- **Glue**
- **Sensor**
- **Hybrid**
- **LV/HV power board**
- **ABC ASIC**
Custom Designed ASICs

ABC130

- **ABC130 - 130nm process**
  - ATLAS binary chip with 256 channels
  - Converts incoming charge signal into hit/no-hit information

HCC - 130 nm process

- Interface between ABC130 and bus-tape
- Collects information from O(10) ABC130 and sends to outside world

AMAC

- Chip for local monitoring

upFEAST

- Chip to control the parallel powering (DC-DC)
- First version (FEAST) worked fine but was not radiation hard
- upFEAST currently being designed (CERN)
Radiation Studies FE-chips

- Studies at various facilities with different dose types, rates and environmental conditions with FE-chip ABC130
- Increase in noise up to ~10 MRad
- Small O(1%) decrease in gain recovering at high doses
- Current peak induced by RINCE at 1MRad

Load on cooling/power at a cable/large object level have been calculated from radiation profiles and single component measurements.

Model being prepared to estimate impact on overall current dissipation

Designed system against changes - new front-end in hands

Improvements before and after irradiation

<table>
<thead>
<tr>
<th>Source</th>
<th>T (C)</th>
<th>Current Increase</th>
<th>Dose Rate (MRad/h)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Co-60 CERN</td>
<td>-25</td>
<td>2.5</td>
<td>0.0023</td>
</tr>
<tr>
<td>Co-60 CERN</td>
<td>-10</td>
<td>1.9</td>
<td>0.0023</td>
</tr>
<tr>
<td>Co-60 CERN</td>
<td>-10</td>
<td>1.3</td>
<td>0.0006</td>
</tr>
<tr>
<td>x-ray CERN</td>
<td>-15</td>
<td>3.9</td>
<td>0.062</td>
</tr>
<tr>
<td>x-ray CERN</td>
<td>-15</td>
<td>13.6</td>
<td>2.25</td>
</tr>
<tr>
<td>x-ray CERN</td>
<td>+20</td>
<td>5.2</td>
<td>2.25</td>
</tr>
<tr>
<td>Birmingham-p</td>
<td>-25</td>
<td>9.7</td>
<td>1.25</td>
</tr>
</tbody>
</table>
Radiation Studies FE-chips

- Studies at various facilities with different dose types, rates and environmental conditions with FE-chip ABC130
- Increase in noise up to ~10 MRad
- Small O(1%) decrease in gain recovering at high doses
- Current peak induced by RINCE at 1MRad

Load on cooling/power at a cable/large object level have been calculated from radiation profiles and single component measurements.
- Model being prepared to estimate impact on overall current dissipation
- Designed system against changes - new front-end in hands
- Improvements before and after irradiation
**Module Developments**

- A few hundred modules produced at 16 different sites.
- Exactly same module assembly process for all different module types.
- Modular tooling.

Recent R&D:
- Optimisation of glue process -> UV glue
- Noise behaviour

- here more ....
- Glue studies
- Stress simulations
- Other stuff

- Nice photos of modules
Test Beam Studies at DESY and CERN

Huge effort ongoing to complete studies for the TDR
- 130 nm barrel LS module tested at 11 positions
- 250 nm EC module studied
- 130 nm single chip card with irradiation sensor under test
- Full module with 130nm chips irradiated up to 7E14 n$_{eq}$ cm$^{-2}$ at PS

Results in preparation for the TDR

List of measurements ....
- Signal to noise
- Charge sharing
- Sensor biasing
- Efficiencies
Results

need to see what I can show at ECFA ….
Travelling Mini-Assembly

- 21 sites around the world involved in the assembly and/or testing of barrel and end-cap modules.
- Mini-assembly with small sensor and front-end chips travelling to check the reproducibility of electrical performance results.

I asked for plots with readable labels!!
LARGER SIZE STRUCTURES

- Modul
- bus tape
- Modul
**Data Transmission on Bus Tape**

- Bus tapes (up to 140cm) provide:
  - all the low and high voltage from the end of structure to the module
  - all the high speed data links

- Designed to have very high reliability and minimum material.
  - Bottom shield is necessary to avoid influence of carbon fiber facing

- 1MHz readout specification by TDAQ requires
  - 640 Mbps for data transmission point to point
  - 160 Mbps transmission of TTC data on multi-drop lines

- Point to point data transmission:
  - Tape bandwidth in excess of the required 640 Mbps. The transmission robustness can be further enhanced by using 8/10b encoding.

- TTC multidrop:
  - Even with reflections from 10 hybrid loads the transmission works well at 160 Mbps
  - No errors in all tests with x2 load values, or x2 speed, or both.

---

Eye diagram for PRBS-31 (equivalent to no data encoding) for 160 Mbps and double the capacitive loads

---

Table 9.22. Radiation Length estimates for the barrel stave and end-cap petal. Power ASICs and the EoS are not included. These numbers need to be confirmed with full stave and petal designs.

**Barrel End-Cap**

<table>
<thead>
<tr>
<th>Element</th>
<th>% Radiation Length</th>
</tr>
</thead>
<tbody>
<tr>
<td>Stave Core</td>
<td>0.48</td>
</tr>
<tr>
<td>Bus Cable</td>
<td>0.18</td>
</tr>
<tr>
<td>Short-Strip Modules</td>
<td>1.08</td>
</tr>
<tr>
<td>Module Adhesive</td>
<td>0.06</td>
</tr>
<tr>
<td>Total</td>
<td>1.80</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Element</th>
<th>% Radiation Length</th>
</tr>
</thead>
<tbody>
<tr>
<td>Petal Core</td>
<td>0.47</td>
</tr>
<tr>
<td>Bus cables</td>
<td>0.03</td>
</tr>
<tr>
<td>Modules</td>
<td>1.04</td>
</tr>
<tr>
<td>Module adhesive</td>
<td>0.06</td>
</tr>
<tr>
<td>Total</td>
<td>1.60</td>
</tr>
</tbody>
</table>

---

9.3.1 Bus-tape

The bus tapes provide all the low voltage and high voltage power from an End of Structure (EoS) card at the end of the stave or petal to the modules. The bus tape provides all the high speed data links to (from) the modules from (to) the EoS. The bus tape also provides I$_2$C communication between the EoS and the AMAC chip on the power board. The modules are glued directly onto the bus tapes.

**Tape Design**

Identical technologies will be used for the barrel stave and petal bus tapes and the differences between the two types of bus tapes will only be those dictated by the different geometry.

- Polyimide
- Glue
- Tracks
- AC Ground
- Tracks
- Polyimide
- Glue
- Shield

Figure 9.87. Sketch (not to scale) to illustrate the stackup of the bus tape, showing the three copper layers (green), three polyimide layers (yellow) and the glue sheets holding them together (blue).

The bus tapes are laminated from two layers of adhesiveless copper/polyimide, c.f. the stackup in Fig. 9.87. The tapes are designed to have very high reliability and minimum material. They therefore use adhesiveless copper/polyimide tapes and all connections to the modules and the EoS are made using standard aluminium wire bonding. The copper thickness used is 17 $\mu$m (1/2 Oz Copper) and the polyimide and glue layers are both 25 $\mu$m thick. Openings are cut out around pads to allow standard Ni/Au plating for the exposed pads (but not the full length of the tracks).

The separation between exposed HV pads and neighbouring pads is greater than 2.5 mm (0.8 mm if the tracks are underneath a cover layer) to respect the IPC specifications. As the same copper layer is used for high speed tracks and for power, the minimum thickness was selected in order to meet the voltage drop requirements without exceeding the available width. The voltage drop requirements for the low voltage return for the stave bus tapes is satisfied by the use of a 60 mm wide trace.
Local and Global Supports

- Progress on the global support design for the barrel and end-cap structures
- End-caps now settled on an approach based on blades as structural elements within a disk
- Tooling for EC assembly is moving ahead
- Insertion and locking mechanism defined
- FEA for frequency response shows design has appropriate stiffness
- Thermo-mechanical prototypes for staves and petals progressing
  - Comparison between FEA and measurements ongoing

Thermo-mechanical prototypes w. dummy modules
Studying the possible reuse of current ID cables is progressing well. Strips will likely reuse SCT Type IV and possibly Type III cables. Pixels will reuse existing Pixel cables at least up to PP2. Existing Pixel HV cables don’t meet the higher 1200V spec for the inner most layer. TRT HV cables may fill this gap. Both Strips and Pixels will require at least new cables from PP2 to PP1. Cable specs in preparation and updated cost estimates will be sought over the summer.

currently only on cables, need to do it more general
Towards Production

- R&D from the start focussed on producibility and ease of handling.
- TDR is in preparation and collaboration is getting ready for production and assembly.
  - Money matrix in preparation
  - Sites starting to gear up
  - Logistics being prepared

- Identified sites for production of various items.
- Optimisation of process ongoing.
Summary and Conclusions
Backup Slides
Hybrid Population in Industry

- First tests of mounting chips on hybrids in industry promising
- Chip tilt larger and may need to be controlled better
- First mechanical module built using these hybrids are underway
**TID Current Increase**

**Surface effects**: Generation of charge traps due to ionizing energy loss (Total ionising dose, TID) (*main problem for electronics*).

- The leakage current is the sum of different mechanisms involving:
  - the creation/trapping of charge (by radiation)
  - its passivation/de-trapping (by thermal excitation)
- These phenomena are dose rate and temperature dependent!

- Charge trapped in the STI oxide
  - +Q charge
  - Fast creation
  - Annealing already at $T_{amb}$

- Interface states at STI-Silicon interface
  - -Q for NMOS, +Q for PMOS
  - Slow creation
  - Annealing starts at 80-100C

STI = shallow trench interface