Module and Electronics Developments for the ATLAS ITk Pixel System

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Overview

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Motivation

Upgrade of the LHC to the High Luminosity LHC (HL-LHC) in ~2024.
   - Increased peak (x ~5-7) and integrated (x ~10) luminosity.

This will result in:
   - A greater number of interactions per bunch crossing (x 8).
   - Increased radiation damage (x ~20).
      • Especially close to the beam pipe.
ATLAS Pixel Detector Evolution

Original ATLAS Pixel Detector

IBL Upgrade
• Installed in May 2015
• Phase 0 upgrade

ITk Upgrade
• Phase 2 upgrade
• Complete replacement of the ATLAS Inner Detector
ITk Pixel Plans

• ITk Pixel Technical Design Review (TDR) to be completed late 2017.
• **Construction:** 2018-2023
• **Installation:** 2024-2025

• The 5 innermost layers of ITk will comprise a pixel detector built of new sensor and readout electronics technologies to improve the tracking performance and cope with the severe HL-LHC environment in terms of occupancy and radiation.
• The total area = up to 14 m²
  – depends on the final layout choice (early 2017).

See: No7-13, The Phase-II ATLAS Pixel Tracker Upgrade: Layout and Mechanics, A. Sharma
Front End Technology

• Under the framework of the RD53 Collaboration, a new front end chip has been designed in a joint ATLAS-CMS effort.

• The prototype FE65-P2 design has been manufactured and measured.
  – A version with an n-in-p sensor was also tested in a test beam.

• A full prototype, known as RD53A, is planned for 2017.

• After the RD53A prototype, an adapted ATLAS design will be produced (2018).


See: N39-8, A Prototype of a New Generation Pixel Readout ASIC in CMOS 65nm for Extreme Rate HEP Detectors at HL-LHC, S. Panati
Sensors – Hybrid

• Hybrid pixel sensors: Readout electronics and sensor are separately produced and connected afterwards.

• Planar and 3D sensors (technology used for the IBL).
  – Re-designed with cell sizes of 50x50 or 25x100 μm² (compatible with the RD53 chip).
    • Prototypes are ready for both designs.
  – Sensor thickness:
    • Outer-layers foreseen as ≤ 150-200 μm
      -> high yield and low costs are required.
    • Two inner-most layers ≤ 100-150 μm (planar)
      -> radiation hardness is the major concern.
    – For 3D the radiation hardness is decoupled from the thickness so it has a wider thickness range.

• Prototyping sensor productions
  – in collaboration with commercial vendors to identify the best technology for the different pixel layers.
Sensors – Hybrid

See: N26-8, Performance Study of N-in-P Active Edge Planar Pixel Sensors for ATLAS Inner Detector Upgrade, T. Rashid

See: N55-5, Optimization of Thin N-in-P Planar Pixel Modules for the ATLAS Upgrade at HL-LHC, A. Macchiolo

See: N55-3, New Thin 3D Pixel Sensors for HL-LHC: First Results, G.-F. Dalla Betta

See: N41-2, 3D Silicon and Passive CMOS Pixel Detectors for Radiation Hard Environments, D.-L. Pohl

See: N41-2, 3D Silicon and Passive CMOS Pixel Detectors for Radiation Hard Environments, D.-L. Pohl
Sensors – CMOS

- Monolithic HV or HR CMOS sensors are also being actively studied.
- A specific R&D program has been started with the aim of producing and testing large size (1-2 cm²) demonstrators by late-2016.
- Potentially offer a significant cost reduction with respect to traditional hybrid pixel detectors.
  - Could be particularly interesting for the outermost pixel layers.

Hybrid CMOS:
- CMOS sensor bonded (via bump-bonds or capacitive coupling) to FE-I4 readout chip.
- Used to study radiation hardness and rate-capability of CMOS design.
  - Radiation hard to $> 10^{15} \text{n}_{\text{eq}}/\text{cm}^2$

Chronopixel:
- 25µm x 25µm (currently)
- 280 µm thick
- Charge collection by diffusion.
- Digital signal of (x,y,t) read out.
- Prototype 3 is currently under study.

See: N26-7, Geiger-Mode Avalanche Pixels in a 180 Nm HV CMOS Process for a Dual-Layer Particle Detector, M. Musacci
See: N53-2, HVCMOS Pixel Detectors - First Measurements on the Reticle Size Prototype for the ATLAS Pixel Layers, F. Ehrler
See: N53-3, Characterization of Fully Depleted CMOS Active Sensors on High Resistive Substrate for High Radiation Environment, T. Hirono
Inter-connectivity

• Particularly challenging aspect of the ITK pixel module assembly.
  – Large area to be covered and a compressed production schedule.
• Multiple industrial suppliers are being qualified with FE-I4 multi-chip modules.
  – Silver tin and indium bump bonding are being investigated.
  – Re-iteration of procedure with the final ITk read-out chip.
    • Higher bump density (50x50 µm²)
    • Larger chip wafer size:
      – 12” for the 65 nm CMOS technology versus the 8” for 130 nm CMOS.
      – Dummy productions for higher density 12” wafers with producers such as IZM and LETI.
• An intense R&D is being carried out to satisfy the yield requirements when using 100-150 µm thin chips and towards cost reduction, exploring the feasibility of mask-less Under Bump Metalisation (UBM) or wafer-to-wafer inter-connection.
  – Chip thickness is a main issue due to the many layers which can be damaged through bending.
• Novel R&D of inter-connectivity with Through-Silicon Vias (TSV).
Powering Scheme

• The current pixel detector is powered in parallel.
  – This is not feasible for the ITk due to the number of modules.
• Baseline design for ITk is that modules will be powered in series.
  – Saves material in the servicing cables.
• Extensive tests are being carried out with FE-I4 modules thanks to dedicated shunt-regulators (Shunt-LDO) in the IBL chip.
  – Operated with a constant current.
• Special protection chip being developed.
  – Would allow switching on/off of individual modules.
  – Mitigates against losing a whole chain due to a single, failing module.
Serial Powering Setup

Performance evaluation of a Serially Powered Pixel Stave Prototype in Bonn.

PSPP Master board

Quad module

PSPP chip

MMC3

End of Stave

PSPP power

HV

I source

MMC3 power
Characterisation results

- The tuning plot (left) shows threshold, threshold dispersion and noise of the quad modules on the stave after tuning to 1500 e-.
  - The threshold dispersion is represented with error bars.

New chip will want to go to lower threshold.

- Minimum threshold tuning algorithms (right).
  - The first algorithm is standard minimum threshold tuning. It was performed with and without noisy FEs in the Serial Powering chain.
  - The second algorithm, Baseline tuning, is more advanced and lower minimum threshold values can be reached.
    - This was performed without noisy FEs in the chain.
Data Transmission Scheme

- Read-out system for a data-rate of several Gb/s is under development
  - Especially for inner-most layer, in which the hit occupancy is the highest.
- Readout speed:
  - Up to 5 Gb/s per data link (FE-chip) for inner-most layers.
    - Based on simulations based on the expected hit rates and the foreseen performance of the RD53
  - 640 Mb/s for the outer-most layers.

- First part of transmission implemented electrically.
  - Due to high radiation level inside the detector.
  - Signals to be converted for optical transmission at larger radii.
  - Cables are being developed for electrical data transmission at rates of up to 5 Gb/s over several metres.
Summary and Conclusion

• Challenging project, particularly due to the:
  – Radiation background.
  – Sensor surface area required.
  – Increased data-rates.

• Variations of sensor technologies have been characterised and tested in test beam environments.
  – Each technology has advantages and disadvantages depending on the layer position.
  – Likely that multiple technologies will be used to utilise the advantages.

• Solutions for the links for the readout and supply chain are being investigated.

• The ITk Pixel Project is in a good condition for the TDR in 2017.
Thank you for your attention.
Backup
Large Hadron Collider at CERN (Geneva, Switzerland)
Pixel Layout

ATLAS ID today

LoI Tracker in HL-LHC in 2012
Pixel Layout

- Initial concept to be chosen early-2017.
- Final design to come with the Pixel TDR, late-2017.
Current ATLAS Pixel Readout

Figure 23. The elements of a pixel barrel module. Most of the thermal management tile (TMT) on to which the module is glued is suppressed.

- sixteen front end electronics chips (FE) each containing 2880 pixel cells with amplifying circuitry, connected to the sensor by means of fine-pitch bump bonding (see section 6.2);
- a fine-pitch, double-sided, flexible printed circuit (referred to as a flex-hybrid) with a thickness of about 100 µm or outputs signal and power;
- a module control chip (MCC) situated on the flex-hybrid;
- for the barrel modules, another flexible foil, called a pigtail, that provides the connection to electrical services via a microcable, whereas for the diskm modules, the microcables were attached without the pigtail connection [4].

The concept of the ATLAS hybrid pixel module is illustrated in figure 23. Sixteen front-end chips are connected to the sensor by means of bump bonding and flip-chip technology. Each chip covers an area of $0.74 \times 1.09 \text{cm}^2$ and has been thinned before the flip-chip process to $195 \pm 10 \mu m$ thickness by wafer-back grinding. As a sizable fraction ($\approx 25\%$) of the front-end chip is dedicated to the End-of-Column (EoC) logic. Once bonded, most of the EoC logic extends beyond the sensor area. Wire bonding pads at the output of the EoC logic are thus accessible to connect each front-end chip to the flex-hybrid by means of aluminum-wire wedge bonding. Copper traces on the flex-hybrid route the signals to the MCC. The MCC receives and transmits digital data out of the modules. The flex-hybrid is also used to distribute decoupled, low-voltages to all the chips. The traces are dimensioned such that the voltage drop variation is limited to $\approx 50 \text{mV}$ in order to keep all the chips in the same operating range. The back-side of the flex-hybrid must be –40–
Pixel cell designs

Planar (a) design 2
25x100

Type-2
50x50 PolySi offset rail

(b) Type-6
25x100 PolySi/offset rail

(c) 3D
50 x 50

50 μm

50 μm

L~35 μm

L~28 μm

N col.
P col.
Bump pad

Sim.

25 x 100

25 μm

100 μm
Chronopixel highlights

- **Monolithic CMOS** design; 25µm x 25µm currently; 280 µm thick (standard CMOS process); charge collection by diffusion.
- Electronics for each pixel records hits above an **adjustable threshold**; electronics under each sensor.
- **Time of each hit is stored in each pixel**, up to a total of 2 hit times per pixel in current version.
- Only the coordinates (x,y,t) for hit pixels are read out.
- With such small pixel size, analog information is not needed for precision tracking.
  - so **only digital readout**
  - electronics considerably simplified.
- Prototype 3 is currently under study.