Tests with beam setup of the TileCal Phase-II upgrade electronics

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On behalf of the ATLAS TileCal Community

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INTRODUCTION

Motivation for Upgrade

- Phase II 2023 - High Luminosity LHC
- Increased designed luminosity
  - More events accepted with current criteria
  - More data generated ~500X
  - Better precision and granularity needed
  - Triggering and event selection
- Ageing of components (> 10 years) and the need for better radiation tolerance

<table>
<thead>
<tr>
<th></th>
<th>Present</th>
<th>Phase-II</th>
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<tbody>
<tr>
<td>Total BW</td>
<td>~205 Gbps</td>
<td>~80 Tbps</td>
</tr>
<tr>
<td>No. Fibres</td>
<td>256</td>
<td>8192</td>
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<tr>
<td>BW/drawer</td>
<td>800 Mbps</td>
<td>320 Gbps</td>
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Test Beam Objectives

- Aiming at the physics measurements (electrons/muons/hadrons)
  - Electrons (EM scale)
  - Muons (Tile tomography)
  - Hadrons (jet/Etmiss performance)

- Assess the status of the demonstrator based on 3in1s
  - Reliability, operation and performance
  - Feedback on existing/potential problems
  - Estimate future commissioning efforts

- Measuring some detector performance in well controlled environment for ATLAS
- Attention and help to FATALIC and QIE
- Demonstrator remains the top priority
Super-drawer DEMONSTRATOR composed of 4 independent mini-drawers, each of them;

- 12 PMTs, 12 front-end boards (3in1 option)
- 1 MainBoard (MB): for the corresponding Front-End option, ADCs
- 1 Daughter-board (DB): common design
- 1 HV regulation board: 2 options (Remote HV & HV_Optos)
- 1 adder base board + 3 adder cards (for trigger)
- New LVPS architecture: redundancy and Point Of Load regulators - LVPS v.8.01

Read-out strategy

- Data readout at 40 MHz to Preprocessor (PPr) off-detector
- Digital trigger with possible full granularity and precision
- Read-out to Front End LInk eXchange (FELIX) after L0 or L1 [more_on_FELIX]

Max PMT# in a detector drawer is 45, even though the Mainboard can load up to 48 PMTs

FELIX is a PC-based multi-interface device designed to mediate between ATLAS detectors which use the GBT protocol, and the ATLAS DAQ system.
3in1 Option (University of Chicago)

- Sharper, bi-gain clamping amplifiers and slow integrator
- 12b ADCs on MB
- Charge Injection Scan (CIS) calibration on every PMT channel
- Improved radiation tolerance, noise performance and linearity
- Commercial off the shelf
- 100 prototype 3-in-1 cards built for demo to test performance

QIE (Argonne)

- ASIC - Charge Integrator and Encoder
- Calibration DACs; Integrator ADC; ADC CAL circuit
- Most of the circuitry is in the QIE front-end cards.
- First units produced and tested in 2016-TB1

FATALIC (Clermont-Ferrand)

- ASIC - 3 gains
- 12b ADCs - 40 MSPS
- Calibration Charge injection in FEB
- Mainboard with Integrator ADC functionality
- First units produced and tested in 2016-TB1
- 2016: Finalize R&Ds; validation and performance on beam tests, TC review of Demonstrator, R&D documentation on the IDR.

- 2017: Demonstrator installation (16EOYSD) postponed
  - 2 Test-beam sessions (June and September ?)
  - Options down-selection & TDR
New Cherenkov installed for September 2016 Test-beam
Two High Voltage regulation options
- Remote regulation + individual cables to the PMTs:
- HVOptos: largely based on the existing system use Kintex-7 FPGA in the daughter board for control of HV settings and monitoring.

→ fLVPS (Finger Low Voltage Power Supply)
Analog trigger output for Demo and Legacy

TB CONFIGURATION - BACK-END (AS OF SEPT 2016)
- TileTB partition uses tdaq-06-01-01 and tile-6.1.1.0 software releases.
- Same DAQ Online Software as currently running in ATLAS experiments
TB CONFIGURATION - TDAQ/DCS SOFTWARE

- **Demonstrator**
  - Backward compatibility with TTC and TDAQ
  - Special segment in TDAQ for configuration
  - Calibrations in TDAQ infrastructure
  - DCS (Detector Control System) GUI
  - DQMD (Data Quality Monitoring Display)

- **Standalone software**
  - PPr monitoring - links configuration
  - Expert Prometeo Web based Panel
  - DAQ - Calibrations
  - DCS - lower level emulates CANbus with PPr and Ethernet port
**DEMONSTRATOR STATUS: CHANGES W.R.T 2015 TB**

- **New hardware components**
  - DBv4: No CDCE but GBTx (GigaBit Transceiver) for clock recovery, Remote FPGA reset
  - Mainboard v2: Frame/bit clock for ADC de-serialisation; Correct channel orientation + new 3in1 cards
  - PPr prototype: new module, no auxiliary boards, operation at 40.08 MHz (4.8 Gbps - 9.6 Gbps), firmware optimisations
    - Common PPr firmware for the 3 Front-End option.

- PCIe module for read-out (basic pseudo-Felix) - kc705 dev module - PCIe
  - GBT link/data-format compatibility with official FELIX
  - Free the IPbus for control, DCS and monitoring
  - Run parameters fragment (run number, L1ID, BCID, calibration)

- New DCS firmware (DB and PPr)
- Mobile Cesium unit in test-beam to perform in-situ Cs calibration runs (New in 2016)
• Operated in parallel all the 3 front-end options for the entire test-beam period
  - 3in1: One complete modules (45 channels)
  - QIE/FATALIC: half module each

• New software to improve the communication through IPbus with PPr
  - Improved the PPr memory stability for multiple application access
  - DCS IPbus OPC server (HV and temperature monitoring)
  - Link status monitoring
  - Front-end configuration at the start of a run

• All calibrations integrated within the TDAQ infrastructure (CIS, MonoCIS, LED and Pedestals)

• Up to 3 PPr/pseudo-FELIX operated in parallel
• Certification of the demonstrator analog trigger signals
• Optimized the GBT latency
  - Reduced and deterministic latency
  - Constant and stable timing
  - Initialization procedure to be optimized

• DB/MB FPGAs Remote programming is now ready
PERFORMANCE ANALYSIS OF THE FRONT-END OPTIONS

- Characterization of the 3 different front-end options and 2 HV regulation systems
- Results are presented in the IDR
- Defining the criteria for the option down-selection

3in1 - HG

Fatalic

QIE

Response of the QIE chip. All Cap IDs are combined.
Physics program to study response to muons, electrons and hadrons.

Data analysis has recently started:
- Examples of some preliminary results
- Analysis from 2016 TB to provide performance results for the different options for selection
- Identify problems and/or weak points with the system
- Provide studies about the stability of the common read-out electronics
CONCLUSIONS

- Upgrade activities are progressing well with the goal of test-beams to do performance analysis for the 2017 option down-selection
- The reliability and stability of the system has been visibly improved with respect to the 2015 TB
  - New hardware components: 3 front-end options running all at once in parallel
  - DCS firmware and software
  - front-end-back-end links: better stability, fixed latency issues and front-end clock recovery
  - Integration with legacy TDAQ software
  - Tests with FELIX system
- More design iterations needed
  - Firmware/Software (DCS, improve reliability in configuration)
  - DB - PPr GTX running at 9.6 Gbps out of specs; new revision of the DB design to use Kintex US+
  - Complete the radiation hardness program
- Demonstrator analog trigger signals integrated successfully into the DAQ for commissioning
- Calibration runs (CIS, CIS mono, Ped and LED) successfully integrated as well
- IDR has been handed over to the review committee (December 2016)
BACKUP
• All mini-drawers are powered using V.8.0 fLVPS (10V)
• Demonstrator SD uses both HV options; Remote and HV Opto
• Demonstrator is readout standalone through FELIX and Legacy ROD
• QIE and FATALIC are only readout through FELIX
• Cs calibration system (new in 2016)
The online monitoring infrastructure has been improved by increasing the buffer in the monitoring tasks and also adding an additional 3 computers. About 4 monitoring tasks have been set up on each of this computer. Monitoring data is received via FELIX from Demonstrator, FATALIC, and QIE. New algorithm has been prepared to publish monitoring histograms on online histogramming server (OH) (for online only).
- Integrated Demonstrator trigger output readout into the DAQ for commissioning.
- QDC used to read the trigger output with LED signal.
- The values in red correspond to two sets of alternating values (one for the legacy and one for the demonstrator in bold)
- This was done after the TestBeam session, and thus, the trigger signals were achieved using the LED system.
DATA ANALYSIS FROM THE DISTINCT FRONT-END OPTIONS
sROD PROTOTYPE

Power Modules
- Linear Technologies
- Low noise
- Jitter cleaners
  - TI CDCE62005
  - Low jitter (< 1ps)
- Clean recovery clocks for GTX
- Unify clock domains

Power supervisory IC
- LT LTC2977
- Power sequencing
- Protection
- Current, voltage, temp.

MiniPOD TX
- 12 x 10 Gbps
- L1 trigger communication

MiniPOD RX
- 12 x 10 Gbps
- Test purposes

Clock generator
- LMK03806B
- 10 diff outputs
- Low jitter

MiniPOD USB ports
- Ethernet port
  - 10/100/1000 Mbps
  - PC communication

SFP module
- TTC reception
- Communication with current DAQ system
  - 4 x QSFP modules
    - FE communication
    - Each module at 40 Gbps
    - Total max. BW: 160 Gbps

JTAG programmer
Current TileCal Readout architecture

Phase-II Upgrade TileCal Readout architecture