USERS MANUAL FOR THE 300 GeV MAGNET TEST SUPPLY (400 V, 5000 A)

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# USERS MANUAL FOR THE 300GeV MAGNET TEST SUPPLY (400V, 5000A)

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1. Specification

The magnet test power supply is used for testing the main ring magnets for the 300 GeV synchrotron. These magnets have the following characteristics:

<table>
<thead>
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<th>Characteristic</th>
<th>Type B1</th>
<th>Type B2</th>
<th>Quadrupole</th>
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<tr>
<td>Peak current (Amps)</td>
<td>4900</td>
<td>4900</td>
<td>2000</td>
</tr>
<tr>
<td>RMS current (Amps)</td>
<td>3100</td>
<td>3100</td>
<td>1200</td>
</tr>
<tr>
<td>Resistance at 22.5°C (mΩ)</td>
<td>3.23</td>
<td>4.42</td>
<td>10.8</td>
</tr>
<tr>
<td>Max. Inductance (mH)</td>
<td>7.73</td>
<td>9.9</td>
<td>17.9</td>
</tr>
<tr>
<td>Peak stored energy (KJ)</td>
<td>88.2</td>
<td>113</td>
<td>32</td>
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The testing involves connecting 4 magnets in series with a reference magnet and making field measurements relative to the reference magnet. This gives a load for the power supply of 5 magnets in series. The current cycle for the test is as shown in fig.1.

The power supply was designed to meet the current pulse requirements for the B2 magnets. The maximum rise time is 4.9 KA/sec.

This gives \[ V_0 = (R \text{Im} + L \frac{dI}{dt}) \times 5 \]
\[ = (4.42 \times 5 + 9.9 \times 4.9) \times 5 \]
\[ = 353 \text{ volts.} \]

With cable drop allowances, and limitation allowance, and regulation this comes up to 400 volts.

The peak current was chosen as 5000 Amps and the r.m.s. current as 4000 Amps, which is higher than the r.m.s. current of the magnets but gives more flexibility to the supply.
The ripple requirements are of the order of $10^{-4}$ of the set value, long term stability $10^{-4}$ of maximum, flat-top slope less than $10^{-4}$ per second, and no overshoots or undershoots are tolerated.
2. General Description

The power supply is a 24 phase rectifier delivering 5000 Amps peak (4000 Amps r.m.s.) at an output voltage of 400 volts (see fig.2 and fig.3). The input voltage (18 kV) is reduced to 6 kV by a stepping transformer which has 5 positions (6 kV; 4,8 kV; 3,6 kV; 2,4 kV; 1,2 kV). This enables the supply to be adapted to different loads. The stepping transformer output voltage is fed to the rectifier transformers via a distribution system in a H.V. cubicle (6 kV cubicle). There are two separate rectifier cubicles, each containing a 12 phase rectifier (Rectifier 'A' and Rectifier'B') The rectifier transformers have polygon connected primaries enabling ± 7,5° el. phase shifts to be made. This gives the necessary 15° e1. phase shift for the 24 phase rectifier. The secondary windings are star and delta for each 12 phase rectifier. The two 6 phase thyristor bridges of each rectifier are connected in parallel via an interphase transformer. The negative output terminals of each 12 phase rectifier are connected together in the D.C. filter cubicle and become the negative output terminal of the system. The positive output terminals of each 12 phase rectifier are connected together via a 24 phase interphase transformer, and this output goes through an LC passive filter to the positive output terminal of the 24 phase rectifier. Each thyristor has a free-wheeling thyristor across it to reduce ripple and reactive power. This free-wheeling thyristor is blocked during de-excitation of the magnets.

The control electronics (fig.4) offer the possibility of generating the current reference waveform locally by means of thumbwheel switches and a timing unit, or alternatively by computer control. The current reference waveform is "rounded off" to prevent overshoots and is fed to the current loop. An internal fast voltage loop is incorporated to correct for main variations. In addition there is the necessary protection and auxiliary control electronics.
3. Power Circuitry

(a) Stepping Transformer

The stepping transformer is a clophene filled 2 MVA unit with a basic stepdown of 18 kV to 6V and thereafter in steps of 20% to 1,2 kV. The primary is "delta" and the secondary "star" giving a phase advance of 30° el. The tap changing mechanism is motor driven and operated only under NO LOAD conditions. Protection devices incorporated are a Buchholz relay with two levels (warning and alarm) and a temperature control with two settable levels (warning and alarm). The output 6 kV is protected by line fuses of 250 Amp. rating. The control electronics for the motor drive is described later. (Stepping transformer control electronics).
(b) 6 kV Cubicle

The 6 kV from the stepping transformer goes to the 6 kV cubicle. On the 6 kV cubicle input is a manual circuit breaker with an earthing switch and position indicating contacts. The earthing switch is mechanically interlocked with the circuit breaker, and earths the input end of the 6 kV. This means that any involuntary switch-on of the 18 kV would feed the 6 kV to an earthed short circuit. This involuntary 18 kV switch-on is inhibited by the information from the position indicating contacts on the circuit breaker and also by door contacts on the 6 kV cubicle. After the circuit breaker the 6 kV lines are taken to distribution bars. Current transformers are fitted such as to give readings of the total 6 kV current, and voltage transformers give the line voltages. These values are displayed on meters. From the distribution bus-bars two outputs go to the two rectifier cubicles and a third output is available for an ac. filter unit should this later be considered necessary. On each of these three outputs a.c. current transformers (mounted on two of the three phases) are fitted. The secondaries of these transformers go to overcurrent protection relays (Siemens type R2As52K) (see fig.5). The current transformers give 5 Amps. secondary current for 100 Amps. primary current in the case of the rectifier output, and 5 Amps. secondary for 50 Amps. primary in the case of the a.c. filter output. The overcurrent relays have a thermal switch-off with variable delay and an electromagnetic switch-off. The thermal switch-off is set to 5 Amps and 0,5 seconds, and the electromagnetic at 15 Amps. The actual value of line current to each rectifier during 5000 Amps. flat top is 85 Amps.rms., giving 4,3 Amps. maximum to the protection relay. The protection relay contacts are used to switch off the 18 kV circuit breaker (for details see logic protection circuitry). The 6 kV outputs to each rectifier and to the a.c. filter are fused (Siemens H.V. fuse type 3GA2117 (ssw), 6 kV, 100 Amps). A contact indicates the state of the fuse and is used in the protection electronics (see later) to switch off the 18 kV.
A second compartment of the 6 kV cubicle contains the 380V auxiliary distribution system. This is mainly motor circuit breakers which supply the cooling fans etc., for the rectifiers. An auxiliary ON/OFF switch interrupts the incoming 380V to all systems. The 380V supply to the electronics crate situated in the D.C. filter cubicle is passed through an isolating transformer situated in the 6 kV cubicle low voltage compartment. This transformer has a primary connected in delta and a secondary in star giving a phase advance of 30°el. All motor circuit breakers have contacts indicating their state. The contacts are all connected in series and indicate a fault to the protection electronics (see later). A 220 volt output is also supplied for the power transformers for the D.C.C.T.'s.
(c) Rectifier Cubicle

The 6 kV from the distribution bus-bars is fed out by overhead 3 phase cables to the two rectifier cubicles - Rectifier 'A' and Rectifier 'B'. The two rectifier cubicles are almost identical - the only differences being the position of the outputs and the connection of the 6 kV to the transformers.

The transformer wiring diagram is shown in fig.6. Two sets of input terminals are available - one for Rectifier 'A' giving a 7,5° el. phase advance and the other for Rectifier 'B' giving a 7,5° el. lag. The phase diagram is shown in fig.7. The transformer has a double primary winding as shown in the construction drawing in fig.6. This effectively decouples the two secondaries reducing the mutual interference of commutation spikes. The transformers are forced - air cooled by means of two fans each.

The transformer outputs feed to three-phase thyristor bridges, (fig.8), via line fuse. The line current is 816 Amps (rms) for 4000 Amps output (r.m.s. max. over the magnet cycle) and 1020 Amps (rms) during the flat top current. The fuses are 1000 Amp r.m.s. rating (Ferray 600 volt, URG 1000 Amps.). The $i^2t$ value (at 300 volt) is $\approx 370000A^2S$. The fuses have indicating contacts which are all connected in series and used to switch off the 18 kV. The $i^2t$ value of the thyristors is 405000A²S at a junction temperature of 124°C, and 550000A²S at a junction temperature of 45°C.

The thyristors are of the capsule type (type T500N1100EOB from A.E.G.), mounted on cooling fins (type KL181 from Seifert), for double sided cooling. The assembly of thyristor cooling fins, R.C. network, pulse transformer, and front panel is regarded as a unit and made such that all such units are inter-changeable - the spares are also such units. In order to change a thyristor the copper bars and fuses in front should be removed and the whole unit (as above) withdrawn. The cooling is by fans; four per rectifier. The thyristor voltage rating is 1100 volts (safety factor = 2,5). The firing pulses are fed
to the thyristors via pulse transformers (type ZKB 443/030 from Vacuumschmelze) and a current limiting resistor. The pulse gives a peak firing current of about 2 Amps. A free-wheeling thyristor is connected across each bridge. This thyristor is fired just after the negative-going zero voltage crossing of the bridge voltage and it is blocked before the bridge goes into inversion to de-excite the magnets. The free-wheeling thyristor is identical to the main bridge thyristors and has a fuse in series with it. Since the main thyristor bridge is never blocked this fuse cannot give rise to dangerously high voltages for the load should it interrupt during free-wheeling. A basic load resistor is connected across each bridge (120 Ω 2 kW) to enable start-up with an inductive load.

The two thyristor bridges (from the star and delta transformer secondaries) are connected in parallel via an interphase transformer. The interphase transformer has an air-gap to avoid saturation due to imbalance of the bridges and in this air-gap a Hall Generator is introduced. The Hall Generator has a sensitivity of 150 mV/KG and is used to balance the bridges (see later).

A surge suppression network is added across the transformer outputs as shown in fig.2. The protection fuses are visible through the plexiglass doors of the rectifier.

The thyristor firing pulses and the auxiliary voltages arrive at AMP connector strips in the rectifier cubicles (see inter-unit cabling lists).

The output positive and negative terminals pass by means of flexible leads through the walls of the rectifier cubicles into the D.C. filter cubicle.
(d) The D.C. Filter Cubicle

The two rectifier outputs connect through into the D.C. filter cubicle where the negative outputs are commoned and the positive outputs connected together via an interphase transformer. The interphase transformer has an air-gap in which a Hall Generator is situated. The Hall Generator output is used to balance the two rectifiers.

The combined 24 phase output is then fed through a passive filter (see fig.9.). This filter gives an attenuation of 20 dB to the basic rectifier output component of 1200 Hz. The choke has a 200 μH inductance (5000 Amp. pk, 4000 Amp. r.m.s. rating) and is forced air cooled. The condensers are metallised paper type in units of 255 μF (630 volt) (type 0670 404 003 from Bosch). Four such units are mounted on an insulating plate (Pecolit-glass fibre reinforced polyester) and in all there are 11 such plates. The condenser terminals are AMP. connectors. The complete condenser assembly is protected by a 400 Amp. fuse (Ferraz 600 URG 400 Amp.) with warning contact.

On the negative output bus-bar a shunt (60 mV at 5000 Amps.) gives the output current measurement to an ammeter mounted on the front of the cubicle. The output voltage is also displayed. On the negative output two D.C.C.T.'s are mounted. One is used in the current control loop and the other gives a magnet current reading to the computer. The D.C.C.T. outputs are isolated from the power circuity.

The auxiliary inputs and protection outputs are taken to an AMP connector strip.

Also situated in the D.C. filter cubicle is the "Power Supply Electronics" crate, which contains the Gate Control Sets for the rectifier, the protection logic, the supply transformers for the D.C.C.T.'s the D.C.C.T. measurement cards and buffer amplifiers for sending and receiving analog signals from the main control electronics crate situated some 10 meters away in the control room.
4. **Electronics**

It is assumed that the reader has the necessary circuit diagrams, and crate wiring and lay-out diagrams. Those circuits whose function is obvious from the circuit diagrams - such as protection circuitry, BCD to Binary decoders, command selectors, etc. - will not be described in detail.

(a) **Power Supply Electronics**

The electronics crate situated in the D.C. filter cubicle contains the gate control sets for generating the thyristor pulses for the rectifiers and free-wheeling thyristors, the power transformers and measurement cards for the DCCT's, the protection circuitry for the power supply, and a buffer amplifier to receive the gate control voltage input from the control room, and to send the control D.C.C.T. output voltage to the control room electronics.

(i) **The Gate Control Set**

The basic 12 pulse gate control set consists of four plug-in units.

- **Frequency Multiplier and Pulse Selector (4015P)**
- **12 x Ramp Generator (4044P)**
- **6 x Output Stage (4048P) - 2 off.**

**The Frequency Multiplier and Pulse Selector (U-4015P)**

Is basically a 600 Hz mains synchronised oscillator which supplies 12 output pulses per 50 Hz period to trigger ramp generators in the 12 X Ramp Generator card. A reference 50 Hz signal (S-T) is fed in through a filter to a squaring circuit (see dwg. 125-4015P) Al a, and then to a ramp generator Al b. Fig. 10 shows the waveforms. The ramp is then compared with a potentiometer voltage P1 and an offset voltage, and when the resulting voltage
becomes greater than zero the discriminator A2 output goes positive. The potentiometer P1 is a set-up for the positioning of the output "ramp-trig-gering" pulses. Fig. 11 shows the range of setting up possible with potentiometer P1 with particular reference to a star primary, zig-zag secondary, application. The discriminator A2 output triggers a monostable IC1 which gives the 50 Hz reference pulse. A 600 Hz oscillator (unijunction transistor T4) is synchronised every 20 ms by this 50 Hz synchronising pulse and in addition has its frequency stabilised against the mains by a bang-bang feedback loop. The oscillator pulses are fed into a counter and the twelfth pulse compared with the 50 Hz reference pulse. If the twelfth pulse comes before the 50 Hz synchronising pulse a bistable circuit IC2 is triggered such that its output, via transistor T5, feeds a voltage back to the oscillator such as to lower the oscillator frequency. If the twelfth pulse arrives too late (i.e. is caused by the synchronising pulse) the bistable circuit IC2 is triggered such that it increases the oscillator frequency. The voltage on the collector of T5 (Vt) should be set up by potentiometer P2 to read 6.3V on a voltmeter (not a digital voltmeter). This means that the correction system is in the centre of its range. The 600 Hz pulses are formed (100μs) in monostable IC5 and then used to reset the 600 Hz ramp generator A3a. The ramp generator output is compared with the current balance signal which is fed in on alternate ramps (divide by two counter output of IC3 via FET, T8, chops the current balance input voltage) and an offset voltage. The zero level is detected by discriminator A3b, which, via bistable IC7, generates the delayed 600 Hz pulses in monostable IC8. The delayed 600 Hz pulse train is then separated out into 12 output pulses on separate lines. This is done by using the 50 Hz synchronising pulse to set up shift registers IC10, IC11, IC12 such that the first output (CI10, pin 13) is positive and all others zero. The non-delayed 600 Hz pulses then clock this positive output sequentially through the shift registers. The shift register output open the gates IC13, IC14, IC15, consecutively allowing the delayed 600 Hz pulses to be fed out through the twelve gates in sequence.
The 12 x Ramp Generator (U-4044P)

Uses the pulses from the Frequency Multiplier and Pulse Selector to start and stop ramps. The ramps are compared with the control voltage from the 12 phase adapter to generate the 'α' delay for the output pulses. The input pulses reset the integrator, which generates the ramps, by means of a F.E.T. The ramp is compared with the reference and the following discriminator output used via a bistable (to prevent multipulsing per period) to generate the output pulses. Since the total range of output 'α' is about 150°el, then each channel can be used twice per 50 Hz period generating two pulses 180°el. apart. A logic circuit decides where the pulses go. This "double ramp" is shown in fig.11. In each channel except the first channel there are two potentiometers - the zero set up and the ramp set up. The first channel has fixed resistors and acts as a reference to which all the others are aligned. The method of setting up is as follows. With a control input voltage V ~ + 9 volts the "zero" potentiometers are adjusted to give the correct output pulse spacing (referred to pulse 1), and then with V ~ - 5V input control voltage the "ramp" potentiometers are adjusted to align the pulses. This process is repeated once again and the resulting pulse displacements should be less than 0,2°el. The pulse delays with respect to pulse 1 can be measured by a counter.

The 6 x Output Stage (U - 4048P)

Amplifies the pulses from the 12 x Ramp Generator and drives the thyristor pulse transformers. The "start-up" double output pulses are achieved by addition of the necessary pulses on the input gates. A blocking signal (OV) to the second gate of ICl allows blocking of the output pulses. In addition a Σ output pulses (diode addition) is available. When a transistor short circuits this signal output is held down to zero and after a delay appropriate action is taken (see 12 Phase Adapter), and the fault "Gate Control Pulse" appears.
The gate Control Sets for the 'A' and 'B' rectifiers are identical and the necessary $15^\circ$ cl. offset is made by adjustment of the potentiometer P1 on the Frequency Multiplier and Pulse Selector Card.

The control input signal is the same for each gate control set and is derived from the 12 Phase Adapter.

The 12 Phase Adapter (U-4053)

The 12 Phase Adapter (4053P) takes the output voltage from the voltage regulator and sets the $\alpha_{\text{min}}$ and $\alpha_{\text{max}}$ firing limits for the rectifier. The limits are $+9$ volts and $-5$ volts respectively, and the limiting is carried out by comparing the control voltage $U_{\text{out}}$ with a reference on a potentiometer and using the resulting signal via a high gain amplifier A1 to clamp the output. Two potentiometers set the $\alpha_{\text{min}}$ and $\alpha_{\text{max}}$ levels. The input signal from the voltage regulator is received by a common-mode amplifier A3. An Inversion input (OV) drives the control voltage to the inversion limit ($-5V$). The 2 output pulses from the 6 x output stages is used to give a pulse monitor display which shows the regularity of the output pulses by converting the pulse spacing to a ramp function. This output shows missing pulses and irregularities clearly. In addition a permanently shorted output transistor causes the logic circuit IC2 to open relay R11. This relay opens the 40 volt supply to the thyristor pulse transformers but sufficient current passes through R46 (1.5K) to allow the 40 volt level to return if the fault is removed. The reason for this current limitation is to prevent burn out of the current limiting resistors in the 6 x output stage in the event of an output transistor short circuit. A fault signal is also sent out which puts the power supply into inversion and the program input to zero.

The Gate Control Set for the free-wheeling thyristors differs from that of the main thyristors in that the pulses have fixed positions (immediately after the bridge output voltage goes negative) and are blocked during the bridge inversion period when the magnets are de-energised and a
negative output voltage is necessary. A Frequency Multiplier and Pulse Selector generates the necessary fixed output pulses for the free-wheeling thyristors of one rectifier and the 15° el. delay for the pulses of the free-wheeling thyristors in bridge 'B' is made in the Pulse Adder and Current Balance Unit.

The Pulse Adder and Current Balance (U-4070)

The Pulse Adder and Current Balance (U-4070) unit contains three separate functions. These are the current balance system, the free-wheeling thyristor pulse distribution, and part of the free-wheeling thyristor blocking logic. The current balance system uses Hall Generators (type SW110/II from Siemens) situated in the air-gaps of the three interphase transformers. The control currents are sent via 470 Ω resistors (R1, R10, R19) and the Hall voltages arrive to the "common mode rejecting" amplifiers IC1, IC2, IC3, the second parts of which have the necessary stabilising networks. The outputs are fed to the two main rectifier Frequency Multipliers and Pulse Selector. The 12 phase bridge current balance signals are used as described in the Frequency Multiplier and Pulse Selector description. The 24 phase current balance voltage acts at the same point as the 12 phase current balance signal but is not chopped by the FET (T8) and so shifts all the output pulses of one Frequency Multiplier and Pulse Selector with respect to the other. The signal level on the current balance outputs is fed through diodes to a discriminator and in the event of a too high level being required a fault "Current Balance Fault" is given which sets the program to zero and inverts the bridges. This signal must be reset manually.

The second function is the pulse distribution of the free-wheeling thyristor pulses. Fig.12 shows the required pulses. For each bridge the free-wheeling thyristor must be fired every 60° el. Thus for one rectifier the 12 pulses per period can be generated from one Frequency Multiplier and Pulse Selector by taking alternate pulse for each free-wheeling thyristor.
This is done for the rectifier 'A' - the alternate pulses being added together by diodes D 9 - D 14, and diodes D 15 - D 20. The pulses for the 'B' rectifier free-wheeling thyristors which come 15° el. later than the 'A' rectifier free-wheeling thyristors are generated as follows. The 12 pulse 'A' train of pulses is made to generate a delay of 15° el. (0.083 ms.) in delay circuit IC6. The delayed output generates a pulse in the monostable IC7, thus giving a 12 pulse per 50 Hz period train of pulses delayed 15° el. with respect to the 'A' rectifier pulses. Theses pulses then pass to two gates which are driven from a bistable circuit. The bistable inputs are, referring to fig.12, the $F_{AA}$ pulses and the $F_{BA}$ pulses. The $F_{AA}$ pulses put the bistable in the state that the gate to the $F_{AB}$ output is open, and hence the pulse 15° el. later passes to the $F_{AB}$ thyristor. The bistable is then put to the other state by the $F_{BA}$ pulse so allowing the $F_{EB}$ pulse to be released.

The third function on this unit is part of the blocking logic for the free-wheeling diodes. The main part of this logic is situated in the Earth and Overcurrent Protection Card (4071P) in the control room electronics crate and the whole logic function is described later under this heading.

The rectifier inversion signal arrives also on this card where it is passed through an inverting gate before going to the adapter card.

(ii) The Protection Logic in the Power Supply Crate (U-4365)

The function of this card is clear from the circuit diagram (q.v.). The different fault inputs which are zero levels via contacts are collected together, memorised where necessary, and sent to the protection logic card in the control room electronics. Those faults which are considered the most dangerous and are made to switch off the 18 kV supply, are duplicated and a separate output called $E$ Power Supply Failures (18 kV off). The other more minor faults are combined to give a second output called $E$ Failures (program to zero) which is used to set the current program to zero. Both these operations are carried out in the control unit protection circuitry.
(iii) **D.C.C.T. Cards**

The circuit lay-out of the D.C.C.T.'s is shown in the U3-4349 drawing. The transformers which supply the 140V. and 10V. levels to the two D.C.C.T.'s are situated in U6-4367. The D.C.C.T. is of the "parallel" cores type and the burden resistor is trimmed to give 10 volts for 5000 Amps. (the calibrating is made with a 10 kΩ resistor load on the output). The characteristics of the D.C.C.T.'s are as described in MPS/ED Note 73-3 "A New and Simple DC - current Transformer with High Precision" (M. Häusler).

(iv) **Power Supplies (+15V, -15V) and (+35V, +5V)**

The +15V, -15V power supply (U-4345) consists of a series regulator type LM723CN with a power transistor output. In the case of a short circuit on the output which would overheat the power transistor (type 2N3055) a unijunction oscillator is allowed (after ~ 1 sec.) to fire a thyristor which shorts out the unregulated voltage input and blows a protection fuse. In parallel with the fuse is a lamp which illuminates when the fuse is blown.

The +5V, +35V power supply (U-4345) has an identical regulation and protection as in U-4345 for the +5V, and the +35V is unregulated.

(b) **Control Room Electronics**

The control room electronics divides into three main functions.

i) The current reference generation and control loops (crate 'B')

ii) The power supply protection circuitry (crate 'A')

iii) The magnet protection circuitry (crate 'C')

In addition there are powers supplies (+15V, -15V) and (+35V, +5V) which are identical to those described under Power Supply Electronics crate, and also a +5V (5A.) supply type O1tronix.
(i) **The Reference and Control Circuitry**

Fig. 4 shows the basic scheme of the reference generation and control circuitry. The current reference wave-form is generated from three digital values, the I_{max}. or flat top current, and the I_{min}. or injection current, and the dI/dt or rate of current rise. These three values are either computer given or generated internally, as is also the timing cycle. The digital current levels are switched by the timing cycle in the digital switch and the resulting digital levels fed to the D/A converter. The square wave from the D/A converter is passed through a rate limiter which also performs certain rounding-off operations. The rate level has its own D/A converter, the output of which is used in the rate limiter. The output of the rate limiter is then the reference for the current regulator and the output of the current regulator goes to the voltage regulator. The voltage regulator output is then sent to the adapter card of the gate control set in the power supply electronics crate. The maximum voltage output of the power supply varies according to the stepping transformer position and in order to keep a constant gain in the voltage loop the rectifier voltage is passed through an attenuator on the "Stepping Transformer Position" unit. This attenuator varies according to the stepping transformer positions. The gain in the current loop remains normally constant since the stepping transformer position is related to the quantity of magnets in the load.

**BCD - Binary Decoder (U3-4065)**

This unit uses the SN 74184 BCD - Binary decoding units to decode the contraves switch I_{max}. set level from BCD to pure binary for the D/A converter. The maximum input allowed is 4999 Ampères otherwise saturation may occur in the D/A converter which gives 10 volts output for 5000 Amps.

**BCD - Binary Decoder (U3-4361)**

This unit is as above but has only 10 bit capacity. The maximum value of injection current allowed is 499 Amps. (1 bit = 1 Amp).
D/A Converter (U3-4063)

The two digit contraves switch $dI/dt$ level (in KA/sec. with a maximum value of 4.9 KA/sec.) is decoded to binary (SN 74181+, Texas instruments). A logic circuitry selects either this local value of $dI/dt$ or a computer input value (6 bits, max 4.9 KA/sec., each bit corresponds to 100 A/sec). The selection depends on the state of the computer/local switch situated on the front panel of the "Digital Switch" unit. The digital value is then fed to a D/A converter (8 bit, ZD 430 from Zeltex). The current output of the D/A converter gives via an amplifier (UA 741) the output $dI/dt$ reference voltage. The amplifier gain is chosen such that for a 4.9 KA/sec. value of $dI/dt$, the output voltage is -10 volts with RL1 not energised (i.e. the load is dipole magnets). In the case of quadrupole magnets as load, the relay RL1 is energised and the output voltage is -10V for a $dI/dt$ rate of 2.0 KA/sec. The reason for this is that in the rate limiter the roundings off of the current reference waveform are made by setting fixed low slope rates to the reference waveform as it approaches the flat top value. These values are preset on potentiometers and since the maximum rate of current rise of the quadrupole magnets (2.0 KA/sec) is lower than that for the dipoles (4.9 KA/sec) these roundings off would have to be changed depending on whether dipoles or quadrupoles were being tested. To obviate this difficulty the quadrupole slope-rate is amplified relative to the dipoles by a factor $\sqrt{2.45}$, the "roundings off" made as for a dipole load, and the new slope-rate function attenuated by the same factor and used as the $dI/dt$ reference. The attenuation is carried out also by RL1. The de-energising $dI/dt$ of the magnets which is a fixed potentiometer value is similarly attenuated for the quadrupole magnets as compared to the dipoles, by means of RL1. Dual-in-line switches allow a 7 bit computer input to be fed to the D/A converter instead of 6 bit should a higher resolution be needed.

Command Selector Ul-4052

The function of the command selector is to select either the computer or local digital current levels according to the position of the switch computer/local on the front panel of the digital switch. A lamp on the front
panel indicates whether local or computer has been selected. There are two such command selector units; one deals with the 13 bit flat-top current level, and the other with the 10 bit injection current level. The units are identical and interchangeable.

**Digital Switch (U-4054)**

The digital switch unit takes the digital levels of flat-top current and injection current, and combines them with the timing to give as output the switched digital current levels for the D/A converter. The timing may be either local or remote, the required mode being selected by the computer/local switch on the front panel. The two timing modes are different in that the computer input is a 15 volt logic signal (open collector) which is positive during injection current and goes to zero for the flat-top current. The local timing consists of two separate pulses, one of which gives the start of flat-top and the other the end of flat-top. The end of flat-top signal is, in both computer and local control, delayed by approximately 30 ms. before changing the digital output from the flat-top level to the injection level. These 30 ms. are used to block the free-wheeling thyristors before the negative rectifier output voltage to de-excite the magnets is required. This function is described fully under U1-4071 (Earth and Overcurrent Protection). The 30 ms. delay is made by IC21 (computer) and IC23 (local). Both signals finally control bistable circuit IC17 which is used via driver stages to switch the 14 logic gates. On local command the function switch on the front panel can be used to select cycle, zero, flat-top current or injection current. The switch should not be left in the zero mode in computer operation since this over-rides the computer input. All other modes are inhibited if the computer switch is in "computer" position. Additionally a "Fault" input sets all digital outputs to zero independently of whether computer or local is selected. A 2048 Amp. limit input is used to limit the digital output to 2048 Amps. in the case of quadrupole magnets being tested. The digital switched output is fed to the D/A converter.
D/A Converter (U2-4066)

This unit is a fairly straightforward digital to analog converter. The basic item is the D/A converter unit type MI913A (13 bit) from Analogic. The current output is voltage converted in the output amplifiers type 3500C from Burr-Brown. The D/A converter has two built-in potentiometers for zero and full-scale setting and the amplifier has a zero offset correction potentiometer. The voltage output of the D/A converter is fed to the Rate Limiter.

The Rate Limiter (U2-4347)

Three inverting amplifiers IC1, IC2, IC3 of which IC2 is an integrator form the basic rate limiter. An overall feedback gives unity gain and the rate of voltage rise and fall is determined by the RC of the integrator and its input reference voltage. This input reference voltage is modified by the set values of dI/dt and is also used to give the "roundings off" required in the current reference waveform to avoid current overshoots and rapid rectifier voltage changes. The first amplifier IC1 has a high gain and saturates at 10 volts output for input signals greater than 0.08 volts, and comes out of saturation when the IC3 output reaches the required output level. The rate level voltage to the integrator IC2 is controlled by amplifiers IC4 (positive rate) and IC7 (negative rate). These amplifiers hold the voltage at the junction of R8 and R9 to a value given on their inputs R15 (positive) and R17 (negative). The derivation of these rate limiting values is carried out by amplifiers IC10 to IC16. Firstly the positive rate is considered. The reference voltage of the dI/dt arrives from the 7 bit converter to card input pin A3. The voltage then passes via FET T2, amplifier IC10, FET T3, and amplifier IC11 to output terminal A2. This output terminal A2 is effectively connected back to terminal A19 (see also D/A converter U-4063 for RL1 function) and used as the dI/dt positive going reference. Fig.13 shows the output waveform of the rate limiter. In order to achieve the necessary rise and fall time characteristics the dI/dt signal is acted on at
various points of the rise time. When the cycle begins (start of rise) the
dI/dt value is switched in slowly with a 30 ms. time constant. This avoids
a sharp current change which would require a voltage step in the rectifier but
gives a wrong initial dI/dt. In 90 ms. (3 x \tau) the error is less than 5%.
When the rate limiter output is within 2% to 5% I max. of its final value
a lower rate is switched in and at 1% I max. a second even lower rate is
switched in. This gives the rounding off shown in fig.13. A similar pro-
cedure for the negative dI/dt ensures no undershoot etc.. For the positive
dI/dt the starting point of the first round off is set by potentiometer P9
and the corresponding dI/dt by potentiometer P6, and the second round off
starting level is set by potentiometer P8 and its dI/dt by potentiometer P7.
The circuit function is as follows. The rate limiter input is added to the P9
setting and compared with the rate limiter output level (in IC12). When a
positive input appears (start of current rise) then provided it is greater
than the P9 setting (~ 0,2 to 0,5 volts), the IC12 output to T7 goes posi-
tive causing T7 to conduct which in turn switches on T2 and T3. The input
reference dI/dt is then switched into IC10 which has a feedback time constant
of 30 ms. This gives the 30 ms. \tau on the initial rise of current. The output
of IC11 is connected to the "positive slope rate in" terminal. When the
rate limiter output reaches the value of the input less the P9 setting, then
F.E.T.'s T2 and T3 open. This leaves as dI/dt reference the voltage derived
through potentiometer P6 from Zener diode D 15. This value is the dI/dt after
the first round off. When the rate limiter reaches the value of the input
less the P8 setting amplifier IC13 causes the F.E.T. T5 to switch on. This
attenuates the slope by an amount depending on the setting of P7. The am-
plifier IC11, the output of which changes for each new dI/dt setting is slowed
down by a feedback time constant of 10 ms. to further smoothen the dI/dt tran-
sitions. In the case of the negative going dI/dt the actual value of dI/dt
is set by potentiometer P12. The first round off starting level is set by P11
and its slope by P14, and the second round off starting level by P10 and its
slope by P13. Amplifier IC16 output (output terminal A17) is connected via
RL1 in U-4063 to the "negative slope rate reference in" on the amplifier IC7.
The voltage output from the Rate Limiter (positive) goes to the current and
voltage Regulator.
Current and Voltage Regulator (U2-4047)

The current reference from the rate limiter and the current measurement from the D.C.C.T. (via buffer amplifiers to reject common mode signals) are summed on the current regulator input (A1). The current regulator output is then summed with the rectifier voltage in the voltage regulator (IC4) and the voltage regulator output is transmitted to the adapter unit in the power supply electronics crate. The various loop characteristics are shown in fig.13. Since the maximum rectifier voltage output changes with the position of the stepping transformer the gain of the voltage loop, if it is to remain optimal, must compensate this. The compensation is made by switching various resistors in parallel to the input resistor of the voltage regulator (R19) depending on the position of the stepping transformer. The resistors are situated in the "Stepping Transformer Position" unit and are switched by relays. (see under U-4067). The voltage divider which gives 10 volts input to IC3 from the 400 volt rectifier output is situated in the rectifier (see fig.2). When the voltage regulator output saturates (level set by potentiometers P9 - negative, and P10 - positive) then a fault indication is given (IC6) which is used in the "start-stop" unit (U-4363) to give inversion to the rectifier bridges and to set the program reference to zero.
ii) Power Supply Protection Circuitry

Fig. 15 shows the scheme of the protection logic. The power supply faults are collected together in the protection unit in the Power Supply (U-4365) and sent to the protection unit (U-4364) and the start-stop unit (U-4363) in the control room. Those faults which cause the 18 kV to be switched off and may be considered as the more dangerous type are duplicated in two separate channels and operate two separate relays which switch off the 18 kV. All faults which disappear when the 18 kV is switched off or the program is switched to zero are memorised in bistable circuits which require resetting. The circuit diagrams in conjunction with fig. 15 give a comprehensive picture of the protection logic. The 18 kV ON/OFF circuitry which is incorporated in the Power Relay Unit (U-4362) is shown in fig. 16 along with the 18 kV auxiliary contacts. It should be noted that in series with the "18 kV passive OFF" signal there is a contact in the stepping transformer which opens when the tap changing motor starts driving. This is a "second line" security to make sure the 18 kV is OFF when the stepping transformer is changing its setting. When no fault is present the relays RLM1 and RLM2 are both energised. The Stepping Transformer protection circuitry is shown in fig. 17. The contacts in the stepping transformer are taken firstly to relays in the 18 kV cell where they are used to switch off the 18 kV in the event of a fault and to display the fault and sound a klaxon. Contacts of these relays are sent to the control room where they are used in the logic to switch off the 18 kV and display the faults. The indication contacts of the fuses on the stepping transformer secondary are connected in series and sent to the control room electronics protection unit (U-4364).

Earth and Overcurrent Protection (U-4071)

This unit contains three separate functions, the earth protection circuitry, the overcurrent protection circuitry, and the logic for the blocking of the free-wheeling thyristors. The earthing system for the magnet test area is described in Note No. 7 (Lab 11/MA/ER, E. Rossa). Basically a common bus-bar is connected to CERN earth by a 2mΩ Nikrothal shunt. This shunt can run
the full 5000 Amps. of the supply for about 15 seconds before it reaches its melting point of 1400°C. The voltage across the shunt is measured by amplifiers IC1 (x20) and IC2 (x180) to give ±7 volts for a ±1 Amp. shunt current. A comparator (IC2) gives an output Earth Fault indication via logic IC3. This fault signal releases the 18 kV circuit breaker. Additionally the output of IC2 is monitored on a μA meter, and the output of IC1 is available on the front panel of the unit. The fault condition is memorised in the Protection (control room) unit (U-4364). Fig.18 shows the overcurrent protection curve. The current from the control D.C.C.T. is fed via RL1 (quadrupole load) to amplifier IC5. The gain of IC5 is x1 for RL1 unenergised (dipole) and x2,5 for RL1 energised (quadrupole). This gives 10 volts for I max. irrespective of magnet type on the output of IC5. The output of IC5 is taken to IC6 which has an offset, adjustable by potentiometer P1, which sets the lower limit of action of the overcurrent protection (amine 3500 Amps. for a dipole and 1400 Amps. for a quadrupole load). The gain of the first part of IC6 is such that with a 5000 Amp. input the output is at 10 volts. The output of the first part of IC6 is then integrated in the second part of IC6. The integrator time constant is chosen such that with a 10 volt input (5000A) the output reaches the following discriminator level in 4 seconds. This level (and hence time) is adjustable by potentiometer P3. The output fault indication is used to set the current program to zero and indicate a program fault. The output of IC5 is also used directly via the level discriminator in the first part of IC4 and logic (IC12) to indicate a fault when the absolute value of current passes 5500 Amps. for dipoles and 2200 Amps. for quadrupoles. This value is set by potentiometer P3. The output fault is made to switch off the 18 kV and indicates fault I>I max. Both I>I max and Program Fault are memorised and have to be reset. The switching waveforms for the free-wheeling thyristor δγ and blocking are shown in fig.19. During the magnet de-energisation the rectifier output must go negative and therefore the free-wheeling thyristors must be blocked. Before blocking the firing angle is slightly retarded in order to be sure that commutation is taking place from the main thyristor
bridges to the free-wheeling thyristors. This is the \( \Delta \gamma \) signal which delays the free-wheeling thyristor firing pulses by about 10\(^{\circ}\)e1. Approximately 10 ms. later the free-wheeling thyristors are blocked. In the unit U-4071 the timing waveform, either computer or local depending on the position of the computer/local switch, is used to generate a 80 ms pulse at the end of flat-top signal. The output of the first amplifier in the rate limiter saturates in a positive direction almost immediately after the D/A converter output goes negative towards injection current. This is about 30 ms. after the end of flat-top signal due to the delay in the digital switch unit (U-4054). This signal is fed to the level discriminator (IC7) and the output is added in the logic (IC11) to the 80 ms monostable to give a pulse which starts at the end of flat-top current signal and ends when the injection current level is reached. The delay (~100ms) on the output of IC7 stretches the period of blocking and \( \Delta \gamma \) since the saturation of the first amplifier in the rate limiter falls off slightly too early. Additionally the bistable circuit IC11 inhibits that the \( \Delta \gamma \) and blocking arrive from the rate limiter output alone. The cycle signals, either local or computer, must be present. The input computer and local timing signals are both gated by the "start operation" signal, and in the case of local command the D.C.I. inj., D.C.I. flat-top, and D.C. zero inputs from the selector switch on the "Digital Switch" unit inhibit the Local Timing Input.

iii) Stepping Transformer Control

The Stepping Transformer Position unit (U-4067) receives the stepping transformer position indication from cam-actuated relays in the stepping transformer. (see fig.20). A zero volt signal is returned on any one of five lines indicating the five positions of the stepping transformer (20\%, 40\%, 60\%, 80\%, 100\% or positions 1,2,3,4,5 respectively). The required position is set by a switch on the front panel of the unit and a logic comparison between desired and actual position causes either the "UP" relay or the "DOWN" relay to be operated.
The following table shows the logic of the decision making.

<table>
<thead>
<tr>
<th>Actual Position</th>
<th>Required Position</th>
<th>Action</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>2</td>
<td></td>
</tr>
<tr>
<td>1 or 2</td>
<td>3</td>
<td>&quot;UP&quot;</td>
</tr>
<tr>
<td>1 or 2 or 3</td>
<td>4</td>
<td></td>
</tr>
<tr>
<td>1 or 2 or 3 or 4</td>
<td>5</td>
<td></td>
</tr>
<tr>
<td>2 or 3 or 4 or 5</td>
<td>1</td>
<td>&quot;DOWN&quot;</td>
</tr>
<tr>
<td>3 or 4 or 5</td>
<td>2</td>
<td></td>
</tr>
<tr>
<td>4 or 5</td>
<td>3</td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>4</td>
<td></td>
</tr>
</tbody>
</table>

The actual position inputs are summed to give the above indicated signals. These are then added to the required position signals as in the table. The "AND" product gives the operation shown in the third column. The output relays in U-4067, RL1 ("UP") and RL2 ("DOWN") are used to energise MORS relays in the Power Relay unit (U-4362). These MORS relays send a mains phase to energise the "UP" and "DOWN" power relays in the stepping transformer unit which energise the tap changing motor. As shown in fig.20 this power phase is interlocked with a contact on the 18 kV circuit breaker. Each position of the stepping transformer is made to actuate a relay on unit U-4067 (RL3...RL7). These relays switch various resistors between card pins A7 and A5 and this is used to vary the input resistor to the voltage regulator such that a constant voltage gain is maintained in the voltage loop irrespect-
ive of the stepping transformer setting. The stepping transformer positions are shown by L.E.D.'s on the front panel. An input on the pin A6 from an 18 kV "OFF" contact (oV) ensures that the "UP" and "DOWN" relays are not actuated when the 18 kV is on.

iv) Magnet Protection Circuitry

This is fully described in Memorandum MPS/ED/LC/bw "Magnet Protection and Fault Display for the 300 GeV Magnet Testing". This memorandum together with the circuit diagrams of units U-4370 (Magnet Failure Bank "X"), U-4371 (Reference Failure), and U-4372 (Σ Magnet Failures) is sufficient for understanding the system. Basically in each of 6 Magnet Failure Bank cards the water temperature and water flow indications from the 5 magnets in each bank are monitored and should a failure occur the program is set to zero in the power supply. Only the bank which is "selected" is monitored and the banks which are "earthed" are ignored. Should a bank appear to be "earthed" and "selected" or "not selected" and "not earthed" then this is considered a potentially dangerous fault and the 18 kV is switched off. If a magnet position in a bank is short-circuited then the water faults from that position are disregarded. All magnet faults are gathered together in the Σ Magnet Failure unit (U-4372), and fault outputs sent to the Protection units. Additionally if any quadrupole bank is selected a signal is sent to the control circuitry so that the overcurrent protection circuitry operates at the correspondingly lower level and that the negative going dI/dt is reduced (see under U-4071 and U-4063). A further fault indication is if both the short circuiting switches for the reference magnet banks and for the measurement banks are closed. This would give a short circuit for the power supply and this condition is used to switch off the 18 kV. All faults and switch positions etc. are displayed and all faults memorised in bistable circuits.
5. Security

a) Operational

While the power supply is in operation the following security features apply,

i) If a door is opened to any cubicle where a high voltage is accessible the 18 kV is switched off.

ii) If an earth current of more than 0.5 Amp. flows the 18 kV is switched off. The earth current is also continuously monitored and displayed.

iii) If the power supply is made to deliver a too high current due to a short circuit or program fault the 18 kV is switched off.

iv) The stepping transformer clophene is monitored by temperature and Buchholz relays which are set to two different levels—the lower level acting as a warning and the upper level being used to switch off the 18 kV. The inrush current at 18 kV switch-on is also measured and if excessive switches off the 18 kV.

v) 18 kV emergency-off push buttons are located in the test area.

vi) All fuses have contacts which indicate when they are blown and switch off the 18 kV.

vii) When the supply is switched off the D.C. Filter capacitor is discharged by (as well as the load) a resistor of 1 kΩ directly across the capacitor bank (τ = 10 seconds) and the rectifier basic load resistors (4 x 120 Ω in parallel giving τ = 0.3 seconds).
b) Maintenance

Should any work be carried out on the heavy current circuitry of the rectifier the following security measures must be taken.

i) 18 kV switched off

ii) The circuit breaker in the 6 kV cubicle opened and the earthing switch closed. This earths the input 6 kV from the stepping transformer.

iii) The earthing cables (Nyffenegger) fitted to the 6 kV terminals of both rectifier transformers (rear of the units).

iv) The earthing cable (Nyffenegger) fitted to short out the condenser bank in the D.C. Filter unit. The terminals are accessible from the front of the unit.
6. **Trouble Shooting**

Faults and possible sources.

<table>
<thead>
<tr>
<th>Faults</th>
<th>Reason</th>
<th>Source</th>
</tr>
</thead>
<tbody>
<tr>
<td>18 kV cannot be switched on</td>
<td></td>
<td>i) Displayed Fault</td>
</tr>
<tr>
<td></td>
<td></td>
<td>ii) If no fault displayed then</td>
</tr>
<tr>
<td></td>
<td></td>
<td>18 kV ON and OFF relays or stepping</td>
</tr>
<tr>
<td></td>
<td></td>
<td>transformer &quot;motor driving&quot; contact not</td>
</tr>
<tr>
<td></td>
<td></td>
<td>making. To eliminate latter change</td>
</tr>
<tr>
<td></td>
<td></td>
<td>position and then return again.</td>
</tr>
<tr>
<td>&quot;Amplifier Saturated&quot;</td>
<td>Control loop not operating</td>
<td>i) 18 kV OFF</td>
</tr>
<tr>
<td></td>
<td></td>
<td>ii) Load open circuit</td>
</tr>
<tr>
<td></td>
<td></td>
<td>iii) D.C.C.T. transformer fuse blown</td>
</tr>
<tr>
<td></td>
<td></td>
<td>iv) Open circuit in current measurement</td>
</tr>
<tr>
<td></td>
<td></td>
<td>v) Insufficient voltage available. Too low</td>
</tr>
<tr>
<td></td>
<td></td>
<td>position of stepping transformer</td>
</tr>
<tr>
<td></td>
<td></td>
<td>vi) Oscillation. Too high position of</td>
</tr>
<tr>
<td></td>
<td></td>
<td>stepping transformer</td>
</tr>
<tr>
<td>Fault</td>
<td>Reason</td>
<td>Source</td>
</tr>
<tr>
<td>-----------------------------</td>
<td>--------------------------------------------------</td>
<td>--------------------------------------------------</td>
</tr>
<tr>
<td>&quot;Current Balance&quot;</td>
<td>Imbalance of bridge currents</td>
<td>i) Oscillation</td>
</tr>
<tr>
<td></td>
<td></td>
<td>ii) Control loop saturated</td>
</tr>
<tr>
<td></td>
<td></td>
<td>(see under amplifier saturated)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>iii) Gate pulse missing</td>
</tr>
<tr>
<td></td>
<td></td>
<td>iv) Fault in current balance</td>
</tr>
<tr>
<td></td>
<td></td>
<td>measurement card (U-4070)</td>
</tr>
<tr>
<td>&quot;Gate Pulse Short&quot;</td>
<td>Output transistor in Gate Control</td>
<td>Transistor died on output stage unit (U-4048)</td>
</tr>
<tr>
<td></td>
<td>Set short circuit</td>
<td></td>
</tr>
<tr>
<td>&quot;Overcurrent&quot;</td>
<td>Thermal overcurrent protection (Siemens Relay)</td>
<td>Overcurrent due to short circuit or current &gt;6KA</td>
</tr>
<tr>
<td>1&gt;</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1&gt;&gt;</td>
<td>Electromagnetic overcurrent protection (Seimens Relays)</td>
<td>Overcurrent due to short circuit (I&gt;15KA)</td>
</tr>
<tr>
<td>&quot;Current Balance cannot be cancelled with 18 KV switched on.&quot;</td>
<td>Thyristor short circuit.</td>
<td></td>
</tr>
<tr>
<td>Distribution (open)</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
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TRANSFORMER TYPE NGDT-6000-TF-400/2000 (Miebach)

(300GeV Magnet Test Supply)

Fig. 6

Primary voltage 6 kV. (line)

Primary 'A'

U V W (U) (V) (W)

Primary 'B'

Primary voltage 6 kV. (line)

SECONDARY 'A'

SECONDARY 'B'

U = 175 V.

Iw5A = 816 A. rms.

U = 303 V.

Iw5B = 0.470 A. rms.

Iw = 24 Amps rms.

Iw = 24 Amps rms.
U, V, W, = 6 kV. after stepping transformer

* The voltages shown in brackets are the secondary voltages of the 'B' rectifier transformer

Fig. 7 PHASE DIAGRAM FOR TRANSFORMER
NGDT-6000-TF-400/2000
(300 GeV Magnet Test Supply)
From Rectifier Transformers

600 volts

URG 1000 A (FERRAZ)

C R

Th4

Twisted

C R

Th6

ZKB 443/03 0 (VAC)

Common

C R

Th2

Basic load resistor

(120 ohm 2 kW)

AMP. Connectors

Pulse 1

Pulse 2

Pulse 3

Pulse 4

Pulse 5

Pulse 6

Common

Fig. 8 THYRISTOR BRIDGE

126-3958-4
**Fig. 9**

**D.C. FILTER**

Diagram showing a DC filter circuit with components labeled as follows:
- Rectifier:
  - Current: 5000 A
  - Inductor: L = 200 µH
- From Rectifier:
  - Resistor: R_D = 0.28 Ω
  - Capacitor: C_2 = 10 mF
- To Magnets:
  - Resistor: R = 1 kΩ
  - Capacitor: C_1 = 1 mF
  - Fuse (400A)
Fig. 10 WAVEFORMS OF GATE CONTROL SET
Fig. 11  PHASE RELATIONSHIPS OF GATE CONTROL SET
Fig. 12  FREE-WHEELING THYRISTOR PULSES
Fig. 13  RATE LIMITER OUTPUT
Fig. 14  BODE DIAGRAM OF CONTROL LOOPS
Fig. 16  18 kV CIRCUIT BREAKER LOGIC
Stepping Transformer

Protection Terminal Strip

- $e_1(2) =$ Bucholz
- $e_2 =$ Thermostat 1
- $e_3 =$ Thermostat 2
- $f_{1,3} =$ Fuse contacts

18 kV cell.

RL1 = Bucholz ‘declenchement’
RL2 = Bucholz ‘signalisation’
RL3 = Thermostat 1 ‘signalisation’
RL4 = Thermostat 2 ‘declenchement’

Fig. 17 STEPPING TRANSFORMER PROTECTION
Fig. 18  OVERCURRENT PROTECTION  (U1-4071)
Fig. 19  FREE-WHEELING  THYRISTOR  $\Delta \varphi$

AND  BLOCKING
Fig. 20  STEPPING TRANSFORMER CONTROL
SWITCH "ON"
380 VOLTS TO SUPPLY
(6kV UNIT)

RESET MAGNET and P.S. FAULTS

O.K.

SELECT STEPPING TRANSF. POSITION

SELECT COMPUTER LOCAL

SWITCH "ON" 18 kV

PUSH "START" BUTTON

SET UP REQUIRED CURRENT PROGRAM

SWITCH "ON" 18 kV

PUSH "START" BUTTON

Fig. 21 SWITCHING "ON" INSTRUCTIONS