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MILESTONE REPORT

DESIGN AND TEST OF ASICs AND READOUT BOARD PROTOTYPE FOR THE TEST INFRASTRUCTURE

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**Abstract:**

For very compact tungsten based forward calorimeters very thin detector modules, comprising thin sensor module and thin readout board, are needed. To build a thin readout board dedicated low-power readout ASICs, performing the requested signal processing from a sensor and including all necessary interfaces, are needed. Prototype ASICs fulfilling the specifications for a very compact calorimeter have been designed, fabricated and tested, together with readout boards needed for these tests. This milestone report describes the accomplishment of the above goal.
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<thead>
<tr>
<th></th>
<th>Name</th>
<th>Partner</th>
<th>Date</th>
</tr>
</thead>
<tbody>
<tr>
<td>Authored by</td>
<td>M. Idzik</td>
<td>AGH-UST</td>
<td>02/04/17</td>
</tr>
<tr>
<td>Edited by</td>
<td>M. Idzik</td>
<td>AGH-UST</td>
<td>04/04/17</td>
</tr>
<tr>
<td>Reviewed by</td>
<td>R. Pöschl, WP Coordinator</td>
<td>CNRS-LAL</td>
<td>19/04/17</td>
</tr>
<tr>
<td></td>
<td>F. Simon, WP Coordinator</td>
<td>MPG-MPP</td>
<td></td>
</tr>
<tr>
<td></td>
<td>F. Sefkow, Scientific Coordinator</td>
<td>DESY</td>
<td></td>
</tr>
<tr>
<td>Approved by</td>
<td>F. Sefkow, Scientific Coordinator</td>
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Executive summary

For very compact forward calorimeters, as will be used e.g. for luminosity measurements at linear colliders, a dedicated readout ASIC together with a readout board and a FPGA-based acquisition system are being developed. To fulfil the specifications the ASIC should consume very low power and should have a novel SoC architecture with all necessary functionalities implemented.

Within this work two prototype ASICs featuring two critical readout functionalities were developed and successfully tested. The FLAME0 is an 8-channel ASIC with analogue front-end and a 10-bit ultra low power ADC in each channel. The serialiser ASIC performs very high-speed (~5Gbps) serialisation and data transmission. To test the ASIC prototypes dedicated readout boards were designed and fabricated, and a FPGA-based data acquisition system was developed. The developed test setup was fully verified and the performed tests showed that both ASICs show the expected performance, in terms of pulse shape, peaking time, gain, noise, linearity, transmission speed, and power consumption. The developed prototypes will be merged into the final 16-channel FLAME readout ASIC, which will be a central part of the deliverable D14.4.

1. INTRODUCTION

The work described in this report is aimed at developing a dedicated, novel architecture, readout ASIC for very compact forward calorimeter. For the individual detector modules complex ASICs, with SoC architecture are necessary. The highly integrated electronics is thus a key part of a sandwich calorimeter with small Molière Radius that will be a main delivery of one of WP14 tasks, namely “Infrastructure for very compact tungsten based calorimetry”. The infrastructure provides a realistic integration environment for prototypes of luminosity detectors at future e+e- colliders. In this infrastructure, e.g. different sensor types meeting different conditions of radiation levels such as silicon or GaAs could be tested.

2. DESIGN OF FLAME READOUT ASIC

The development of the ASIC, called FLAME (FcaL Asic for Multiplane rEadout) has been started in CMOS 130 nm process. The complete FLAME ASIC will contain 16 channels with front-end and 10-bit ADC, fast serialisation and data transmission, plus all necessary functionalities and interfaces. A block diagram of the ASIC is shown in Figure 1.

![Fig. 1 Block diagram of FLAME ASIC.](image-url)
2.1. FLAME0 ASIC

The prototype ASIC, called FLAME0, contains 8 complete channels. A schematic diagram of a single channel is shown in Figure 2. Each channel contains a charge preamplifier with variable gain, a differential CR-RC shaper with a peaking time of 50 ns, and an ultra-low power 10-bit ADC with variable sampling frequency up to 40 MSps. The front-end electronics is required to handle sensor capacitances up to 50 pF. It was simulated that the ENC (Equivalent Noise Charge) is about 900 electrons for a 20 pF sensor. The simulated power consumption per channel is below 2 mW.

![Prototype FLAME channel schematic](image)

*Fig. 2 Schematic diagram of single FLAME channel.*

In addition to the 8 channels with front-end and ADC the FLAME0 chip contains back-end electronics and interfaces allowing for serialising and transmitting the data.

The layout of the complete FLAME0 ASIC, submitted to fabrication, is shown in Figure 3.
2.2. SERIALISER ASIC

The block diagram of the prototype ASIC is shown in Figure 4. It contains an ultra-low power fast serialiser, a fast SST output driver, and a test-data generator. The serialisation performs 22-bit to 1-bit operation. A critical block of the serialiser is an ultra-low power multi-phase PLL. According to simulations the power consumption of the complete ASIC is about 20 mW at 10Gbps.
The layout of complete serialiser ASIC is shown in Figure 5.

![Fig. 5 Layout of Serialiser ASIC.](image)

### 3. MEASUREMENT RESULTS

#### 3.1. TEST SETUP

To perform tests of the FLAME0 and Serialiser ASIC prototypes, dedicated test setups and readout boards are needed. A block diagram of the developed test setup is shown in Figure 6.
The test setup contains: a) a readout board for the DUT, b) a so-called uASIC board that delivers all necessary biases, fast data links, and monitoring circuitry and c) a FPGA-based evaluation board that receives digital data from the DUT, processes them and sends them to the host PC. A dedicated readout board designed for FLAME0 together with uASIC board is shown in Figure 7.

During the tests, the digital data from FLAME0 were sent through the uASIC board to the FPGA-based evaluation board at a rate of a few hundred Mbps. In the final setup, with real detector data, a much faster data rate of a few Gbps will be used. In this case, the uASIC board will not be used any longer but the data from the FLAME ASIC will be sent serially directly to high-speed receiver links of the FPGA-based evaluation board. Prototypes of XILINX evaluation boards (Artix 7) containing high-speed (~6.6Gbps) serial links are already available and the firmware for the first transmission tests has been written and verified.
3.2. TEST RESULTS

3.2.1. FLAME0 ASIC results

A number of FLAME0 tests was performed. First, the basic functionality of the complete front-end and ADC channels were successfully validated. In the next step detailed measurements of parameters like pulse shape, peaking time, gain, linearity, and noise, were carried out. As an example Figure 8 shows the pulse shapes at the front-end output for different sensor capacitances, obtained with the highest gain.

![Figure 8: Pulse shapes at the front-end of the FLAME0 ASIC for different sensor capacitances.](image)

The ASIC response features the expected semi-Gaussian pulse shape with amplitude and peaking time changing slightly with sensor capacitance. The measurement was repeated for all (four) possible gain setting. The noise ENC was determined to be (for highest gain) about 850 electrons at 20 pF sensor capacitance, fulfilling the specifications. Finally, the sampled signal was measured at the ADC output confirming thus the expected ASIC functionality.
3.2.2. Serialiser ASIC results
First serialiser tests used the internal pattern generator for measuring the so-called “Eye diagram” of the output signal. The result obtained at 5Gbps rate is shown in Figure 9.

![Eye diagram obtained at 5Gbps.](image)

The opening of the “eye” is large enough for signal transmission. The quantitative measurement of the BER needs to be still done.

4. CONCLUSIONS
The prototype readout ASICs for very compact forward calorimeters have been designed, fabricated and tested. To obtain these goals dedicated readout boards for the ASICs, plus an additional uASIC board for the test setup were also designed and produced. For the data acquisition, a XILINX-based FPGA evaluation board, with a dedicated firmware, was used. With this complex test setup two prototype ASICs, the 8-channel FLAME0 ASIC and a fast serialiser ASIC, were found fully functional, confirming the advantages of the adopted architecture and proving that the milestone described in this report was achieved. The milestone will allow for providing the infrastructure for tests highly compact calorimeters that constitutes the deliverable D14.4 in Month 48.

5. ANNEX: GLOSSARY

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<th>Definition</th>
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<tbody>
<tr>
<td>ADC</td>
<td>Analog to Digital Converter</td>
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<tr>
<td>ASIC</td>
<td>Application Specific Integrated Circuit</td>
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<tr>
<td>BER</td>
<td>Bit Error Rate</td>
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<tr>
<td>CMOS</td>
<td>Complementary Metal-Oxide-Semiconductor</td>
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<tr>
<td>DUT</td>
<td>Device Under Test</td>
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<tr>
<td>ENC</td>
<td>Equivalent Noise Charge</td>
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<tr>
<td>FPGA</td>
<td>Field Programmable Gate Array</td>
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<tr>
<td>PLL</td>
<td>Phase Locked Loop</td>
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<tr>
<td>SoC</td>
<td>System on Chip</td>
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