ATLAS
LAr Calorimeter Phase-II Upgrade
Technical Design Report
Abstract

This Technical Design Report documents plans to upgrade the Liquid Argon calorimeters’ readout electronics for the ATLAS experiment for operation at the High Luminosity LHC. When the High Luminosity LHC begins operations in 2026 it will be able to reach a peak instantaneous luminosity of $7.5 \times 10^{34} \text{cm}^{-2}\text{s}^{-1}$, which corresponds to approximately 200 inelastic proton-proton collisions per beam crossing. The new Liquid Argon readout electronics will be operational for more than ten years, during which time the LHC is expected to deliver $4000 \text{fb}^{-1}$ of proton-proton collision data. These requirements are a significant challenge in the design of the new readout system. The design, construction and expected performance of the future readout electronics are presented in detail. These include the results of measurements of prototypes and the plans for their mass production. This document also describes the management of the project, its schedule and major milestones. The costs of the new readout electronics and the collaboration that plans to build it are also presented.
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Part I

Motivation
1 Introduction

This Technical Design Report details the technical implementation of the ATLAS Liquid Argon (LAr) calorimeter Phase-II upgrade project. The project is proposed to maintain and enhance the physics reach of the experiment following the high luminosity upgrades to the Large Hadron Collider (LHC), foreseen to be completed in 2026. The scope of the project is to design and build an entirely new readout electronics system, and to install it during the third long shutdown (LS3) of the LHC, which begins in 2024. The ATLAS Phase-II Scoping Document [1] provides a general overview of the Phase-II plans.

At the High Luminosity LHC (HL-LHC) instantaneous luminosities up to $7.5 \times 10^{34}$ cm$^{-2}$ s$^{-1}$ are expected, with the goal of providing an integrated luminosity of 4000 fb$^{-1}$ after a period of about 12 years. Prior to LS3, the second long shutdown (LS2) in 2019–2020 also provides an opportunity to upgrade the detector. During this period, the Phase-I [2–4] upgrades of the ATLAS detector will take place.

The objective of the LAr Phase-II upgrade is to replace the LAr readout electronics and the low-voltage powering system due to the limited radiation tolerance of certain currently installed front-end components. The LAr calorimeters themselves are expected to operate reliably during the HL-LHC period, even though a signal degradation is expected in the forward calorimeters, as described in Section 2.5. Furthermore, at the expected maximum instantaneous luminosity of the HL-LHC, the high energy and particle densities (particularly in the forward region) will challenge the trigger system due to the large number of interactions per bunch crossing, or “pileup”. The ATLAS trigger system will therefore be upgraded, making the present LAr readout electronics incompatible with the future ATLAS trigger scheme [5, 6]. Due to both the limited radiation tolerance and the incompatibility with the proposed trigger system, the existing readout electronics will have to be replaced completely.

The proposed upgrade will take advantage of the technological progress made since the original construction, to implement a more flexible readout architecture. This new flexibility will be exploited to make the full calorimeter granularity and longitudinal shower information available to the lowest level trigger processors. This will allow ATLAS to deploy more sophisticated trigger algorithms enhancing the selection of events, which in turn will enhance the ability to measure the properties of the Higgs boson, improve the measurements of other Standard Model (SM) processes, and extend the potential for discovery of physics beyond the SM.
1.1 LHC roadmap

The scientific programme of the LHC spans the next 20 years and includes an ambitious series of upgrades that will ultimately result in an accumulated integrated luminosity for proton–proton collisions of 4000 fb$^{-1}$. This represents more than an order of magnitude more data than that which will be collected prior to the HL-LHC run. The improvements necessary to achieve this accelerator performance will be realized during two long shutdowns, each of two to three years duration. The last of these, LS3, starting at the end of 2023, will include major performance upgrades of the accelerator for the HL-LHC, as shown in Figure 1.1 and described in the HL-LHC Technical Design Report [7].

Figure 1.1: The LHC and HL-LHC baseline plan for the next decade and beyond, showing the energy of the collisions (upper red line) and luminosity (lower green lines). The cumulative integrated luminosity at the end of each period is also indicated.

The LHC roadmap, including the already completed first shutdown as well as the ongoing run, is outlined below in more detail:

- **Long Shutdown 1 (LS1): 2013–2014.** This shutdown was used to consolidate machine elements (repairing the magnet splices and upgrading the collimation scheme) in order to achieve the design luminosity and increase the beam energy.
- **Run 2: 2015–2018.** The LHC began colliding beams at $\sqrt{s} = 13$ TeV in 2015, and has exceeded the design peak luminosity of $L = 10^{34}$ cm$^{-2}$ s$^{-1}$. An integrated luminosity of approximately 120 fb$^{-1}$ per experiment is expected to be delivered to ATLAS and CMS during the four years of Run 2.
- **Long Shutdown 2 (LS2): 2019–2020.** The Linac4 will be connected into the injector complex, and the injection beam energy of the Proton Synchrotron Booster will be upgraded in order to reduce the beam emittance. New cryogenic plants will be installed to separate the cooling of the superconducting radio frequency modules and the magnet cooling circuit.
- **Run 3: 2021–2023.** The LHC design parameters should allow for an ultimate peak instantaneous luminosity of $L \sim 2.2 \times 10^{34}$ cm$^{-2}$ s$^{-1}$ (Phase-I operation) and for delivering an integrated luminosity of approximately 300 fb$^{-1}$ by the end of Run 3. The
LHC is expected to reach its design beam energy and provide proton–proton collisions at $\sqrt{s} = 14\text{ TeV}$.

- **Long Shutdown 3 (LS3): 2024–2026.** The LHC will undergo a major upgrade of its components (e.g. low-$\beta$ quadrupole triplets, crab cavities at the interaction regions).

- **HL-LHC: 2026–2037 and beyond.** The LHC complex will deliver Levelled instantaneous luminosity $L = 5–7.5 \times 10^{34}\text{ cm}^{-2}\text{ s}^{-1}$ (Phase-II operation) and an annual integrated luminosity of 250 to 320 fb$^{-1}$, i.e. up to approximately 4 000 fb$^{-1}$ after 12 years of running.

### 1.2 ATLAS upgrade plan

To optimize the physics reach at the HL-LHC, ATLAS is following a staged programme in three phases, corresponding to the three long shutdowns.

The upgrades during LS1 consisted of consolidation of the existing sub-detectors including the installation of a fourth (inner) layer for the pixel detector requiring a new, smaller radius central beryllium beam pipe, additional chambers in the muon spectrometer to improve the geometrical coverage, more neutron shielding in the muon endcap toroids, as well as a new Level-1 topological trigger processor and a fast track trigger at the input of the Level-2 trigger system.

After LS2, instantaneous luminosities of $L \sim 2.2 \times 10^{34}\text{ cm}^{-2}\text{ s}^{-1}$ are expected with 25 ns bunch spacing and the average number of interactions per crossing will be $\langle \mu \rangle \sim 60$. In order for ATLAS to exploit this increase in luminosity and maintain a low-$p_T$ lepton threshold (approximately 25 GeV) in the Level-1 trigger while keeping the same trigger bandwidth (100 kHz), the development of new detector and readout components is needed [2]. This is the primary motivation of the Phase-I detector upgrades, which include the replacement of chambers in the forward muon spectrometer, the upgrade of the calorimeter trigger electronics and the installation of new Level-1 trigger processors. The performance requirements and design specifications of each upgrade component are defined for $L = 3 \times 10^{34}\text{ cm}^{-2}\text{ s}^{-1}$ and $\langle \mu \rangle = 80$ interactions per bunch crossing, to allow some margin in case of further improvements in the LHC peak instantaneous luminosity.

The Phase-II upgrades [1] for the HL-LHC run are motivated by the ageing of the inner tracker (primarily because of radiation exposure), by the increased occupancy of the detector systems and data volumes that would saturate the readout links, by the obsolescence of some of the detector sub-system electronics, and by additional requirements that the trigger system will impose on the detector readout in order to cope with the expected luminosity during the HL-LHC era ($5$ to $7.5 \times 10^{34}\text{ cm}^{-2}\text{ s}^{-1}$ with $\langle \mu \rangle = 140$ to 200 interactions per bunch crossing). Specifications of each upgrade component are therefore defined for up to $\langle \mu \rangle = 200$ interactions per bunch crossing$^1$.

$^1$ The average number of interactions per bunch crossing values are calculated using the formula
1.3 Outline of this report

This report will first present an overview of the LAr calorimeter system up to Phase-I (Chapter 2), followed by a discussion of the requirements (Chapter 3) and expected performance (Chapter 4) of the calorimeter electronics upgraded for Phase-II. In the subsequent chapters the implementation of these upgrades is discussed, beginning with an abbreviated summary in Chapter 5 of the technical chapters 6 to 11 that follow. The technical chapters discuss the upgrades in more detail, starting with the calibration system (Chapter 6) and front-end electronics (Chapter 7), then the off-detector electronics (Chapter 8), and finally the power supplies (Chapter 9) and control system (Chapter 10). The report concludes with a discussion of the installation and commissioning (Chapter 11) and an overview of the project organization (Chapter 12).

\[ \langle \mu \rangle = \mathcal{L} \times \sigma_{\text{inel}} / n_b \times f_{\text{rev}}, \] where the total inelastic proton–proton cross section is assumed to be \( \sigma_{\text{inel}} = 85 \text{ mb} \) at \( \sqrt{s} = 14 \text{ TeV} \), the LHC revolution frequency is \( f_{\text{rev}} = 11.245 \text{ kHz} \), and \( n_b \) is the number of colliding bunches at IP1. A benchmark scenario with a \( \langle \mu \rangle \) of approximately 200 is obtained by assuming \( n_b = 2808 \) and a peak instantaneous luminosity of \( \mathcal{L} = 7.5 \times 10^{34} \text{ cm}^{-2} \text{s}^{-1} \). For more details, see the HL-LHC Technical Design Report [7].

Chapter 1: Introduction
2 System Overview

The ATLAS detector [8] is one of the two large general-purpose experiments designed to study proton–proton (pp) as well as heavy-ion collisions at the LHC. The detector is situated in an underground experimental cavern at Point-1 near the CERN main site. This chapter provides a brief overview of the existing ATLAS detector in Section 2.1, followed by a description of the LAr calorimeter system in Section 2.2. The current readout electronics chain, including the on-detector, off-detector, and trigger electronics, are discussed in Section 2.3. An overview of the system, as will be after the planned Phase-I electronics upgrade, is presented in Section 2.4. Finally, in Section 2.5, the radiation tolerance and the performance of the LAr calorimeters at the HL-LHC are discussed.

2.1 Current ATLAS detector

The present ATLAS detector covers approximately 99% of the entire solid angle around the collision point and successively consists of an inner tracking detector (ID) surrounded by a thin superconducting solenoid, electromagnetic (EM) and hadronic calorimeters, and a muon spectrometer incorporating three large toroidal magnet systems.

The ATLAS calorimeter system covers the pseudorapidity $|\eta| < 4.9$ and provides energy measurements of particles. Sampling calorimeters based on Liquid Argon (LAr) technology are used for the detection of EM objects such as electrons and photons up to $|\eta| = 3.2$, as well as hadronic objects in the $|\eta| > 1.5$ to 4.9. Hadronic calorimetry within $|\eta| < 1.7$ is provided by a steel/scintillator-tile calorimeter (TileCal).

2.2 The ATLAS LAr calorimeter system

In ATLAS, precision EM calorimetry is provided by barrel ($|\eta| < 1.475$) and endcap ($1.375 < |\eta| < 3.2$) accordion geometry lead/LAr sampling calorimeters. An additional

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1 ATLAS uses a right-handed coordinate system with its origin at the nominal interaction point (IP) in the centre of the detector and the z-axis along the beam pipe. The x-axis points from the IP to the centre of the LHC ring, and the y-axis points upward. Cylindrical coordinates $(r, \phi)$ are used in the transverse plane, $\phi$ being the azimuthal angle around the z-axis. The pseudorapidity is defined in terms of the polar angle $\theta$ as $\eta = -\ln \tan(\theta/2)$. In ATLAS, the so-called “side-A” refers to positive $z$-values while “side-C” refers to the negative side.
thin LAr presampler covering $|\eta| < 1.8$ allows corrections for energy losses in material upstream of the EM calorimeters. The EM barrel (EMB) calorimeter [9] consists of two half-barrels housed in the same cryostat. The EMB shares the cryostat with the superconducting solenoid. The EM endcap (EMEC) calorimeter [10] comprises two wheels, one on each side of the EM barrel. The wheels are contained in independent endcap cryostats together with the hadronic endcap [11] (HEC) and forward calorimeters [12] (FCal). The wheels themselves consist of two co-axial wheels, with the outer wheel (OW) covering the region $1.375 < |\eta| < 2.5$ and the inner wheel (IW) covering the region $2.5 < |\eta| < 3.2$. The HEC is a copper/LAr calorimeter providing hadronic coverage in the region $1.5 < |\eta| < 3.2$ and consists of two independent wheels which combined provide 4 longitudinal calorimeter layers. Finally, the FCal provides coverage over $3.1 < |\eta| < 4.9$. Three cylindrical modules comprise the FCal, arranged sequentially; the module closest to the interaction point (FCal1) is optimized for EM measurements and uses copper as absorber, while the two subsequent modules (FCal2 and FCal3) are made mainly of tungsten and are optimized for hadronic measurements.

Figure 2.1: The ATLAS Liquid Argon calorimeter system.

The EM calorimeters are comprised of accordion-shaped copper-kapton electrodes positioned between lead absorber plates and kept in position by honeycomb spacers while the system is immersed in LAr (Figure 2.2). The HEC uses a parallel plate geometry. In order to withstand the high particle fluxes in the forward region, the FCal is based on a design that uses cylindrical electrodes consisting of rods positioned concentrically inside tubes parallel to the beam axis, supported by a metal matrix. Very narrow LAr gaps have been chosen for the FCal to mitigate ion buildup at high rates and the gap is kept constant with a winding radiation hard fibre wrapped around the rods.

For most of the EM calorimeter (EMB and EMEC-OW) each module has three layers in depth with different cell granularities, as can be seen in Figure 2.3, while each EMEC-IW module
has only two layers. The cell segmentation in depth and $\eta$ is obtained by etching on the electrodes. The $\phi$ segmentation is achieved by ganging together the appropriate number of electrodes. Incident particles shower in the absorber material and subsequently the LAr is ionized. Under the influence of the electric field between the grounded absorber and the electrode which are kept at a high-voltage (HV) potential, the ions and electrons drift, the latter inducing a triangular pulse (Figure 2.4) on the electrodes. In the EMB, for example, the size of the drift gap on each side of the electrode is 2.1 mm, which corresponds to a total electron drift time [13] of approximately 450 ns for a nominal operating voltage of 2 000 V. In the EMEC, the gap is a function of radius and therefore the HV varies with $\eta$ to provide a uniform detector response. In order to operate normally close to the LHC beamline and mitigate ion buildup, in a region of high particle flux, the FCal employs LAr gaps that are much narrower than those used for the other LAr calorimeter subsystems, 270, 375, and 500 $\mu$m in FCal1, FCal2, and FCal3, respectively.

The induced pulse height is proportional to the energy deposited in each calorimeter cell, while the pulse peaking time can be used to measure the arrival time of the incident particle. The EM calorimeter is designed such that the largest fraction of the energy is collected in the middle layer while the back layer collects only the tail of the EM shower. Using the energy measurement and the positions of all cells in all layers of the calorimeter contained in the shower, the incident particle energy can be reconstructed and, taking advantage of the fine segmentation of the front layer, its direction and characteristics can be inferred. As discussed later, the fine segmentation is extremely useful in the discrimination between photons and jets with a leading $\pi^0$ meson, which primarily decays to two photons. In addition, with its pointing geometry, the calorimeter can reconstruct the direction of neutral particles, such as unconverted photons, for which semiconductor tracking cannot be used [14]. The arrival time of the particle is determined by the time measurement of the most energetic cell in the middle layer.

### 2.3 Existing LAr readout electronics

The current LAr readout electronics system is designed to record energies in a range from about 50 MeV to approximately 3 TeV for a total of 182,468 channels and with a required energy resolution of $\sigma_E/E = 10\%/\sqrt{E} \pm 0.7\%$ out to $|\eta| < 3.2$. The system applies shaping to the current signals, samples them at 40 MHz and sends digitized samples for each bunch crossing upon a Level-1 (L1) trigger accept. In Run 1, five samples were transmitted with a maximum L1 trigger rate of 75 kHz. For the ongoing Run 2, four samples are transmitted and the system is operating at L1 trigger rates up to 110 kHz.

An overview of the readout architecture is depicted in Figure 2.5. It is comprised of two main components: Front-End (FE) electronics placed on the detector and Back-End (BE) electronics located off the detector in the USA15 counting room. The system has been in operation almost continuously and extremely reliably since its installation in 2006. Maintenance
Figure 2.2: Accordion structure of the EMB. The top figure is a view of a small sector of the barrel calorimeter in a plane transverse to the LHC beams.

Figure 2.3: Sketch of an EMB module where the different layers are visible. The granularity in $\eta$ and $\phi$ of the cells of each of the three layers and of the trigger towers is also shown.
operations have taken place during end-of-year shutdowns and during LS1 when access to the FE electronics was possible.

2.3.1 On-detector front-end electronics

Due to the stringent performance requirements on the LAr electronics, the FE electronics are mounted directly on the LAr cryostats, in the gap between the barrel and endcap calorimeters and on the outer face of the end cap cryostats. These areas have limited access and require radiation tolerant electronics components. The on-detector electronics have been qualified, in terms of radiation tolerance, for up to 10 years of operation at the LHC, i.e. equivalent to an integrated luminosity in the range of 700 to 1 000 fb\(^{-1}\) [15].

The FE electronics are housed in 58 FE crates. As shown in Figure 2.5, each FE crate contains:

**Readout Front-End Boards (FEBs):** These are the main elements in the FE electronics and are designed to read out and digitize the LAr calorimeter signals without degrading the energy resolution. Analog signals are summed on Layer Sum Boards (LSBs). Each FEB is a large (approximately 0.5 m × 0.5 m), dense, 10-layer PCB that processes the signals from up to 128 channels in a specific layer of the calorimeter.
Figure 2.5: The schematic block diagram of the current LAr readout electronics architecture. The LAr ionization signal proceeds upwards, through the FE crates mounted on the detector to the BE electronics in the USA15 counting room. This diagram is valid for the EM calorimeters; slight changes would be needed to describe the HEC and FCal which include additional electronics inside the endcap cryostat.
**Tower Builder Boards (TBBs):** Analog signal sums\(^2\) are sent over a dedicated backplane in the FE crate to the TBB, which forms trigger towers with a granularity of \(\Delta \eta \times \Delta \phi = 0.1 \times 0.1\). The corresponding signals are sent over analog cables to the L1 calorimeter trigger system receivers.

**Calibration Boards:** The calibration boards deliver an electronic pulse with precisely known amplitude and whose shape is close to the calorimeter ionization signal. The readout electronics are inter-calibrated to better than 0.25%.

**Controller Boards:** The controller boards receive and distribute the 40 MHz LHC clock as well as other configuration and control signals.

On the FEB, the detector signals are first subject to several stages of analog processing. Preamplifier hybrids amplify the raw signals; three versions match the subdetector capacitances and dynamic ranges. Although 97% of the preamplifiers are on the FEBs, the HEC has cryogenic preamplifier summing boards mounted on the detector inside the endcap cryostat. In the case of the FCal, summing boards mounted on the rear of the HEC, also inside the endcap cryostat, serve to perform signal summing, as well as to distribute the HV through a protection resistor which limits the current in case of a spark or short in an electrode. For the HEC, the preamplifiers on the FEBs are replaced by preshapers that invert, amplify, and shape the signal. The signals are then split and further amplified by shaper chips to produce three overlapping linear gain scales, with gain ratios of about 10. Gain selector chips choose the gain for each channel based on the peak sampled value of each signal. Fast bipolar shaping is performed with a time constant \(\tau = RC = 13\) ns. The shaped signals are then sampled at the LHC bunch crossing frequency of 40 MHz by switched capacitor array analog pipeline chips. Figure 2.4 shows the triangular pulse shape from the detector along with the shaped and sampled signal pulse shape. For events accepted by the L1 trigger, typically four (Run 2) or five (Run 1) samples per channel are read out from the switched capacitor array using the optimal gain scale, and digitized using a 12-bit analog-to-digital converter (ADC). The digitized data are formatted, multiplexed, serialized, and then transmitted via a 1.6 Gbps fibre optic link off the detector to the BE electronics.

Throughout this report, the term “front-end electronics” generally refers to the more easily accessible “warm” electronics mounted on the detector, outside the LAr. Unless otherwise noted, the term does not include the HEC and FCal “cold” electronics which are housed inside the endcap cryostat and which is not foreseen to be opened for the Phase-II upgrade.

### 2.3.2 Off-detector readout

The BE electronics perform digital filtering, formatting, and monitoring of the calorimeter signals. Each FE crate is associated to a VME-based Readout Driver (ROD) crate, which

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2 In the HEC and FCal, no further summation of signals is required, so Tower Driver Boards (TDBs) are used in place of TBBs.
Read Out Drivers (RODs) : The RODs synchronize the output of the FEBs with the L1 trigger and compute physical quantities such as the energy, time phase, and quality of the signal.

CPU Board : The CPU board is a VME processor that controls the ROD crate.

SPAC Master Board : A communication module to configure or load parameters into the various boards of the FE crate or to read back registers; configuration and monitoring take place using the Serial Protocol for ATLAS Calorimeters (SPAC).

Trigger and Busy Module (TBM) : The TBM receives the trigger, timing, and control (TTC) signals that include the 40 MHz LHC clock and other synchronous commands and provides back the busy state of the LAr readout electronics.

Each ROD receives raw data (digitized samples) from up to eight FEBs. Four input field programmable gate arrays (FPGAs) parallelize the incoming data and verify its integrity. The memory is separated into two banks: one for writing incoming data, the other for the data that is read by the digital signal processor (DSP). A ROD holds four Processing Units (PUs), each with two DSPs. Each DSP can perform $5.7 \times 10^9$ instructions per second, and the calculations have been optimized to accommodate the L1 trigger rate (for a rate of 110 kHz, the calculations must be performed within 9.1 µs). An optimal filtering (OF) algorithm [16] is used to calculate the energy deposited in the calorimeter from the digitized samples. For deposits above a given (programmable) energy threshold, the time of the energy deposition and the quality of the pulse are also calculated. The quality factor quantifies the agreement of the measured pulse shape with its expectation and can indicate whether the measured pulse is distorted. A second energy threshold is defined, above which the values of the raw samples are written out in addition to the results of the optimal filtering algorithm. These resulting quantities are then sent via optical fibres to the data acquisition (DAQ) system.

2.3.3 L1 trigger readout

The current Level-1 calorimeter (L1Calo) system receives analog, summed Trigger Tower signals from the LAr Tower Builder Boards described in Section 2.3.1, as well as equivalent signals from the TileCal. The architecture of the L1Calo system is illustrated in Figure 2.6.

Pre-processor Module (PPM) : The PPMs sample the analog Trigger Tower signals at 80 MHz, identify the bunch crossing using the pulse shape, and use an FPGA to compute the transverse energy. The digital data are then transmitted to the Cluster Processor Modules and Jet Energy Modules.
Cluster Processor Module (CPM) : Each CPM identifies isolated electron, photon and τ lepton candidates from the $\Delta \eta \times \Delta \phi = 0.1 \times 0.1$ granularity energy deposits in a given calorimeter region. A Region of Interest (ROI) is defined using a sliding window algorithm, and electromagnetic and hadronic isolation quantities are computed from the surrounding clusters.

Jet Energy Module (JEM) : Each JEM identifies energetic jet candidates from $\Delta \eta \times \Delta \phi = 0.2 \times 0.2$ jet elements in a given calorimeter region. Similar to in the CPM, a ROI is defined using a sliding window algorithm. The total transverse energy and the missing transverse energy are also computed.

Common Merger eXtended module (CMX) : The results from the CPMs and JEMs are transmitted over crate backplanes and summed in CMXs before being sent to the Central Trigger Processor (CTP). In addition, trigger objects for the whole $\eta$–$\phi$ range processed by L1Calo are transmitted optically by the CMX to the new topological trigger processor [4] (L1Topo), commissioned in Run 2, which also receives data from the Level-1 muon trigger system (L1Muon). L1Topo forms combined trigger objects, based on the full event topology, and transmits them to the CTP.

The CTP then combines the input of the L1Calo system with other trigger inputs. If an event is to be accepted, it issues a “Level-1 Accept”. After receiving a L1 Accept, the L1Calo modules provide readout data and ROIs to the High-Level Trigger (HLT) system via readout drivers.

2.4 LAr Phase-I electronics readout upgrade

The Phase-I upgrade is the first step in the readout electronics upgrades for the HL-LHC. This upgrade will provide higher-granularity, higher-resolution and longitudinal shower
information from the calorimeter to the L1 trigger system. The increase in granularity can be seen in Figure 2.7, which compares the energy deposition of an electron in the existing trigger readout system to that of the planned upgrade system. This upgrade improves the trigger energy resolution and efficiency for selecting electrons, photons, \( \tau \) leptons, jets, and missing transverse energy \( (E_T^{\text{miss}}) \), while enhancing discrimination against backgrounds and fakes in an environment with high instantaneous luminosity, i.e. with high pileup. As the LHC luminosity increases above the design value, the improved calorimeter trigger electronics will allow ATLAS to deploy more sophisticated algorithms already at the L1 trigger to restrict the L1 trigger rates to the maximum of 110 kHz supported by the current FE and BE electronics.

Figure 2.7: An electron (with 70 GeV of transverse energy) as seen by the existing L1 Calorimeter trigger electronics (a) and by the planned upgraded trigger electronics for Phase-I (b).

The existing calorimeter trigger information is based on the concept of a “Trigger Tower” that sums the energy deposition across the longitudinal layers of the calorimeters in an area of \( \Delta \eta \times \Delta \phi = 0.1 \times 0.1 \). The Trigger Tower is created through several stages of on-detector
Table 2.1: Comparison of the current Trigger Tower granularity vs. the planned Super Cell granularity in the LAr EM barrel calorimeter, in terms of both elementary cells and \( \Delta \eta \) and \( \Delta \phi \). The number of elementary cells grouped for the trigger readout in \( \eta \) and \( \phi \) are indicated by \( n_\eta \) and \( n_\phi \), respectively.

<table>
<thead>
<tr>
<th>Layer</th>
<th>Elementary Cell</th>
<th>Trigger Tower</th>
<th>Super Cell</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>( \Delta \eta \times \Delta \phi )</td>
<td>( n_\eta \times n_\phi )</td>
<td>( n_\eta \times n_\phi )</td>
</tr>
<tr>
<td>0</td>
<td>Presampler</td>
<td>( 0.025 \times 0.1 )</td>
<td>( 4 \times 1 )</td>
</tr>
<tr>
<td>1</td>
<td>Front</td>
<td>( 0.003125 \times 0.1 )</td>
<td>( 32 \times 1 )</td>
</tr>
<tr>
<td>2</td>
<td>Middle</td>
<td>( 0.025 \times 0.025 )</td>
<td>( 4 \times 4 )</td>
</tr>
<tr>
<td>3</td>
<td>Back</td>
<td>( 0.05 \times 0.025 )</td>
<td>( 2 \times 4 )</td>
</tr>
</tbody>
</table>

Figure 2.8: Geometrical representation in \( \eta, \phi \) space of an EM Trigger Tower in the current system, where the transverse energies in all four layers are summed (left) and of the Super Cells planned for the Phase-I upgrade, where the transverse energy in each layer is retained in addition to the finer granularity in the front and middle layers (right). Each square represents an area of size \( \Delta \eta \times \Delta \phi = 0.1 \times 0.1 \).

The new finer granularity scheme is based on so-called “Super Cells”, which provide information for each calorimeter layer for the full \( \eta \) range of the calorimeter, as well as finer segmentation (\( \Delta \eta \times \Delta \phi = 0.025 \times 0.1 \)) in the front and middle layers of the EMB and EMEC for \(|\eta| \leq 2.5\). This scheme is detailed for the EMB in Table 2.1 and is illustrated in Figures 2.7 and 2.8. A full description of the geometrical representation of the Super Cells planned for the entire calorimeter can be found in [2].

The architecture of the upgraded calorimeter trigger electronics is depicted in Figure 2.9, with the upgraded and new components outlined in red. The technical implementation of the upgraded front-end and back-end electronics is described in detail in the LAr Phase-I
upgrade TDR [2].

To provide high-granularity and high-precision information to upgraded trigger processors called Feature EXtractors (FEXs) [4], new LAr Trigger Digitizer Boards (LTDB) are installed in the available spare slots of the front-end crates. The upgrade of the layer sum boards and of the baseplanes allows the LTDBs to digitize information with granularity up to \( \Delta \eta \times \Delta \phi = 0.025 \times 0.1 \) in the front and middle layers of the EM calorimeters. The LTDB also recreates the \( 0.1 \times 0.1 \) analog sums and feeds them back to the TBB to maintain the “legacy” system fully operational. The TBBs will eventually be retired during LS3. The digitized signals are processed remotely by the LAr Digital Processing Blade (LDPB) modules, which convert the samples to calibrated energies in real-time and interface to the FEX processors.

![Schematic block diagram of the Phase-I upgrade LAr trigger readout architecture](image)

Figure 2.9: Schematic block diagram of the Phase-I upgrade LAr trigger readout architecture. The new components are indicated by the red outlines and arrows.

The scope of the ATLAS Phase-I upgrades is limited to a few sub-detectors only. The readout of most of the systems will remain unchanged, limiting the capability of extending some of the parameters of the L1 trigger system, such as the maximum rate and maximum latency.
The total latency is 44.2 bunch crossings (BCs). In addition, the FEX processors require 14 BCs to extract the trigger primitives and transmit them to the Topological Trigger processors. The overall 58.2 BC latency of the calorimeter trigger system is consistent with the maximum (65 BCs) value allowed at the input of the Topological Trigger processors where data from both the calorimeter and the muon trigger modules are combined.

The Phase-I upgrades provide better control of the trigger rates by improving the selectivity of EM and $\tau$ objects, the resolution of jets and $E_T^{\text{miss}}$ trigger signatures, and the discrimination power against background emerging from both the out-of-time and in-time pileup. Performance studies and impact on physics analyses are outlined in the LAr [2] and TDAQ [4] Phase-I TDRs.

The Phase-I upgrade accomplishes

1. Reduced jet backgrounds in the L1 EM trigger by deploying shower shape algorithms and high-precision isolation criteria for electron and photon identification.
2. Deployment of algorithms currently used in the HLT to improve $\tau$ identification at L1.
3. Improvement of L1 jet and $E_T^{\text{miss}}$ resolutions and efficiencies to effectively reduce the rates while retaining the same physics acceptance in the offline analyses.

These improvements are achieved by taking advantage of the higher $\eta$-granularity of the Super Cells compared to Trigger Towers, the layer segmentation, providing longitudinal shower information for the L1 trigger, and the higher digitization precision of the energy in the Super Cells. Ultimately the goal is to maintain the thresholds of single and multi-object L1 calorimeter triggers at values comparable to those used in Run 1, despite the increased centre-of-mass energy, potential instantaneous luminosity up to $\mathcal{L} = 3 \times 10^{34}$ cm$^{-2}$ s$^{-1}$, and pileup up to $\langle \mu \rangle = 80$. Following the Phase-I upgrade, the state of the LAr readout electronics will remain the same until the Phase-II upgrade begins.

2.5 Radiation tolerance and performance of the LAr calorimeters at the HL-LHC

The operation of the ATLAS LAr calorimeters in HL-LHC conditions would exceed the original design specifications which assumed 10 years of operation at nominal LHC luminosities up to $10^{34}$ cm$^{-2}$ s$^{-1}$ [15, 17]. The LTDB, which will have been installed for the LAr Phase-I upgrade, has been designed with the HL-LHC in mind and has been qualified for the expected luminosities at the HL-LHC [2]. The upgraded trigger electronics will therefore remain operational during Phase-II. One concern for operating the LAr calorimeters at the HL-LHC is the integrated luminosity and the corresponding radiation dose taken by the detector components. During the initial detector design [17] and in subsequent irradiation campaigns, possible poisoning of argon and radiation damage of organic detector materials, like kapton foil, connectors, cables, honeycomb spacers, G10 epoxy, printed circuit board (PCB) materials and PEEK fibres has been measured.
Poisoning of argon by introducing oxygen or organic compounds was tested for different parts of the EM calorimeter [18] up to neutron fluence of $2 \times 10^{14} \text{n}_{\text{eq}}/\text{cm}^2$. It was found that the contamination is mostly due to PCB materials (G10, FR4 and prepreg). Assuming a linear dependence on the radiation dose, a pulse height degradation below 3% is expected over the lifetime of the HL-LHC. This pulse degradation is in an acceptable range as it can be taken into account during the calibration. The liquid argon impurity is moreover monitored regularly [19], currently showing no dependence on accumulated luminosity. However, the radiation tolerance of the purity monitors themselves, which are installed inside the cryostat and therefore will not be accessible, will have to be verified.

Similar tests for HEC and FCal materials (kapton EST boards, FR4 strip lines, honeycomb, PEEK cables, etc.) have been performed for neutron fluence up to $1 \times 10^{16} \text{n}_{\text{eq}}/\text{cm}^2$ [20]. No pollution has been observed from either material or their combination. Possible neutron-induced outgassing from the tungsten alloy of FCal-2/3 slugs was also studied up to neutron fluence of $1.5 \times 10^{16} \text{n}_{\text{eq}}/\text{cm}^2$ [21]. The conclusion is that LAr will be contaminated by not more than 0.1 ppm of oxygen equivalent. Note that the results are conservative since this measurement was done at room temperature where outgassing rate is much higher than at LAr temperature.

Various components of the readout chain of the liquid argon calorimeters were exposed to high neutron fluences and gamma doses. The results are presented in the Liquid Argon Calorimeter TDR [17] and in a detailed report available in Reference [22]. Peeling tests of copper strips laminated to PCBs revealed a 6% decrease of the peeling load after exposure to a neutron fluence of $7 \times 10^{15} \text{n}_{\text{eq}}/\text{cm}^2$ and a gamma dose of 67 kGy. Also, a 2% variation of the kapton coaxial cable capacitance was found after cable exposure to a neutron fluence of $1.8 \times 10^{16} \text{n}_{\text{eq}}/\text{cm}^2$ and an accompanying gamma dose of 300 kGy. The FCal resistors, capacitors, and transformers together with capacitors and sintimid disks of the purity monitor have been irradiated in liquid argon at a maximal neutron fluence of $1 \times 10^{16} \text{n}_{\text{eq}}/\text{cm}^2$ [23]. In general, the results of resistance, capacitance, impedance, leakage current and high voltage breakdown measurements after irradiation show minor changes only for some parameters. More recent HEC and FCal irradiation studies were performed and are discussed below. In the case of the EMB and EMEC calorimeters the total doses delivered in the studies above are comparable to the conditions at the HL-LHC, since the expected maximum TID and NIEL values for 4000 fb$^{-1}$ in the relevant region are of the order of 10 to 100 kGy and 0.2 to $8 \times 10^{15} \text{n}_{\text{eq}}/\text{cm}^2$, respectively, depending on the position. The observed effects in the original studies for the current detector are therefore considered small, even when applied to the expected HL-LHC luminosity.

As mentioned previously, in the HEC, the preamplification of the LAr signals is done on the detector, inside the cryostat in the LAr bath. Radiation tests have shown that the cold electronics will remain operational for 4000 fb$^{-1}$ [24] assuming a safety factor of two. The primary component of the cold electronics for the HEC is a GaAs ASIC called BB96 [25]. Each ASIC houses eight preamplifiers and two drivers or summing amplifiers. Typically the signal from four preamplifiers are summed and amplified by one summing amplifier.
Under irradiation, the gain of the preamplifiers and summing amplifiers degrade and the response becomes non-linear. Both effects are small at the expected maximum NIEL values corresponding to 4000 fb$^{-1}$. Additionally, gain degradations can be accounted for in the calibration. However, the summing of typically four signals of different height causes an irreducible non-linearity in the event that the individual preamplifiers become non-linear. A deviation of less than 1% of the output from linear expectation, normalized to the maximum expected amplitude, was the original requirement for the cold electronics chain. This level is quickly (exponentially) surpassed at Si NIEL values beyond $4 \times 10^{14}$ n$_{eq}$/cm$^2$ which would correspond to an integrated luminosity of 5000 fb$^{-1}$ (without including a safety factor). At this point, the gain degradation will reach 30%, which can be taken into account by calibration. Thus, from the radiation point of view and allowing for a safety margin, it is possible to operate the HEC cold electronics without significant losses in performance up to an integrated luminosity well above the foreseen 4000 fb$^{-1}$.

An additional irradiation campaign took place in 2010 as part of FCal R&D studies. PEEK fibres, such as the ones used in the FCal, were irradiated with 500 MeV protons up to an integrated NIEL dose of $2.7 \times 10^{17}$ n$_{eq}$/cm$^2$, which corresponds to an integrated luminosity of approximately 4000 fb$^{-1}$ for the high-$\eta$ region of the FCal. No change of fibre diameter or minimal bending radius was observed. FCal materials were also irradiated with neutrons up to $3 \times 10^{17}$ n$_{eq}$/cm$^2$. It was found that fibres, interconnection boards, and cables are not degraded.

Of special concern, at the HL-LHC, is the high particle and energy density in the forward region of ATLAS, which is covered by the FCal. In the LAr calorimeters, a nominal electric field of about 1 kV/mm is applied across the LAr gaps. Under these conditions the individual current pulses created by ionizing particles will keep their ideal triangular shape in most regions of the detector, the exceptions being the EMEC inner wheel and the FCal. The FCal is affected most by the signal degradation due to ion buildup in the LAr gaps and high current draws across protection resistors used to inject the high voltage. There were also concerns that the increased ionization load might lead to boiling of the liquid argon. For these reasons, a replacement of the FCal with a high-granularity “sFCal” with reduced LAr gap size, lower-value protection resistors and improved cooling capabilities was considered [1]. Detailed studies of the sFCal have shown that an improved measurement performance and robustness to high particle densities is indeed reached [26, 27]. However, the extraction of the FCal and installation of the sFCal involves risks which were analysed in detail, with mitigation strategies developed for those that were deemed most significant [28]. In particular, those risks leading to permanent (irreparable) damage of the EMEC and HEC calorimeters, installed in the same end-cap cryostats, the only modest performance degradation of the FCal expected at HL-LHC, together with a study showing that argon bubble formation in the FCal is not expected, and could be avoided by operating the LAr cryostat at a reduced temperature [29], have led to the decision not to pursue an FCal replacement [30]. The current FCal detectors will therefore remain in operation during the HL-LHC phase.
Finally, for stable calorimeter operations, a functioning HV system is essential. A recent survey of HV shorts that developed in the EMEC and HEC detectors showed that most of the damage happened when the cryostats were moved from the B180 assembly site to the ATLAS cavern. For example, for the HEC the number of HV shorts was 28 in B180 and 84 in the cavern, while for EMEC C 16 and 27 shorts were observed. Some channels could be recovered by applying a strong current (HV burning). Only in a few cases did both HV sides remained non-operational. For some HV channels, dedicated power supplies, which can provide higher currents, are used in order to bring them back into operation. In general, the overall number of dead HV channels has been stable in the decade since installation and there are currently no dead HV regions. With the procurement of HV supplies with improved current control [31], together with a stable LAr purity, the current HV system is expected to remain reliable in the future.
3 Requirements for the Proposed Upgrade

The upgrade of the LAr readout electronics is necessary for the LAr detector to meet the ATLAS physics goals in the demanding conditions of the HL-LHC. The trigger requirements for the high luminosity, both on the rate and on the latencies, imply a revision of the readout electronics architecture towards a free-running scheme where all data are sent off-detector. The large integrated luminosity imposes radiation tolerance requirements on all front-end components, beyond the qualification for operation of the existing electronics. Finally, the ATLAS physics programme for the HL-LHC, that comprises searches for new physics at high energies and precision physics of the Higgs sector and more generally at the electroweak scale, puts stringent requirements on the performance of the electronics chain.

In this chapter, Section 3.1 describes the requirements coming from the trigger and DAQ upgrades, that motivate the change in the LAr readout architecture. Section 3.2 summarizes the radiation tolerance that has to be achieved by all front-end components. The physics needs of the experiment also implies additional requirements on the system characteristics such as the dynamic range, linearity, noise and analog pulse shaping time. The requirements on each of these aspects are described in Sections 3.3 to 3.6, respectively. Finally, Section 3.7 describes the optimization of the digitization scheme proposed for the new LAr readout electronics.

3.1 Trigger and DAQ upgrade

The upgrade of the Trigger and DAQ (TDAQ) system is a core element of the preparation of the ATLAS detector for high luminosities. The mean number of \( pp \) interactions per LHC bunch crossing will reach values of \( \langle \mu \rangle = 200 \), which will lead to an increased number of background events passing the trigger thresholds. In order to keep a high efficiency for physics processes with signatures at the electroweak energy scale, the rate of events recorded on disk will be increased and more detailed detector information will allow a refinement of the trigger signatures.

The Phase-II TDAQ system baseline design consists in one hardware trigger level, with the option to implement a two-level hardware trigger as an evolution of the baseline solution [6], driven by physics opportunities during the HL-LHC era. In both options, the so-called Level-0 (L0) trigger is expecting detector information at a low latency with coarse granularity: nearby calorimeter cells should be summed, and the full precision on their energy is not
necessary. As specified in the TDAQ Interface Requirements Document [6], calorimeter data shall be available for the Level-0 calorimeter trigger (L0Calo) 1.7 µs after the LHC bunch crossing time. The Super Cell readout of the LAr calorimeters, which will already be installed as part of the Phase-I upgrade [2], will provide the main part of these data. In Phase-II, the new LAr calorimeter readout will extend the L0 information by providing additional inputs to the new Global Event trigger processors. Using the energies of all calorimeter cells which are above a few times the noise threshold, the system is expected to perform topological clustering (topoclustering) which will improve jet triggers, to add additional shower shape information to improve the efficiency of electron and photon triggers, and to improve pileup suppression in forward jet tagging. Section 4.4 describes some of the performance gains expected with the use of this additional information at L0.

The general TDAQ system requirements for the LAr readout are:

1. In case of a L0-only system, pre-processed calorimeter information shall be transmitted at up to 1 MHz rate to a switched trigger farm interfaced by FELIX modules. Burst rates of 8 events in 0.5 µs, and 128 events in 128 µs, must be sustained;

2. Output bandwidth and buffering capability for further development towards a two-level hardware trigger system with a L0 accept rate of up to 4 MHz and a L1 accept rate up to 800 kHz shall be provided. In this case, burst rates of 128 events in 30 µs must be sustained;

3. The LAr system shall implement data processing for local data reduction mechanisms to reduce and optimize the bandwidth to the Global Event processors. The data reduction may be done by physics-based requirements, e.g. by applying signal-over-noise thresholds, by technical data compression techniques, or by zero-suppression;

4. The precision data of all LAr readout channels shall be buffered by the LAr system until a final trigger accept or a fast-clear signal is received;

5. The data transmission and processing speed must be compatible with 1.7 µs latency for L0 input.

6. The size of the pipelines for data buffering until arrival of the trigger accept signals must match the maximum 10 µs time interval until L0 accept and the maximum value of 35 µs until L1 accept.

### 3.2 Radiation tolerance

The current front-end electronics were qualified (with safety factors) for operation for up to 1 000 fb\(^{-1}\) at \(\sqrt{s} = 14\) TeV [15], with some components showing some degradation at the highest values. While in-situ measurements have allowed a moderate reduction in the safety factors imposed on the simulated radiation levels, the reduction does not compensate the...
expected integrated HL-LHC luminosity of at least $4000 \text{fb}^{-1}$. In addition, if not replaced, the front-end electronics will be required to operate on the ATLAS detector for at least 30 years.

Table 3.1 summarizes the radiation tolerance requirements for the LAr front-end electronics and low voltage power supplies (LVPS) for a total luminosity of $4000 \text{fb}^{-1}$ (HL-LHC “ultimate” scenario). The requirements include safety factors to account for the radiation level simulation uncertainties (reduced thanks to in-situ measurements), uncertainties in low-dose rate effects in TID testing, and variations of radiation tolerance from lot to lot and within lots of components [15]. These estimates do not account for uncertainties on the expected integrated luminosity. The tolerance requirements for the LVPS are provided for two possible installation positions, at the so-called “PP2” locations and between the TileCal “fingers” (see Section 9.1). Meeting these radiation requirements imposes the use of custom devices for many components. Appendix C shows the radiation maps from which the radiation requirements are obtained.

Table 3.1: Radiation tolerance requirements for the LAr front-end electronics for operation at the HL-LHC for a total luminosity of $4000 \text{fb}^{-1}$, including safety factors given in brackets.

<table>
<thead>
<tr>
<th></th>
<th>TID [kGy]</th>
<th>NIEL [$n_{eq}/cm^2$]</th>
<th>SEE [$h/cm^2$]</th>
</tr>
</thead>
<tbody>
<tr>
<td>ASIC</td>
<td>2.26 (2.25)</td>
<td>$4.9 \times 10^{13}$ (2)</td>
<td>$7.7 \times 10^{12}$ (2)</td>
</tr>
<tr>
<td>COTS (multiple lots)</td>
<td>30.2 (30)</td>
<td>$19.6 \times 10^{13}$ (8)</td>
<td>$3.1 \times 10^{13}$ (8)</td>
</tr>
<tr>
<td>COTS (single-lot)</td>
<td>7.5 (7.5)</td>
<td>$4.9 \times 10^{13}$ (2)</td>
<td>$7.7 \times 10^{12}$ (2)</td>
</tr>
<tr>
<td>LVPS between TileCal fingers (barrel)</td>
<td>6.0 (30)</td>
<td>$4.4 \times 10^{13}$ (8)</td>
<td>$8.0 \times 10^{12}$ (8)</td>
</tr>
<tr>
<td>LVPS at PP2 (barrel)</td>
<td>0.39 (30)</td>
<td>$2.4 \times 10^{12}$ (8)</td>
<td>$3.4 \times 10^{11}$ (8)</td>
</tr>
<tr>
<td>LVPS between TileCal fingers (endcap)</td>
<td>4.26 (30)</td>
<td>$9.8 \times 10^{12}$ (8)</td>
<td>$1.5 \times 10^{12}$ (8)</td>
</tr>
<tr>
<td>HEC LVPS</td>
<td>0.32 (2.25)</td>
<td>$2.4 \times 10^{12}$ (2)</td>
<td>$3.8 \times 10^{11}$ (2)</td>
</tr>
</tbody>
</table>

### 3.3 Dynamic range

#### 3.3.1 EM calorimeters

The required dynamic range for the LAr electronics is given by the smallest and largest signals that are expected to be measured at the HL-LHC in the LAr cells.

The low end of the dynamic range is defined by the energy deposit of muons at the minimum of ionization (MIP) in one cell. These muon energy deposits are an important input to the electron energy calibration, as they allow intercalibration of the electromagnetic calorimeter layers [32], especially the first and second ones. MIP values for each layer are reported in Tables 3.2 and 3.3 for the electromagnetic barrel and endcaps, respectively. The measurement
of these low energy deposits is a challenging requirement on the noise level to be achieved by the preamplifiers.

The high end of the dynamic range imposes the maximum input current that can be transformed by the preamplifier, as well as the maximum energy that has to be digitized by the ADCs. The values used in the present system are the result of detailed simulation studies [17]. With the higher integrated luminosity of the HL-LHC, the number of collisions expected at large $x$ or large $Q^2$ increases, so resonances can be observed at higher masses. As such high energy events are rare but very important for physics, they must be well measured.

Monte Carlo simulated samples have been used to estimate the maximum currents required for the LAr cells at HL-LHC, using the following representative cases:

- The number of events that saturate LAr cells expected in the tails of SM processes, assuming the high integrated luminosity of 4 000 fb$^{-1}$, must be small, typically less than 10. This has been investigated with high-$p_T$ multijet events (where the leading jet starts at $p_T > 2$ TeV, and up to the kinematic limit) at 14 TeV with $\langle \mu \rangle = 200$ pileup;

- If a high mass $Z'$ resonance decaying to electrons exists, it must not lead to saturated signals for a significant fraction of cases. A 5 TeV $Z' \rightarrow ee$ sample has been used in this case. The design of the existing electronics required that no more than 5% of the electrons from such a 5 TeV $Z'$ would saturate a cell;

- Finally, a sample of 4 TeV single-electrons has been used to validate with higher statistics the behaviour of the tails of the energy distributions of the electrons.

The maximum signal currents were estimated by fitting the distribution tails to estimate the number of events above a given threshold at 4 000 fb$^{-1}$, or reading directly the highest current value predicted by the Monte Carlo sample. Tables 3.2 and 3.3 show the maximum currents obtained from these simulations for the electromagnetic barrel and endcaps outer wheels, respectively, and compare them with the maximum currents allowed by the present analog electronics. The highest possible currents in the middle layer for $|\eta| < 0.8$ and front layer in the endcap exceed the current preamplifier maxima. In the inner wheel of the endcap, the lower values of $\mu$A GeV$^{-1}$ yield maximum expected currents lower than those of the outer wheel, and always below 7 mA.

The baseline solution to accommodate these new estimations of the high end of the dynamic range (including some safety margin), is to replace the existing 50 Ω, 1 mA preamplifiers by 2 mA ones, and to use only one type of 25 Ω preamplifier, of 10 mA, instead of having both a 5 mA and a 10 mA variants.

### 3.3.2 Forward calorimeters

As mentioned previously, the FCal is made of LAr gaps that are much narrower than those used for the other LAr calorimeter subsystems. FCal channels therefore have a lower...
Table 3.2: Characteristic values for the LAr electromagnetic barrel cells: typical energies from MIP, maximum currents and energies allowed by the existing electronics, and new estimations of the maximum input currents as obtained in simulation.

<table>
<thead>
<tr>
<th>Layer</th>
<th>Presampler</th>
<th>Front</th>
<th>Middle</th>
<th>Back</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>&lt;0.6</td>
<td>&gt;0.6</td>
<td>&lt;0.8</td>
</tr>
<tr>
<td>MIP values [MeV]</td>
<td></td>
<td>—</td>
<td>50</td>
<td>35</td>
</tr>
<tr>
<td>µA GeV⁻¹</td>
<td>0.84</td>
<td>2.67</td>
<td>3.16</td>
<td>2.67</td>
</tr>
</tbody>
</table>

| Current electr. | Preamp. max. current [mA] | | | |
| | 1 | 1 | 5 | 10 | 5 |
| Max. energy [GeV] | 1190 | 375 | 317 | 1873 | 3165 | 1873 | 1582 |

| Req. for HL-LHC | Max. current from 5 TeV Z⁺ [mA] | | | |
| | <0.05 | 0.51 | 0.84 | 0.81 | 5.36 | 7.86 | 0.91 | 0.90 |
| Max. current from jets [mA] | <0.05 | 0.23 | 0.57 | 0.78 | 6.78 | 7.13 | 1.63 | 2.42 |
| Max. from both [mA] | <0.05 | 0.51 | 0.84 | 0.81 | 6.78 | 7.86 | 1.63 | 2.42 |

Table 3.3: Characteristic values for the LAr electromagnetic endcap cells of the outer wheel (|η| < 2.5): typical energies from MIP, maximum currents and energies allowed by the existing electronics, and new estimations of the maximum input currents as obtained in simulation.

<table>
<thead>
<tr>
<th>Layer</th>
<th>Presampler</th>
<th>Front</th>
<th>Middle</th>
<th>Back</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>&lt;1.8</td>
<td>&lt;2.0</td>
<td>&gt;2.0</td>
</tr>
<tr>
<td>µA GeV⁻¹</td>
<td>0.28</td>
<td>2.26–2.71–</td>
<td>2.26–2.69–</td>
<td>2.33–2.68–</td>
</tr>
</tbody>
</table>

| Current electr. | Preamp. max. current [mA] | | | |
| | 1 | 1 | 10 | 5 |

| Req. for HL-LHC | Max. current from 5 TeV Z⁺ [mA] | | | |
| | 0.11 | 1.90 | 1.41 | 7.15 | 7.68 | 0.22 | 0.77 |
| Max. current from jets [mA] | 0.09 | 1.61 | 0.61 | 6.16 | 3.30 | 0.89 | 1.50 |
| Max. from both [mA] | 0.11 | 1.90 | 1.41 | 7.15 | 7.68 | 0.89 | 1.50 |

Chapter 3: Requirements for the Proposed Upgrade
sampling fraction and a correspondingly lower current produced for a given energy deposit. Most of the readout channels in the FCal are produced by summing the signals from four groups of electrodes, with each group containing 4/6/9 electrodes in the FCal1/2/3. The passive summing electronics are located within the endcap cryostats and will remain in place for operations in the HL-LHC era. At the outer and inner peripheries of each module, there are also unsummed channels which are formed by a single group of electrodes, so without summing. The transformer summing halves the current from the input electrode groups; for unsummed channels that are included with summed channels in analog sums used by the trigger, the current is also halved using a “π-network” of resistors, to ensure that the energy scale is the same as for the summed channels. Unsummed channels that are not mixed with summed channels in trigger sums have an energy scale that is twice as high.

The current produced per GeV of deposited energy is determined by the calorimeter design and the cold electronics which will not be changed, so these numbers are the same as those for the existing FCal. The values (for the summed channels) are reported in Table 8 of Reference [12], which also provides a more detailed description of the FCal cold electronics.

Similarly to the electromagnetic calorimeter case, several simulation samples were investigated, that aim to probe the extreme physics events expected in the FCal. These are dijets, VBF Higgs production, and $Z' \rightarrow t\bar{t}$ events for masses of 3 and 5 TeV. In each case, pileup corresponding to $\mu=200$ was simulated. The largest currents observed in the FCal modules appear in the FCal1 modules; these are about 1.4 mA. In the FCal2 and FCal3 modules the largest currents are 0.3 mA and 0.2 mA respectively.

Taking into account the 25 Ω FCal signal cables impedance, the baseline choice described above for the EM calorimeter, of a 25 Ω, 10 mA preamplifier, can be used for the FCal cells. A better matched choice would be to use a 25 Ω, 2 mA variant.

### 3.3.3 Hadronic endcaps

As mentioned in Section 3.2, the electronics chain for the HEC comprises preamplifiers and a summing stage in the LAr cryostat, that will not be exchanged in the Phase-II upgrade.

Using the same simulation of the high-$p_T$ jets sample as in the electromagnetic case, it has been checked that the summing stages, whose dynamic range is 1 mA, are not expected to saturate in a significant number of events. This conclusion has been further validated using a simulation of single-pions of 7 TeV, which induce much higher currents than multijet or pileup events: even in such an extreme case, less than 5% of the events saturate a HEC cell.

These studies show that the dynamic range of the HEC cold electronics is well suited to the physics case of the HL-LHC.
3.4 Linearity

As explained later in section 6.2, the final energy scale of the LAr calorimeters is set in data using the $Z$ or $J/\psi$ standard candles. In order to use this knowledge with low systematic uncertainties in precision measurements, such as the determination of the Higgs or $W$ masses, excellent linearity is needed. Thus, it is desirable that the system keeps non-linearities at the per-mille level, in the range of energies used for precision measurements, i.e. typically up to 300 GeV or 10% of the full dynamic range.

Preamplifiers cannot maintain such a stringent requirement on the linearity over the full dynamic range. However, uncertainties on the energy scale are no longer dominant in physics analyses involving very high energy objects, such as searches for high mass resonances. Therefore, larger non-linearities are acceptable, especially given that they can be calibrated out\(^1\). Under the hypothesis that they are not corrected, a study has been done to estimate how large they can be without affecting the physics.

A simulated $Z' \rightarrow ee$ sample of 5 TeV has been used, in which the energy measurements of the electrons have been artificially degraded, according to the simulated integral non-linearity curve (INL) of a preamplifier simulation, shown in Figure 3.1. For the 25 $\Omega$, 10 mA preamplifier, the response is linear at the per-mille level up to 6 mA, then degrades to about 1% at 8 mA, and 4% at 10 mA. A similar curve is used for the 50 $\Omega$, 2 mA preamplifier used for the cells in the first layer.

Worst case scenarios have been tested as well, where the non-linearity goes up to 10% at 10 mA, or where the deflection point (at which non-linearities start to be sizeable) moves closer to 6 mA. In all cases, only a small fraction (3%) of the events in the $Z'$ samples were significantly affected by the non-linearities, with shifts in the energy measurement up to 80 GeV (17 GeV on average). Therefore, above 80% of the dynamic range, linearities of several percents are acceptable and do not impact the physics performance.

3.5 Noise

The noise term of the calorimeter resolution is the sum of electronics (preamplifier) noise, quantization noise and pileup noise, after shaping and digital filtering. This term is the dominant contribution to the total energy resolution for low energy particles, and should therefore be minimized.

At high luminosity, the pileup noise will dominate over the other terms. However, as the luminosity may change during the 10 years of HL-LHC operation, the ability to measure small signals such as muon MIPs should be preserved, as this is an important element of the

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\(^1\) The calibration system described in chapter 6 measures the noise and the gains of each LAr cell. The energy ramp runs could however be used as well, in case of large non-linearities at high energies, to correct for them.
Figure 3.1: INL curve from an early 10 mA preamplifier design, used to shift the measurement of high energy cells. The gain of the preamplifier is obtained by a linear fit in the 0 to 6 mA range. The residuals above 6 mA are changed to explore worse case scenarios.

LAr calibration. The measurement of the MIP signals as part of the inter-layer calibration is done statistically using large samples; however the measurements still require a signal-to-noise ratio typically greater than 0.75 to be reliable. Furthermore, it is also likely that ATLAS will continue to pursue certain types of precision physics, where low $\mu$ operation will give improved results; therefore the performance of the new electronic readout at low $\mu$ must be equivalent to that of the existing system. The electronics noise should therefore be lower than the MIP signal.

Hence the requirements on the electronics noise should not be relaxed compared to the existing electronics: the preamplifiers should target noise values of the order of 50 MeV on a single sample before optimal filtering for the second layer in the EM calorimeter.

The optimal filtering technique [16] used in the back-end is designed to reduce the total noise (electronics and pileup), where the pileup noise consists of in-time pileup and out-of-time pileup contributions of similar size. The out-of-time pileup contribution to the noise term can be reduced by using digital filters with active out-of-time pileup correction, as they estimate the size of the out-of-time pileup on an event by event basis. Such techniques have already been studied in the context of the Phase-I upgrade of the trigger readout [2], and typically make use of the amplitude of the signal before the pulse to be measured, to estimate the size of the out-of-time pileup contribution.

The use of a free-running architecture, where all data are sent to the back-end – compared to 4 samples per pulse to 100 kHz of L1 triggers in the present system – makes it possible to use such filters, to reduce the total noise beyond what is feasible with the optimal filtering.
The choice of an algorithm requires in-depth studies, as the performance has to be evaluated under various hypotheses for the bunch-train structure, and as differences between real pulse shapes and ideal pulse shapes used to tune the algorithms end up in the constant term of the resolution, that dominates for high-energy electrons and photons. Performance expectations using optimal filtering are presented and discussed in Section 4.1.

### 3.6 Shaping

The analog shaping of the triangular LAr physics pulses before their digitization is an important step to reduce the total noise of the energy measurement, and thus get the best energy resolution. The characteristics of the present shapers, bipolar of type CR-(RC)$^2$ with a shaping time of 13 ns, are the result of an optimization presented in the original LAr calorimeter TDR [17] to balance electronics and pileup noise. It is expected that the conclusions presented there still hold to a large extent.

The use of monopolar shaping could reduce the power consumption and would allow the use of the full dynamic range of the ADCs, while bipolar shaping requires that a quarter of this be reserved for the negative lobe of the pulses. However, the absence of pedestal shift with bipolar shaping simplifies considerably the rest of the design.

Bipolar shapers can have different numbers of integration stages, as well as various peaking times, which both affect the total noise (electronics plus pileup) on the analog pulse. The optimal configuration can vary for different calorimeter cells and pileup levels, as it depends on the exact pulse shape and on the relative weights of electronics and pileup noise. Figure 3.2 shows the total noise for one EM cell from the middle layer and one HEC cell, as a function of the pileup level, for different shaping functions. The optimal filtering coefficients (OFC) are computed for each case. For the EM cell considered, the CR-(RC) filter yields too short a peaking time and therefore a larger noise level. No significant differences can be seen between the CR-(RC)$^2$ and CR-(RC)$^3$ cases. For the HEC, a CR-(RC)$^2$ shaper improves the noise by 5% over a CR-(RC)$^3$.

It has been shown in [17] that the resolution at the maximum of the pulse depends critically on the peaking time of the shaper, where longer peaks are preferred to reduce electronics noise, and shorter peaks are better against pileup noise. A peaking time of 13 ns is used in the current system. Figure 3.3 shows the total noise for the representative cells, when varying the peaking time of a CR-(RC)$^2$ shaper around 13 ns. For the representative EM cell, the peaking time of 13 ns is shown to be close to minimizing the total noise at high pileup, while the HEC cell results show at high pileup a 5% reduction of the total noise when reducing the peaking time from 13 ns to 8 ns. The optimal peaking time depends on the precise pulse shape and noise levels, which in turn depend on the cell capacitance and cable length. For a fixed shaper, the optimal peaking time is then expected to vary across all cells of the calorimeter.
Figure 3.2: Total noise as a function of the level of pileup, $\mu$, for a cell from the EM middle layer at $\eta = 0.5$ (a) and a HEC cell in the first layer at $\eta = 2.35$ (b), obtained after optimal filtering, for different numbers of integration stages in the shaper.

Figure 3.3: Total noise as a function of the level of pileup, $\mu$, for a cell from the EM middle layer at $\eta = 0.5$ (a) and a HEC cell in the first layer at $\eta = 2.35$ (b), obtained after optimal filtering, for different peaking times of the shaper.

The baseline is to keep using CR-(RC)$^2$ shaping, and to require that the peaking time be programmable in order to adjust for differences in the LAr signals between different parts and layers (since, for instance, the FCal has much faster pulses due to smaller LAr gaps).
3.7 Digitization

3.7.1 Gain switching

Tables 3.2 and 3.3 show that the dynamic range for the physics signals to be measured in the LAr cells is typically 14 to 15-bits wide. As explained in Section 3.5, the electronics noise needs to be lower than the MIP signal, so it can be measured. The least significant bit (LSB) value of an ADC needs to be even lower, in order for the quantization noise to be smaller than the electronics noise. Hence the total dynamic range to be digitized is typically 16-bits wide.

The baseline development for the ADCs to be used on the new FEBs targets 14-bit, radiation hard 40 MHz ADCs of 12-bit precision using 12-bit SAR blocks and a dynamic range enhancer (DRE). A two-gain system must therefore be used, where each ADC digitizes only a part of the dynamic range. The baseline option is to transmit the ADC outputs for both gains to the LAr off-detector electronics.

The gain ratio between the two outputs has been studied for both preamplifier types, to ensure that the following requirements are simultaneously met:

• The full dynamic range of the preamplifier (10 mA or 2 mA) is digitized;
• The quantization noise must be lower than the electronics noise, knowing that it is typically around half a LSB;
• The bipolar shaping of the LAr pulses requires that about a fourth of the dynamic range is used for the negative lobe (pedestal values around 4 000 for a 14-bit ADC), and even more in the FCal;
• At the lowest energy at which the low gain is used (gain-switching energy), the quantization noise must stay lower than the intrinsic LAr resolution (typically $10\% / \sqrt{E/\text{GeV}} \oplus 0.2\%$ in the EM calorimeters), in order not to degrade the total resolution by more than 5%.

These requirements are most difficult to meet simultaneously in the EM calorimeters, especially in the first and second layers. Studies have shown that a system with two 14-bit ADCs, with gain ratio 30, can fulfil all of them, with the electronics noise being typically 4 times larger than the LSB, and the quantization noise being a factor 5 to 10 lower than the LAr resolution at the gain-switching energy. Figure 3.4 shows the comparison of the quantization noise with the intrinsic LAr resolution in this scheme, for the front and middle layers of the EM calorimeter.

As a last requirement, it is desirable that most of the photons from $H \rightarrow \gamma\gamma$ decays have all their cells in the high gain. With the present system of three gains, with 12-bit ADCs, the electrons from $Z$ decays used to set the energy scale mostly have all their cells in the high gain, while many photons from $H \rightarrow \gamma\gamma$ decays have a cell in the medium gain. Any
3.7 Requirements for the Proposed Upgrade

3.7.2 Sampling rate

The requirement on the choice of the digitization sampling rate is that it minimizes the data transfer bandwidth to the back-end while providing sufficient information to obtain a cell-level performance close to ideal.

The existing electronics digitizes the analog signals at 40 MHz. Sampling at 80 MHz provides additional information on the pulse shape, which can in principle be used to improve the energy resolution. Figure 3.7 compares the expected noise for different levels of pileup for 40 and 80 MHz sampling rates, when the energy reconstruction is done by optimal filtering. Moving to 80 MHz yields some gain in the noise in all cases. Such a modest improvement, of

 imperfect knowledge of the gain intercalibration is a source of systematic uncertainty, as was observed in the measurement of the Higgs mass in Run 1 [33]. Fulfilling the stated requirement would eliminate this effect.

A simulated sample of $H \rightarrow \gamma\gamma$ events has been used to check the proposed digitization scheme. The maximum energy in a cell is computed for each photon in the front and middle layers separately. The results are shown in Figure 3.5. Taking a safety margin and assuming that gain switching would occur at 90% of the maximum output of the high gain, only about 1.7% (4.3%) of the photons would have a cell from the middle (front) layer in the low gain using the proposed scheme. Furthermore, mostly photons in the endcaps would be affected, as shown in Figure 3.6.
Figure 3.5: Maximum energy in cells in photons coming from $H \to \gamma\gamma$ events for (a) front layer and (b) middle layer of the LAr EM calorimeter. The energy above which the cell would be in the low gain, assuming gain switching occurs at 90% of the maximum high gain energy, is indicated as a black arrow.

Figure 3.6: Pseudorapidity distributions of the fraction of $H \to \gamma\gamma$ photons which would have a cell in the low gain (yellow), and of those which would have a middle layer cell in low gain (red).
the order of 5% to 10% at $\mu = 200$, is expected as the readout samples are highly correlated due to the shaping time of 13 ns. Even a faster shaping of $\tau = 8$ ns does not improve the EM and HEC noise further. These numbers do not justify the doubling of the bandwidth required to transmit the samples to the back-end electronics at 80 MHz.
4 Expected Performance of the LAr Calorimeters

The goals of the HL-LHC physics programme include precision measurements of Higgs boson properties and of other SM processes, as well as searches for phenomena beyond the SM.

The LAr calorimeter system plays a critical role in enabling a rich and varied ATLAS physics programme; for example, the performance of the electron, photon, jet and missing energy reconstruction depends directly on the LAr calorimeter system performance. It is therefore of utmost importance that the upgraded readout electronics for the LAr calorimeter system provide the ability to maintain overall an object and physics performance similar to that achieved in Run 2, even under the harshest running conditions expected at HL-LHC.

Section 4.1 presents the performance expectations at the cell level, using the digital filtering algorithm currently used in the ATLAS readout in Run 2 (the optimal filter). The new LAr Signal Processor (LASP) system will provide the ability to run more sophisticated digital filtering algorithms that will make it possible to suppress in part the contribution of out-of-time pileup thereby improving the cell-level resolution that can be achieved under the harshest HL-LHC running conditions. The calorimeter cell-level energy resolution has a direct impact on the performance of energy measurements of objects such as electrons, photons, jets and missing transverse energy.

Section 4.2 briefly describes the current algorithms used to reconstruct electrons, photons, jets and missing transverse energy and illustrates their performance in conditions expected at the HL-LHC with an upgraded detector. The algorithms used to reconstruct these objects will eventually be modified to take full advantage of the new upgraded detector capabilities as well as re-optimized to account for the different pileup level expected at HL-LHC. With new pileup mitigation techniques based on full detector information (calorimeter, tracking, timing), object reconstruction performance comparable to those of Run 2 should be achievable. Maintaining the electron and jet energy resolution achieved in Run 2 is essential, for example, in order to reconstruct new narrow resonances decaying into two electrons or jets. Measurements of the properties of the Higgs boson and other SM processes will also require an electron, photon, jet and $E_T^{miss}$ performance comparable to those achieved in Run 2.

Section 4.3 illustrates the expected physics capability of the upgraded detector for a few examples of physics final states that depend directly on the performance of the LAr calorimeter.
Unless otherwise explicitly indicated, the studies presented in this chapter are based on full simulations of the Phase-II upgraded ATLAS detector using GEANT4 [34]. The effect of multiple simultaneous $pp$ collisions, both from the same crossing and previous/subsequent crossings are simulated by overlaying additional generated minimum bias events on the hard-scatter event prior to digitization. The number of overlapping $pp$ collisions ($\mu$) is simulated as Poisson distributed. The LAr pulse reconstruction is done using an optimal filter of depth of 5 with optimal filtering coefficients computed for the pileup condition of interest (e.g. $\mu = 0$ and $\mu = 200$). The number of samples chosen corresponds to the original design of the calorimeter, and is that used in Run 1. The Phase-II upgraded detector simulation assumes the LAr system Run 2 electronics noise level.

As mentioned in Chapter 3, the use of more sophisticated filtering algorithms is planned to better suppress out-of-time pileup. The performance results obtained with an optimal filter of depth 5 should therefore be understood as a worst case for these high pileup conditions. When appropriate, the text will mention the expected further improvements.

### 4.1 Cell-level performance

This section illustrates the cell-level performance of the LAr readout at a high luminosity up to $\mu=200$.

The energy resolution of the calorimeter is given by the equation

$$\frac{\sigma_E}{E} = \frac{a}{\sqrt{E}} + b + c$$

(4.1)

where the sampling term $a$ depends on the construction of the calorimeter, and the constant term $c$ depends on the precise knowledge of the non-uniformities in the geometry of the calorimeter or in the pulse shapes. Therefore the figure of merit used in this section is the noise term $b$ of the energy resolution. It comprises analog electronics noise (coming mainly from the pre-amplifier), digitization noise, and pileup noise, which is expected to dominate at the HL-LHC.

Energy measurements in the current LAr back-end system are obtained using an optimal filtering algorithm [16] using 5 samples in Run 1 and 4 samples in Run 2. The reduction in the number of samples took place to accommodate an increase of L1 trigger rate (up to 110 kHz), without increasing the dead time of the system. The baseline algorithm retained for the simulation of Monte Carlo samples of the Phase-II upgrade uses 5 samples.

After the application of this optimal filtering algorithm, Figure 4.1 shows the total noise expected in several different LAr cells, representative of the various layers and at different rapidities, as a function of pileup conditions. The optimal filtering coefficients are always tuned to minimize the total noise in each pileup configuration. The pileup noise dominates
over the electronics noise in the high pileup scenarios, and is more important at large rapidities, as expected. Typically, the pileup noise contributes 85 to 90% of the total noise for a middle cell of the EM barrel at $\mu = 200$, hence the noise term of the cell-level energy resolution is shown to be more than three times larger at $\mu = 200$ than that obtained without the presence of pileup.

![Figure 4.1: Total noise as a function of the level of pileup for various calorimeter cells from the EM part (a) and the HEC (b).](image)

After the Phase-II upgrade, the LASP system will provide the resources necessary to implement more sophisticated digital filtering algorithms and/or use increased filter depth. This will provide the ability to suppress in part the effect of out-of-time pileup on the energy measurement in order to maintain adequate cell energy resolution even under the highest pileup conditions expected at HL-LHC. Simulations of the noise level expected in the absence of out-of-time pileup show that an improvement of the noise term of the resolution of up to 20 to 25% compared to the optimal filtering can be theoretically achieved. This is illustrated in Figure 4.2, which compares the application of optimal filtering on a sample with the standard pileup distribution and on a sample with only in-time pileup, which corresponds to the case of an ideal algorithm that would perfectly subtract the out-of-time pileup contribution. An improvement of the order of 20% is observed.

Figure 4.3 shows the total noise obtained when increasing the filter depth of the optimal filtering algorithm, with up to 13 samples on two representative cells. At low $\mu$, where the electronics noise dominates, a small gain can be achieved on the resolution, as this effectively integrates the signal over a longer time. At high pileup, only a modest improvement in noise of the order of 5% is obtained when using up to 13 samples. Further improvement in noise at high pileup will come from new algorithms, that will more significantly benefit from the increased filter depth.

The development of filters with out-of-time pileup correction, such as the Wiener filter with and without active pileup correction [35–37], as well as the extended optimal filter (EOF) [36, 38, 39] was started in the context of the LAr trigger upgrade in Phase-I [2] for the
Figure 4.2: Pileup contribution to the noise term of the resolution of unconverted photons in the barrel, when only the in-time pileup contribution (red) or the full contribution (black) is present.

Figure 4.3: Total noise as a function of the level of pileup for a cell from the EM middle layer at \( \eta = 0.5 \) (a) and a HEC cell in the first layer at \( \eta = 2.35 \) (b), for various filter depths.

Super Cell readout with promising results. In the EOF approach, the sampling points are assumed to result from the sum of a sequence of pulses, and the digital filter coefficients are determined such that the filter output is proportional to the deposited energy at a given bunch-crossing and insensitive to out-of-time pulse contributions. The Wiener filter directly aims at a filter output which is non-zero only at times where an energy deposit with the expected signal pulse shape is detected, but requires additional filter stages to correct for the negative tail of the pulse which contributes to subsequent pulses (forward correction). The adaptation and optimization of such digital filtering algorithms to be used in the LASP in Phase-II is ongoing. Simulations show that, using up to 24 samples, these algorithms are capable of reducing the out-of-time pileup noise while having a slightly less optimal in-time noise suppression compared to the OF. Figure 4.4 illustrates this behaviour in the case of a Wiener filter with forward correction, which is able to correctly measure the energy of a low energy pulse occurring in the tail of a high energy one. Figure 4.5 shows a
comparison between the total noise obtained with the optimal filter and that obtained with the Wiener filter with forward correction, for a HEC cell at large rapidity that receives large pileup contributions. Under lower pile-up conditions and/or in regions of the calorimeter where the electronics noise dominates, the optimal filter performs best since it optimizes the filter output to provide the smallest total noise level. However, in a region of the calorimeter dominated by pileup noise, the event-by-event subtraction of the out-of-time pileup performed by the Wiener filter with forward correction is shown to outperform the optimal filter, yielding a decrease of the total noise of approximately 5% at $\mu=200$. Further developments of this kind of filters are expected to eventually yield larger performance improvements.

Figure 4.4: Although an ideal Wiener filter (WF) only yields a single energy output for a given waveform, a realistic implementation of a Wiener filter requires a correction of the trailing non-zero tail, which is achieved by corrective filter element, the “forward correction”. (a): Illustration of the “forward correction” feedback loop that is activated when a detected pulse shape agrees with the expected signal shape. (b): Output of a Wiener filter with “forward correction” (WFFC), which illustrates the capability of this filter to reduce noise and measure smaller amplitude pulses on the negative lobe of a large amplitude signal. Figures taken from [37].
Filters doing out-of-time pileup subtraction usually rely on a precise knowledge of the signal pulse shape, especially its tail, and of the pileup conditions. Their performance is thus affected by differences between the predicted and the actual pulse shapes, which can end up increasing the constant term of the energy resolution. Optimal filtering is almost insensitive to the knowledge of the tail of the pulses, and only mildly sensitive to that of the peak, as illustrated in Figure 4.6. It shows the total noise obtained for various pileup conditions, when the optimal filtering coefficients have been tuned for $\mu = 140$. The tuning of the optimal filtering algorithm is only mildly sensitive to the pileup level, as using coefficients tuned for $\mu = 140$ at $\mu = 80$ or $\mu = 200$ leads to degradations of the noise below 5–10% compared to using coefficients optimized for each pileup level.
Most of the physics studies shown in the next sections assume that energy measurements are obtained using the current optimal filtering algorithms with filter depth of 5, and therefore do not take into account the planned improvements in out-of-time pileup suppression. The performance is therefore expected to demonstrate a worst case scenario, and even in this case it is shown that adequate overall physics performance is achieved using full detector information which will make it possible to carry out the HL-LHC physics programme.

4.2 Object reconstruction performance

The reconstruction of electrons, photons, jets and missing energy directly depends on the energy measurements provided by the LAr detector systems. This section briefly describes the Run 2 algorithms used to reconstruct different objects and the performance expected from these algorithms using the upgraded ATLAS detector layout at HL-LHC and pileup conditions of $\mu = 200$. A brief discussion of possible improvements in the reconstruction algorithms is also included.

4.2.1 Electron and photon reconstruction

EM object reconstruction

The EM showers that develop in the LAr calorimeter are currently reconstructed as EM clusters of calorimeter cells using the “sliding-window” algorithm [40]. In this algorithm, the EM calorimeter $\eta \times \phi$ space is divided into a matrix of elements with size $\Delta \eta \times \Delta \phi = 0.025 \times 0.025$ (the size of a cell in the middle EM calorimeter layer).

The reconstruction algorithm then proceeds in two steps. First, calorimeter regions where the transverse energy exceeds a given threshold are identified as cluster seeds. The position of a cluster seed is defined as the energy-weighted barycentre of all cells within this region. Then, an EM cluster is built around a seed by adding cells within a window of size $N_{\eta}^{\text{clus}} \times N_{\phi}^{\text{clus}}$ around a layer-dependent seed position. Cells in the middle layer are assigned to the cluster if they fall within the cluster window defined around the position of the seed. Cells in the front and back layers are processed using a similar procedure using a window positioned, this time, around the energy-weighted barycentre of the cells included in the middle layer. Finally, the energy-weighted barycentre of cells in the front layer is used for the clustering of cells in the presampler layer. As a result of this procedure, a set of EM clusters of fixed size $N_{\eta}^{\text{clus}} \times N_{\phi}^{\text{clus}}$ is created; a different size is used to defined clusters in the barrel and the endcap region. Since the beginning of Run 2, the cluster size used is $3 \times 7$ in the barrel and $5 \times 5$ in the endcap. The size is the same for electron as well as converted and unconverted photon candidates.
In recent releases of the ATLAS software, the baseline reconstruction of EM objects uses so-called super-clusters, that work like topoclusters [41] within a given window. These super-clusters better recover losses due to bremsstrahlung; however, they tend to add more cells to each cluster than the fixed size windows, which increases the pileup noise in HL-LHC conditions. The electron and photon performance discussed below is however still using the fixed size clusters.

**Electron and photon reconstruction**

Tracks reconstructed in the inner detector are matched to the EM clusters. Candidate conversion vertices are also reconstructed from pairs of tracks. Quality criteria on the tracks, the conversion vertices, and on the matching between tracks and clusters, are then used to classify the EM clusters as candidate electrons, unconverted photons or converted photons. References [42, 43] give a complete description of this procedure.

Different sets of quality cuts are applied on the tracks, on the cluster shower shapes and on the matching between tracks and clusters of the electron and photon candidates: they are tuned to select true electrons (photons) with high efficiency, while rejecting most of the hadrons that may fake an electron (photon) signature. The fine transverse segmentation of the calorimeter, as well as its division in three layers in depth, allows the use of many criteria to select the EM showers from electrons and photons. Powerful variables exploit the ratios of energy depositions in the calorimeter layers (including leakage into the hadronic calorimeter), or the moments of the transverse energy distribution in the first and second layers (typically the shower width). In particular, the very fine segmentation in $\eta$ of the first layer allows the rejection of $\pi^0$s by looking for two maxima of energy deposition.

The expected performance of the electron identification in Phase-II has been studied in the context of the Inner Tracker Strip Detector TDR [44].

A cut-based identification algorithm has been developed with three working points for the electron efficiency, referred to as Loose, Medium, Tight, with increasing rejection of backgrounds, and that target identification efficiencies close to the equivalent working points of Run 2. The identification requirements vary according to the transverse energy and pseudorapidity of the electron candidate, in the range $p_T > 7$ GeV and $|\eta| < 2.5$. The samples used for this analysis use the inclined ITk layout, and are evaluated for $\mu$ in the range 190 to 210. A $Z \rightarrow ee$ MC sample is used for the prompt electrons, and dijet MC samples are used to study background electrons.

These background electrons are mainly misidentified charged hadrons, photons converting in the inner detector material, and electrons from semi-leptonic decays of $b$- or $c$-hadrons. Track-based variables are of primary importance for the rejection of photon conversions and semi-leptonic decays, while the shower shape in the calorimeter is very efficient at discriminating charged pions.
Figure 4.7 shows the overall efficiency to reconstruct and identify generator-level isolated electrons, while Figure 4.8 displays the probability of reconstructing and misidentifying generator-level jets as electrons. Overall, rejection factors of background electrons of the order 600 to 3000 are achieved, for identification efficiencies of the prompt electrons of 89 to 63%. This is similar to what was achieved with a cut-based approach in Run 1 [45]. In Run 2 a multivariate discriminant is used, that combines many track- and calorimeter-based variables, and achieves an improved rejection of a factor 2 to 5 for the same efficiencies. It is expected that the use of similar techniques will lead to equivalent gains at HL-LHC.

Figure 4.7: The electron selection efficiency (relative to generator-level and including both reconstruction and identification) as a function of $E_T$ (a) and $|\eta|$ (b).

Figure 4.8: The efficiency (relative to generator-level) with which jets are reconstructed and identified as electrons as a function of $E_T$ (a) and $|\eta|$ (b).
Electron and photon energy measurement

The EM clusters contain a large fraction of the deposited energy for electron and photon candidates; however, some energy is not contained in the fixed-size cluster and some is lost upstream or downstream of the calorimeter, creating the need to apply corrections offline [32]. Calibration constants are calculated from MC simulation as a function of $\eta$, energy and shower depth. Residual correction factors for the energy scale are set using reconstructed mass distributions from $Z \to ee$ events, e.g. from data.

Figure 4.9 illustrates the expected energy resolution of photons under $\mu = 0$ and $\mu = 200$ pileup conditions, assuming the same reconstruction techniques as those currently employed in Run 2. Simulated $H \to \gamma\gamma$ events produced via VBF are used and the resolution is shown only for unconverted photons in the barrel region of the detector ($|\eta| < 0.8$). As for all other studies presented in this chapter, the level of electronics noise simulated is that of the existing LAr readout. The photon resolution curves obtained at $\mu = 0$ and $\mu = 200$ are subtracted in quadrature in order to illustrate the size of the pileup-only contribution to the photon resolution. The pileup noise contribution is the dominant contribution to the photon energy resolution for photons with energy up to 140 GeV, and has an increasing impact for lower photon energies.

Figure 4.10 compares the simulated electron energy resolution in Run 2 to that expected at HL-LHC, assuming the same electron reconstruction techniques are employed. Electrons from a single-electron sample are used to obtain the Run 2 curve, while electrons from $Z \to ee$ decays are used for the HL-LHC expected resolution. The reconstructed energy of the electrons are smeared so that the constant term of the resolution matches the one measured in Run 2 data. As for photons, the electron energy resolution is seen to degrade
with increasing pileup, the effect being the largest for electron energy less than 120 GeV in the barrel. The effect is much larger in the endcaps, where pileup noise dominates up to higher energies.

It is expected that the noise term in the electron/photon energy resolution curve will improve by the time of the construction of the HL-LHC over the one shown in Figures 4.9 and 4.10. As discussed in Section 4.1, the use of more sophisticated digital filtering techniques should provide a reduction in the noise from out-of-time pileup. Furthermore, the electron/photon cluster size 1, or the choice of cells included in the super-clusters, can be tuned to limit the pileup contribution, with an expected improvement of up to 15%. The use of particle-flow-like techniques making use of the Phase-II upgraded detector capability (tracking, energy and timing) could also lead to a better treatment and a reduction of the in-time pileup.

The measurement of the electron energies could also make use of the track momentum reconstruction. Because of bremsstrahlung effects, the resolution of the electron cluster energy is better than that of the track momentum for $p_T > 15$ GeV in the existing detector, thus only the cluster energy is used. After Phase-II upgrade, the ITk should have a better resolution than the current tracker and the amount of material (hence $X_0$) in front of the calorimeter should be reduced (reducing the bremsstrahlung impact), while the cluster energy will be more affected by pileup, so a combination of the tracker and calorimeter measurements will probably be useful for electrons of energies up to a few tens of GeV.

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1 The existing cluster sizes used in Run 2 were optimized for $\langle \mu \rangle = 40$ [46]
Finally, the very high statistics of data samples used for the calibration of the electron energies, typically $Z \rightarrow ee$, will allow to reduce the constant term of the energy resolution. Important components of the constant term are non-uniformities in the calorimeter response and the knowledge of the material upstream of the calorimeter. Both can be improved by a more granular calibration procedure, which requires very large samples of data. The constant term is thus expected to reach its design value of 0.7%.

4.2.2 Jet reconstruction

The reconstruction of jets in ATLAS proceeds as follow. First, clusters of calorimeter energy deposits are reconstructed using the topological clustering algorithm [47] which performs three-dimensional reconstruction of particle showers. Clusters are seeded by cells whose absolute energy measurements exceed four times the expected noise, which includes both electronic noise and the average expected contribution from pileup. This provides a first mitigation of the impact of pileup at the cluster level. The hadronic topological clusters are then calibrated using a local cluster weighting (LCW) scheme [47]. Jets are then reconstructed from these locally calibrated topological clusters using the anti-$k_t$ algorithm [48, 49] implemented in FASTJET [50] and using a radius parameter of 0.4. The reconstructed jets are then calibrated to the stable-particle-scale using a numerical inversion method [51].

Pileup in $pp$ collisions at the LHC has a significant impact on jet reconstruction. In Run 2, the impact of pileup is mitigated using a jet-based correction performed with the jet-area method described in Reference [52]. The $p_T$ of each anti-$k_t$ jet in the event is corrected with

$$p_{T,\text{corr}}^\text{jet} = p_T^\text{jet} - \rho \times A$$

(4.2)

where $\rho$ is the transverse momentum density (i.e. the amount of transverse momentum per unit area that is added by pileup) and $A$ is the jet area in ($\eta$, $\phi$) space.

To effectively mitigate the impact of the expected level of pileup at HL-LHC, the performance of several algorithms acting at the jet-constituents level has been studied. Details of this study can be found in Reference [53].

One of the constituent-level pileup mitigation technique studied is the Voronoi subtraction method which extends the concept of the jet-area correction to the constituent level. In the Voronoi subtraction, each jet constituent forms a Voronoi cell in ($\eta$, $\phi$) space which contains all points that are closer to that constituent than to any other. For each individual constituent (i.e. cluster) the pileup-corrected $p_T^\text{cluster}$ is calculated as

$$p_{T,\text{corr}}^\text{cluster} = p_T^{\text{cluster}} - \rho \times A_{\text{Voronoi}}$$

(4.3)

where $\rho$ is again the transverse momentum density (i.e. the amount of transverse momentum per unit area that is added by pileup) and $A_{\text{Voronoi}}$ is the area of the constituent taken to be equal to the Voronoi area. After subtraction, several clusters have negative values of...
\(p_{\text{cluster,corr}}\) which cannot be used as inputs for jet reconstruction with standard clustering algorithms. One technique to suppress negative fluctuations in pileup energy density is to “spread” any negative values of \(p_{\text{cluster,corr}}\) to nearby clusters such that after spreading every cluster has \(p_{\text{cluster,corr}} \geq 0\) GeV and jet clustering can be performed.

Unlike the calorimeter-based Voronoi subtraction, the cluster vertex fraction (CVF) pileup mitigation technique also uses tracking information. The technique consists of determining the fraction of a cluster \(p_T\) that is due to charged particles from the primary vertex. The CVF subtraction algorithm is then carried out by simply removing from the event the clusters which have only tracks from pileup vertices associated to them.

The calorimeter-based Voronoi subtraction and the CVF method are complementary and can be both applied to an event.

Figure 4.11 shows the jet \(p_T\) resolution of low-\(p_T\) jets achieved at (a) \(\langle \mu \rangle = 20\), (b) \(\langle \mu \rangle = 80\) and (c) \(\langle \mu \rangle = 200\) using different pileup mitigation techniques all described in Reference [53]. At \(\langle \mu \rangle = 20\), the standard jet-area subtraction technique currently used in Run 2 improves the jet \(p_T\) resolution by approximately 5% compared to uncorrected jets. The constituent-level pileup mitigation techniques considered in the study do not provide any significant additional improvement in the jet \(p_T\) resolution compared to performance achieved with the jet-area subtraction method. At \(\langle \mu \rangle = 200\), however, the use of a constituent-level pileup mitigation technique significantly improves the jet \(p_T\) resolution; for example, the combination of the Voronoi subtraction with negative energy spreading and CVF (“Vor. Spread. + CVF 5 GeV”) improves the resolution by nearly 20% as compared to the resolution achieved by the standard (jet-level) area-subtracted method. Significant improvement in jet \(p_T\) resolution is obtained for jets of transverse momenta up to 50–60 GeV. In particular, the performance of the “Vor. Spread. + CVF” algorithm at \(\langle \mu \rangle = 200\) is similar to that of the jet area subtraction at \(\langle \mu \rangle = 80\). Given that the Run 2 pileup profile is in between the \(\langle \mu \rangle = 20\) and the \(\langle \mu \rangle = 80\) cases, and that the jet-area subtraction method is used, it means that the combined use of Voronoi subtraction and CVF at \(\langle \mu \rangle = 200\) would achieve a jet \(p_T\) resolution that is within 15% of that obtained in Run 2.

This study demonstrates the potential of constituent-level pileup corrections methods to achieve adequate jet reconstruction performance at HL-LHC.

### 4.2.3 Missing energy reconstruction

In Run 2, the missing transverse energy \(E_T^\text{miss}\) is computed as the vector momentum sum of high \(p_T\) physics objects in the event, plus a soft-term, from particles which are not associated with high-\(p_T\) objects. The soft term in ATLAS is only computed using charged tracks assigned to the hard-scatter vertex [54]. Jet vertex tagging techniques, aimed at removing jets originating from pileup vertices, are crucial to maintain good \(E_T^\text{miss}\) resolution under the high pileup conditions expected at HL-LHC. The Phase-II upgraded ATLAS detector will have a new tracker with an acceptance extending to \(|\eta| < 4\) (as compared to the current...
Figure 4.11: Transverse momentum resolution of low-$p_T$ jets reconstructed with anti-$k_T$ with $R = 0.4$ versus true jet $p_T$. An average of (a) 20, (b) 80 or (c) 200 pileup events is superimposed on the multijet signal. The different constituent-level pileup mitigation methods presented are explained in Reference [53]. Monte Carlo statistical uncertainties are negligible, and the estimated jet energy resolution uncertainty is 2–3%.
tracker acceptance of $|\eta| < 2.5$). This will make it possible to extend track-based pileup suppression techniques to the forward region and improve the performance of the $E_T^{\text{miss}}$ reconstruction in high pileup conditions.

The impact of the increase in tracker acceptance on the $E_T^{\text{miss}}$ reconstruction is studied using a simplified version of the $E_T^{\text{miss}}$ recommended calculations for Run 2 [54]. The $E_T^{\text{miss}}$ is reconstructed using selected muons with $p_T > 2.5$ GeV or $p > 4$ GeV, electrons with $p_T > 10$ GeV, and jets with $p_T > 20$ GeV that satisfy the requirement of $R_{pT} > 0.1$. The discriminant $R_{pT}$ [55], is used to tag and suppress pileup jets, and is defined as the scalar $p_T$ sum of the tracks that are associated with a jet and originate from the hard-scatter vertex $PV_0$, divided by the fully calibrated jet $p_T$, i.e.

$$ R_{pT} = \frac{\sum_k p_{trk}^{(PV_0)}}{p_{jet}^T}. \; \; \; (4.4) $$

Pileup jets typically have a small value of $R_{pT}$ corresponding to jets with small charged particle $p_T$ fraction originating from the hard scatter vertex $PV_0$. Finally, tracks coming from the hard-scatter, not associated to muons, electrons or jets, are used to reconstruct the soft-term of the $E_T^{\text{miss}}$.

Figure 4.12 shows the $E_T^{\text{miss}}$ resolution derived from simulated $t\bar{t}$ events with $\langle \mu \rangle = 200$ as function of the number of primary vertices, $N_{PV}$, in the event. The red (black) curve is obtained using tracking information up to $|\eta| < 2.7$ ($|\eta| < 4.0$) which corresponds to the acceptance of the current (new) tracker. In such $t\bar{t}$ events the $E_T^{\text{miss}}$ scale is driven by the energy measurement of the hard scatter objects (electrons, muons and jets) in the calorimeters and in the muon spectrometer, so although the scale is not explicitly corrected to be the same in the two cases, it is sufficiently close that the resolutions can be directly compared. The $E_T^{\text{miss}}$ resolution is therefore improved by approximately 20% using the full acceptance of the new tracker which improves the ability to remove pileup jets in the forward region of the detector. The $E_T^{\text{miss}}$ resolution with the new tracker is also shown to be slightly less dependent on $N_{PV}$.

New pileup jet algorithms, e.g. using timing information from the High Granularity Timing Detector (HGTD), may further improve the $E_T^{\text{miss}}$ performance. Figure 4.13 illustrates the improvement in forward jet pileup suppression that can be achieved with the HGTD as function of hard-scatter selection efficiency for different $R_{pT}$ selections. Furthermore, new and more sophisticated tracking, vertexing and track-vertex association selection using the ITk information are likely to be developed, also leading to improved pileup jet rejection. In general, the increased pileup jet rejection will in turn lead to further improvements in the $E_T^{\text{miss}}$ reconstruction, both on its resolution, and on the reduction of the tails.
The resolutions are shown as a function of the number of primary vertices in the event, $N_{PV}$, with MC statistical uncertainties. A selection criterion of $R_{pT} > 0.1$ is applied. The $R_{pT}$ is calculated from tracks with $|\eta| < 2.7$ (red) and $|\eta| < 4.0$ (black) that fulfil the quality requirements in Reference [56] and are required to have a transverse momentum larger than 1 GeV. The distance between the hard-scatter vertex and the $z_0$ impact parameter of the tracks used in the $R_{pT}$ calculation is required to be within 1 mm and 4 mm, depending on the $|\eta|$ of the track. The “Inclined Barrel” layout is described in Reference [56].

### 4.3 Benchmark physics performance

The following studies show the impact of the increased statistics, collision energy and upgraded detector on the sensitivity of different physics channels that depend directly on the performance of the LAr detector systems. The effects of an upgraded ATLAS detector are taken into account by applying energy smearing, efficiencies and fake rates to truth level quantities, following parameterizations based on detector performance studies with full simulation and HL-LHC conditions. As explained in section 4.1, most of the studies assume the use of the existing reconstruction techniques, extrapolated to $\langle \mu \rangle = 200$. In the case of $H \rightarrow \gamma\gamma$, where the performance depends significantly on the energy resolution, the impact of expected improvements is investigated through specific parameterizations.

#### 4.3.1 Higgs boson studies with the $H \rightarrow \gamma\gamma$ decay

The impact of the LAr calorimeter upgrade has been assessed in the $H \rightarrow \gamma\gamma$ decay channel using simulated $pp$ collisions at $\sqrt{s} = 14$ TeV.
Figure 4.13: The efficiency for pileup jets as a function of the efficiency for hard-scatter jets with $20 < p_T < 40$ GeV in the $2.4 < |\eta| < 3.8$ region using the $R_{\text{PT}}$ discriminant, in POWHEG+PYTHIA $tt$ events. The vertices are normally distributed along the beam axis and in time with $\sigma_z = 50$ mm, $\sigma_t = 180$ ps and $\langle \mu \rangle = 200$. The tracks used in the $R_{\text{PT}}$ calculation for the black curve fulfil the quality requirements in Reference [56] and are required to have a transverse momentum larger than 1 GeV. The distance between the hard-scatter vertex and the $z_0$ impact parameter of the tracks used in the $R_{\text{PT}}$ calculation is required to be within 1 mm and 4 mm, depending on the $|\eta|$ of the track. The blue curve is obtained using tracks matched to true charged particles from the hard scatter vertex. For the red curve, reconstructed tracks selected as for the black curve and with a timing consistent within 60 ps with the hard-scatter vertex are considered. The time resolution of the tracks is assumed to be 30 ps. The “Inclined Barrel” layout is described in Reference [56]. Jets are clustered using the anti-$k_T$ algorithm with $R=0.4$.

Performance of the diphoton reconstruction

For this study, the gluon-gluon fusion (ggF) production of the SM Higgs boson is modelled using the POWHEG-BOX-V2 event generator [57]. POWHEG-BOX uses the PDF4LHC NLO PDF set [58] and is interfaced to PYTHIA 8 [59] for showering and hadronization. The ggF Higgs boson production is accurate to next-to-next-to-leading order (NNLO) in QCD, using the POWHEG method for merging the next-to-leading order (NLO) Higgs boson plus jet cross section with the parton shower, and the MINLO method [60] to simultaneously achieve NLO accuracy for inclusive Higgs boson production.

A basic event selection is applied, requiring that events have at least two reconstructed photons passing the Loose identification working point [61] and with $p_T > 25$ GeV.

A key element of the $H \rightarrow \gamma\gamma$ analysis is the capability to reconstruct the $z$ position of the interaction vertex with good accuracy, in order not to degrade the diphoton invariant mass resolution. Due to its fine segmentation and its division in layers in depth, the ATLAS EM calorimeter has the unique ability to estimate this position of the vertex along $z$ using the photon clusters alone. This is reconstructed using the barycentres of the energy deposits in
Figure 4.14: Expected z-vertex resolution in events with two unconverted photons with the HL-LHC detector layout at \( \langle \mu \rangle = 0, \langle \mu \rangle = 200 \), and compared to that obtained in Run 2.

the first and second layers of the calorimeter, and is thus quite insensitive to pileup effects. Figure 4.14 shows the z-vertex resolution obtained at \( \langle \mu \rangle = 0, \langle \mu \rangle = 200 \), and in Run 2, for pairs of unconverted photons. The two reconstructed photon candidates with the largest \( E_T \) are considered and used to identify the diphoton primary vertex among all reconstructed vertices, using the pointing information from the calorimeter clusters and a constraint from the position of the beamspot. The plot shows only a modest degradation in vertex resolution measured using unconverted photons under HL-LHC conditions. The vertex resolution achieved, around 15 mm, ensures it has a negligible impact on the resolution of the reconstructed diphoton invariant mass.

Converted photons, which use track information in addition to pointing information obtained from the calorimeter cluster, achieve a better z-vertex resolution than unconverted photons. Their resolution will be even improved with the ITk upgrade. Compared to the existing detector, the upgraded layout has indeed less material, which leads to less multiple scattering, therefore the converted photons are expected to be measured more accurately. In summary, when combining both unconverted and converted photons together, a z-vertex resolution on par with what is achieved in Run 2 is expected at the HL-LHC.

Figure 4.15 shows the \( H \to \gamma\gamma \) invariant mass distributions in the Run 2 geometry and at HL-LHC, comparing several vertex selection techniques. It illustrates that the vertex selection using the photons information alone (Common \( \gamma\gamma \) vertex, described previously) gives an invariant mass resolution close to the ideal one obtained when using the true vertex position in the computation. Similarly to what is done in Run 2, the performance
can be slightly improved by using a neural network discriminant that uses, in addition, information on the tracks at the vertices (Selected vertex). Thus the invariant mass resolution is dominated by the photon energy resolution, and not the vertex position resolution, even at high pileup.

As explained in Section 4.2, the electron and photon energy resolution are expected to be improved through the use of improved reconstruction techniques, compared to what is in the current HL-LHC simulations. In order to study the impact of such possible improvements on the $H \rightarrow \gamma\gamma$ analysis, two scenarios called optimistic and pessimistic were implemented for the global constant term and the pileup contributions. The resulting resolution curves are then used to smear the photons true energy in the analyses. The optimistic scenario assumes that the high statistics at HL-LHC will provide the possibility to reduce the global constant term close to 0.7% which is its design value. The pessimistic scenario keeps the same constant term as estimated with 2015 data (1% in the barrel and 1.4% in the endcaps). Concerning the pileup noise, the pessimistic approach use the values extracted from full simulation with the current reconstruction algorithms while the optimistic assumes that offline corrections will reduce this noise to a value equivalent to $\langle \mu \rangle = 75$. The energy resolution smearing functions were separately parameterized for the barrel and endcap regions.

Figure 4.16 presents the reconstructed diphoton invariant mass obtained in Run 2, and expected with HL-LHC $\langle \mu \rangle = 0$ and $\langle \mu \rangle = 200$ in the two scenarios. Comparing the $\langle \mu \rangle = 0$ and $\langle \mu \rangle = 200$ curves, it shows that the high pileup degrades significantly the mass resolution with the Phase-II detector, down to 2.6 GeV in the pessimistic scenario, and...
2.0 GeV in the optimistic one. However this performance at $\langle \mu \rangle = 200$ in the optimistic case remains similar or slightly better than the one observed in Run 2, even though the noise term is still higher than the Run 2 one. Two effects then explain this good performance. At photon energies typical of $H \rightarrow \gamma \gamma$ events, both the noise and the constant terms are important, so the better constant term assumed in the optimistic scenario compensates partially the worse noise term. Second, the upgraded inner detector contains less material than the present one, so there are more unconverted photons, which have a better energy resolution than the converted ones.

**Differential cross section measurements**

A key analysis when investigating the behaviour of the SM Higgs is the measurement of fiducial differential cross sections. These describe the total rate of the process $pp \rightarrow H \rightarrow \gamma \gamma$ and its shape dependence with respect to various quantities relating to the Higgs kinematics, properties of the event and associated final state objects. This section provides an estimate of the expected sensitivity of the differential cross section measurement of the Higgs transverse momentum using the diphoton decay channel, $p_T^{\gamma \gamma}$, as a representative example. The selections, MC samples and methodology of the most recent Run 2 analysis [62] are utilized. An integrated luminosity of 3000 fb$^{-1}$, pileup of $\langle \mu \rangle = 200$ and centre-of-mass energy of $\sqrt{s} = 14$ TeV are assumed.

Signal yields are typically measured by performing an extended maximum likelihood fit to the diphoton invariant mass, $m_{\gamma \gamma}$ of selected events within a fit range of $m_{\gamma \gamma} \in [105, 160]$ GeV.
In order to estimate the statistical precision of the measurement, such a fit is performed on a toy dataset which is constructed using sensible parameterizations for the shapes of the expected signal peaks and the falling background spectra which are typically composed of non-resonant $\gamma\gamma$, $\gamma j$ and $jj$ events, in an approximate proportion of 80%, 20% and less than 5%, respectively. Simple systematic uncertainties on the unfolding and background modelling, based on the Run 2 analysis, are assumed.

The background rates expected at HL-LHC are obtained by scaling the Run 2 data sidebands using (i) the expected change in selection efficiencies of the $\gamma\gamma$, $\gamma j$ and $jj$ backgrounds when transferring between Run 2 and HL-LHC conditions and (ii) the relative contributions of these processes as measured using the data-driven double 2D sideband method as part of the Run 2 analysis. Aiming for a similar rejection of fake photons originating from hard-scatter jets (scale factor 1), the selection efficiency for real photons is expected to degrade at low energies, with a scale factor of 0.65 at $p_{T}^\gamma \sim 25$ GeV, while the Run 2 performance is recovered at higher energies (scale factor of 1.01 at $p_{T}^\gamma \sim 200$ GeV). The contribution from pileup is modelled using two scenarios: an optimistic scenario in which the scale factor is 1, meaning that the number of selected photons reconstructed from pileup objects does not change between Run 2 and HL-LHC, and a pessimistic scenario in which it scales linearly with the pileup, i.e. $\frac{200}{\mu\text{evt}}$. The pileup contribution to diphoton events is found to be negligible, therefore these scenarios only affect the amount of background $\gamma j$ and $jj$ events.

An additional bin at $p_{T}^{\gamma\gamma} \in [350, 600]$ GeV is included by extrapolating the predicted background yields using a MC-driven functional form. The background rates and shapes are modelled as a function of $m_{\gamma\gamma}$ by fitting the scaled sidebands with the functional forms used in Run 2. These rates are additionally scaled by a factor of 1.13 to account for the increase in cross section due to the change in centre-of-mass energy.

The expected signal shapes are obtained by smearing the energy of truth level photons according to the optimistic and pessimistic resolutions estimated for the upgraded detector. Events are selected according to the kinematic requirements and binned in $p_{T}^{\gamma\gamma}$. The signal shape is taken as a double-sided Crystal Ball function, the parameters for which are obtained from a fit to the diphoton invariant mass of the selected events in each bin. As has been shown, the primary vertex selection efficiency is high enough that the impact on the mass resolution is negligible.

The expected signal yields are obtained by scaling the Run 2 signal MC samples [62] according to the ratio of cross sections at $\sqrt{s} = 14$ TeV and $\sqrt{s} = 13$ TeV [63] and the expected change in signal selection efficiency. The change in the shape of the production cross section as a function of $p_{T}^{\gamma\gamma}$ is estimated to have an effect of less than 5% in all bins and is therefore neglected.

A simple scheme of systematic uncertainties is assumed. Three nuisance parameters are contained within the likelihood fit in order to describe the effects of Higgs mass, photon energy scale (PES) and resolution (PER) uncertainties on the signal shapes. These uncertainties are based on the Run 2 values in each bin of $p_{T}^{\gamma\gamma}$ and have a combined effect of 1 to
Table 4.1: Summary of expected uncertainties on the differential cross section measurement of the Higgs transverse momentum using the diphoton decay channel, $p_T^{\gamma\gamma}$ at HL-LHC assuming $\int \mathcal{L} dt = 3000 \text{fb}^{-1}$, $\langle \mu \rangle = 200$ and $\sqrt{s} = 14 \text{ TeV}$. Four scenarios are considered, labelled XY where $X, Y \in \{O, P\}$ represent whether optimistic or pessimistic pileup rejection and energy resolution, respectively, are assumed. Systematic uncertainties based on the Run 2 fiducial cross section measurement [62] are assumed. These are dominated by modelling uncertainties which will likely be reduced over time.

<table>
<thead>
<tr>
<th>Bin of $p_T^{\gamma\gamma}$ [GeV]</th>
<th>Fit stat.</th>
<th>Fit syst.</th>
<th>Other syst.</th>
<th>Total</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>OO</td>
<td>PO</td>
<td>OP</td>
<td>PP</td>
</tr>
<tr>
<td>[0, 20]</td>
<td>3.7 %</td>
<td>3.9 %</td>
<td>4.8 %</td>
<td>5.1 %</td>
</tr>
<tr>
<td>[20, 30]</td>
<td>5.5 %</td>
<td>5.6 %</td>
<td>7.2 %</td>
<td>7.4 %</td>
</tr>
<tr>
<td>[30, 45]</td>
<td>5.2 %</td>
<td>5.6 %</td>
<td>6.8 %</td>
<td>7.3 %</td>
</tr>
<tr>
<td>[45, 60]</td>
<td>6.1 %</td>
<td>6.4 %</td>
<td>7.8 %</td>
<td>8.3 %</td>
</tr>
<tr>
<td>[60, 80]</td>
<td>6.2 %</td>
<td>6.8 %</td>
<td>8.0 %</td>
<td>8.8 %</td>
</tr>
<tr>
<td>[80, 120]</td>
<td>4.8 %</td>
<td>5.2 %</td>
<td>6.0 %</td>
<td>6.6 %</td>
</tr>
<tr>
<td>[120, 170]</td>
<td>4.1 %</td>
<td>4.7 %</td>
<td>5.0 %</td>
<td>5.7 %</td>
</tr>
<tr>
<td>[170, 220]</td>
<td>4.8 %</td>
<td>5.6 %</td>
<td>5.6 %</td>
<td>6.6 %</td>
</tr>
<tr>
<td>[220, 280]</td>
<td>5.6 %</td>
<td>5.8 %</td>
<td>6.5 %</td>
<td>6.7 %</td>
</tr>
<tr>
<td>[280, 350]</td>
<td>6.9 %</td>
<td>7.1 %</td>
<td>7.8 %</td>
<td>8.1 %</td>
</tr>
<tr>
<td>[350, 600]</td>
<td>7.6 %</td>
<td>8.3 %</td>
<td>8.5 %</td>
<td>9.4 %</td>
</tr>
</tbody>
</table>

2% on the signal yields. All other systematic uncertainties are assumed to be equal to those in the Run 2 inclusive fiducial volume, taken as background modelling (3.7%), luminosity (3.2%), pileup (1.1%), photon reconstruction (1.8%) and theoretical modelling (4.2%). The combined effect of those systematic uncertainties not accounted for in the signal extraction is 6.8%. Note that the dominant uncertainties due to background and theoretical modelling are expected to be reduced over time, and so this 6.8% is likely pessimistic for the HL-LHC analysis.

A summary of the expected uncertainties is shown in Table 4.1 and the resulting sensitivity on the cross sections is shown in Figure 4.17. The statistical-only case can be interpreted as the best possible sensitivity, achievable by reducing all systematic uncertainties to zero. When optimistic pileup and resolution are assumed, the measurement is systematically limited in all bins and would benefit from a reduction in modelling uncertainties. The total uncertainty, about a factor four smaller than that of the Run 2 measurement, has a similar precision than the current state-of-the-art theoretical calculations. Assuming pessimistic scenarios increases the statistical uncertainty by 1.4 to 2.6% relative to the measured cross sections. Compared to the Run 2 measurement, the higher statistics allows to probe much larger Higgs boson transverse momenta, allowing more stringent tests of anomalous Higgs boson interactions far above the electroweak scale.
4.3.2 Di-Higgs analysis in the $bb\gamma\gamma$ channel

One of the most promising channels to measure the Higgs self-coupling is the $HH \rightarrow b\bar{b}\gamma\gamma$ final state. This channel profits from a clean $HH$ signal extraction thanks to the narrow mass peak of the $H \rightarrow \gamma\gamma$ decay and two isolated b-jets. Both photons and b-jets are preferentially produced in the central part of the detector; however its low branching ratio (0.26%) associated with a $HH$ cross section of 39.6 fb \(^{[63]}\) and a selection efficiency below 5% requires to analyse the full HL-LHC statistics to reach a significance above 1. A recent study \(^{[64]}\) based on truth level particles convoluted with resolution and efficiency smearing functions computed for $\langle \mu \rangle = 200$ has shown an efficiency of $2.85 \pm 0.01\%$ (approximately 10 selected signal events with $3000 \text{ fb}^{-1}$) and an expected contamination from jets+$H \rightarrow \gamma\gamma$ ($t\bar{t}H, b\bar{b}H, ggH, ZH$) and continuum background ($b\bar{b}\gamma\gamma, b\bar{b}j\gamma, c\bar{c}\gamma\gamma, jj\gamma\gamma, \ldots$) of roughly 16 and 75 events respectively.

This section presents updated results obtained with the improved photon energy resolutions described in Section 4.3.1. The previous study obtained a diphoton mass resolution of
around 2.7 GeV, due to a detector layout with more material in the inner tracker, and the use of electron resolution curves to parameterize the photon resolutions. Table 4.2 displays the updated diphoton mass resolutions for the $H \rightarrow \gamma\gamma$ events coming from gluon-gluon fusion (ggF) or double Higgs production. The better resolution in double Higgs events comes from the harder photon $p_T$ spectrum than in gluon fusion single Higgs events.

Table 4.2: Diphoton mass resolutions in GeV for $H \rightarrow \gamma\gamma$ coming from gluon fusion or double Higgs events for the two energy resolution scenarios.

<table>
<thead>
<tr>
<th>Resolutions [GeV]</th>
<th>ggF</th>
<th>HH</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pessimistic</td>
<td>2.64</td>
<td>2.06</td>
</tr>
<tr>
<td>Optimistic</td>
<td>1.99</td>
<td>1.62</td>
</tr>
</tbody>
</table>

The cut flow used in the previous study has not been modified, except for minor updates to the parameterization of other discriminating variables (e.g. $b$-tagging, etc.). The events are required to contain a pair of high-$p_T$ photons ($p_T > 30$ GeV) and a pair of jets with $p_T > 30$ GeV passing a $b$-tagging requirement. Isolation and angular cuts are applied to select the di-Higgs topology. The photon and the $b$-jet pairs must have invariant masses compatible with the Higgs mass within the resolution. Finally, events are categorized depending on the $|\eta|$ positions of the photons.

Figure 4.18 displays the updated diphoton mass resolution after the event selection, except for the application of the diphoton invariant mass cut. As a consequence of the narrower mass peak, this mass window could be reduced from 6 to 4 GeV. As shown in Table 4.3, the expected number of events from the continuum background is thus reduced by a factor 1.4 while the impact is within 10% for the $HH$ and single-$H$ events. As a result, a gain in significance of 23% is achieved between the previous study and the optimistic scenario. The limits on the Higgs boson self-coupling at 95% CL are improved by 18%. The 95% CL upper limit on the cross section is shown in Figure 4.19.

4.3.3 Search for a $Z' \rightarrow ee$ resonance

High mass dilepton resonances, predicted by a number of phenomenological models, would be a spectacular and clear sign of new physics beyond the SM. The large integrated luminosity of the HL-LHC (3000 fb$^{-1}$) will statistically yield more collisions at high $Q^2$, and thus will increase the reach for such resonances. For a high mass resonance decaying to two electrons, the performance of the LAr calorimeter has a direct impact on the dielectron invariant mass resolution, which in turn dictates the search sensitivity. As explained in Chapter 3, more stringent requirements on the dynamic range and on the linearity of the electronics than those of the existing system must be met to obtain a good sensitivity at high
Figure 4.18: Diphoton invariant mass distribution of expected signal and background contributions after applying all other selection cuts. The continuum is split in $b\bar{b}\gamma\gamma$, 'Reducible' background ($b\bar{b}j\gamma$, $b\bar{b}jj$, $c\bar{c}\gamma\gamma$, $c\bar{c}j\gamma$) and ‘Others’ ($t\bar{t}, \gamma\gamma Z$).

Table 4.3: Expected numbers of events after event selection for 3000 fb$^{-1}$, significances and limits at 95% CL on $\lambda_{HHH}/\lambda_{SM}^{HHH}$.

<table>
<thead>
<tr>
<th>Channel</th>
<th>Previous study $\pm$</th>
<th>Pessimistic $\pm$</th>
<th>Optimistic $\pm$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Events $HH$</td>
<td>9.54 ± 0.02</td>
<td>9.28 ± 0.02</td>
<td>10.75 ± 0.03</td>
</tr>
<tr>
<td>Events Single-$H$</td>
<td>15.74 ± 0.41</td>
<td>14.05 ± 0.39</td>
<td>16.56 ± 0.45</td>
</tr>
<tr>
<td>Events Continuum</td>
<td>75.08 ± 2.02</td>
<td>58.76 ± 2.12</td>
<td>58.76 ± 2.12</td>
</tr>
<tr>
<td>Significance</td>
<td>1.05 ± 0.03</td>
<td>1.13 ± 0.02</td>
<td>1.29 ± 0.02</td>
</tr>
<tr>
<td>$\lambda_{HHH}/\lambda_{SM}^{HHH}$ @ 95% CL</td>
<td>[-0.8, 7.7]</td>
<td>[-0.4, 7.3]</td>
<td>[-0.1, 7.1]</td>
</tr>
</tbody>
</table>
masses. The energy resolution of high energy electrons is dominated by the constant term of the calorimeter resolution (see equation 4.1), which depends on the precise knowledge of non-uniformities, and is expected to be improved through more precise calibrations at HL-LHC. As the energy resolution of electrons is much better than that of muons at high-$p_T$, exclusion and discovery limits for this search are more stringent in the electron than in the muon channel.

The study presented here summarizes the prospects for the exclusion reach for a $Z'$ boson decaying into two electrons as predicted by the Sequential Standard Model (SSM) [65]. The most stringent exclusion limits on the mass of a $Z'_\text{SSM}$ boson to date come from the ATLAS search based on 36.1 fb$^{-1}$ of $\sqrt{s}=13$ TeV data and sets a 95% confidence level (CL) lower limit on the SSM $Z'$ mass of 4.1 TeV for the combined $ee$ and $\mu\mu$ channels [66].

The dominant background in this search arises from Drell-Yan (DY) production. This process was simulated using the next-to-leading-order (NLO) POWHEG-Box [57] event generator, implementing the CT10 [67] parton distribution function (PDF), in conjunction with PYTHIA 8.186 [59] for event showering, and the ATLAS AZNLO set of tuned parameters [68]. The DY event yields are corrected for higher-order EW and QCD effects with a rescaling that depends on the dielectron invariant mass, leading to corrections of the order of 15% at 3 TeV. More details are given in Reference [69]. Other backgrounds originate from top-quark and diboson ($WW$, $WZ$, $ZZ$) production. For dielectron invariant masses above around 2 TeV, the contribution from top-quark production is negligible, due to the boost of the top-quarks at high energies. The contribution from diboson production is not considered in this analysis as the impact of these processes on the limit is negligible at high $m_{ee}$. The effect of reducible
background arising from $W$+jets and multijet events in which one or more jets satisfy the electron selection criteria is not included in the study. The SSM signal $Z' \to ee$ was generated at leading-order (LO) in QCD using PYTHIA 8.186 \cite{59} with the NNPDF23LO PDF set \cite{70} and the ATLAS A14 set of tuned parameters \cite{71} for event generation, parton showering and hadronization. The $Z'_{SSM}$ boson is assumed not to couple to the SM $W$ and $Z$ bosons and interference between the $Z'$ boson and the SM $Z$ boson production amplitudes is neglected. Higher-order QCD corrections were computed with the same methodology and applied as for the DY background.

The event selection is similar to the one developed for Run 2 \cite{66}. The events have to be accepted by the single electron trigger which requires at least one electron with transverse momentum $p_T > 22 \text{ GeV}$ in $|\eta| < 2.5$. Events are required to contain exactly two electrons fulfilling the medium identification working point and have $p_T > 25 \text{ GeV}$ in $|\eta| < 2.47$ excluding $1.37 < |\eta| < 1.52$. The electrons are reconstructed and identified as detailed in Section 4.2.

The resulting dielectron invariant mass spectrum ($m_{ee}$) is shown in Figure 4.20(a) for the DY background as well as for an example $Z'$ boson with a mass of 5 TeV. The statistical analysis is performed for the search for a $Z'_{SSM}$ boson using the $m_{ee}$ distribution. The same methodology is used as in the Run 2 analysis which uses a Bayesian analysis \cite{72}. Upper limits on the cross section for producing a $Z'_{SSM}$ boson times its branching ratio ($\sigma \times BR$) are computed at the 95% CL as a function of the $Z'_{SSM}$ boson mass. The 95% CL

![Figure 4.20: (a) Invariant mass distribution for events satisfying all selection criteria in the dielectron channel. The expected background is shown together with a SSM $Z'$ boson with a mass of 5 TeV. (b) Observed (solid black line) and expected (dashed black line) upper limits on cross section times branching ratio ($\sigma \times BR$) as a function of the SSM $Z'$ boson mass in the dielectron channel. The 1$\sigma$ (green) and 2$\sigma$ (yellow) expected limit bands are also shown. The predicted $\sigma \times BR$ for SSM $Z'$ production is shown as a black line. The vertical dashed line indicates the observed mass limit of the ATLAS Run 2 results using 36.1 fb$^{-1}$ of $\sqrt{s} = 13$ TeV data \cite{66}.](image-url)
upper limits on $\sigma \times BR$ as a function of the $Z'_{\text{SSM}}$ mass are shown in Figure 4.20(b). Using 3000 fb$^{-1}$ of data and neglecting the effect of systematic uncertainties, $Z'_{\text{SSM}} \rightarrow ee$ bosons can be excluded up to masses of 6.4 TeV. A similar analysis in the dimuon channel yields a limit which is optimistic since it assumes looser identification criteria compared to the Run 2 analysis. The limit obtained in this channel is 0.2 TeV less stringent as the calorimeter resolution is around 1% for very high-\(p_T\) electrons, while the momentum resolution of the combined ITk and muon spectrometer track is around 7 to 8% for muons with \(p_T = 1\) TeV [73]. Combining the two channels improves the mass limits to 6.6 TeV. This improves the limits by 2.5 TeV compared to the current Run 2 limits [66].

Discovery limits have also been computed using a cut and count method within $\pm 2\sigma$ around the mass peak. In the muon channel the discovery reach is up to 5.2 TeV, while in the electron channel a $Z'_{\text{SSM}}$ boson with masses up to 5.9 TeV can be discovered at the HL-LHC, thanks to its much better resolution. The reach is about 900 GeV higher than that with 300 fb$^{-1}$ of data.

### 4.3.4 Search for $t\bar{t}$ resonances

Several theories of physics beyond the SM predict new particles with masses at the TeV scale that decay primarily to a $t\bar{t}$ pair. A $t\bar{t}$ resonance search is a benchmark analysis for evaluating physics prospects at the HL-LHC. The calorimeter plays a major role in the computation of the $t\bar{t}$ invariant mass, through the accurate determination of the jets' energies and masses, of the electron energies, and of the $E_T^{\text{miss}}$. For a high mass resonance, the products of the hadronic decay of a top quark are typically inside a single boosted jet, whose transverse momentum is then of several TeV. Therefore, similarly to the $Z' \rightarrow ee$ case discussed in Section 4.3.3, meeting the requirements on the dynamic range and on the linearity of the calorimeter cells is necessary to keep a good sensitivity at high mass. In addition, a good energy resolution per cell is necessary to perform the pileup mitigation techniques, such as trimming, which allow to probe the substructure of jets from top quark decays.

A $t\bar{t}$ resonance would cause a local excess or deficit in the $t\bar{t}$ mass spectrum as predicted by the SM. A search for such a deviation is performed using $t\bar{t}$ pairs selected from events in Monte Carlo simulations of $pp$ collisions with a centre of mass energy of 14 TeV, for a total integrated luminosity of 3000 fb$^{-1}$ [74]. The search is performed in the semi-leptonic decay channel: both top quarks decay to a $b$-quark and a $W$ boson; one $W$ decays to two quarks and the other decays to a lepton and a neutrino ($t\bar{t} \rightarrow WbWb \rightarrow \ell v qq'$).

A Topcolour model containing a spin-1 $Z'$ boson is used as a benchmark signal [75–77]. The signal simulation $pp \rightarrow Z' \rightarrow t\bar{t}$ was done with PYTHIA 8 [59], assuming a signal width of 1.2%, and using the A14NNPDF23LO PDF set. The main background is SM $t\bar{t}$ production which was generated using POWHEG+PYTHIA [57], the CT10 PDF set and setting the $hdamp$ parameter to the top mass. NNLO cross sections were used [78]. $W+$ jets and $Z+$ jets were generated with SHERPA [79] (merged Matrix Element+Parton shower, matched and merged
for 0 to 4 additional QCD partons in LO), using the CT10 PDF set [79]. Single top production was generated by A**MC+PYTHIA** [80]. The cross sections were scaled to NNLO except single top which was NLO [81, 82].

The effects of an upgraded ATLAS detector are taken into account by applying energy smearing, efficiencies and fake rates to truth level quantities, following parameterizations based on detector performance studies with full simulation and HL-LHC conditions.

Events are required to have exactly one electron (or muon) passing $p_T > 30$ GeV (25 GeV) and $|\eta| < 2.5$, which is well identified and isolated. There must be missing transverse momentum $E_T^{\text{miss}} > 20$ GeV and $E_T^{\text{miss}} + m_T(W) > 60$ GeV, where $m_T(W)$ is the transverse mass of the lepton plus $E_T^{\text{miss}}$ system. Events must contain at least one jet that was identified as containing a $b$-hadron by the MV1 $b$-tagging algorithm. These cuts are applied with the aim of suppressing the reducible backgrounds, the largest of which is $W+$jets. Events are separated into topological decay channels: boosted and resolved. The top quark which decays hadronically is referred to as $t_{\text{had}}$, and the top quark which decays leptonically is referred to as $t_{\text{lep}}$. Events are further separated into different channels depending on whether the single lepton is an electron or a muon. In a boosted event, all the decay products of $t_{\text{had}}$ are detected inside one trimmed anti-$k_t$ large-R jet of radius 1.0, passing $p_T > 300$ GeV and $|\eta| < 2.0$. For high-mass $Z'$ events, the typical energy resolution for these boosted jets is around 8%. In a resolved event, the jet decay products of $t_{\text{had}}$ and $t_{\text{lep}}$ are detected as well separated small-R jets. Thus the four channels are boosted electron, resolved electron, boosted muon and resolved muon; these are recombined for the limit setting procedure.

The invariant mass of $t\bar{t}$ pairs is reconstructed for the events selected as consistent with a semi-leptonic $t\bar{t}$ decay, employing kinematic reconstruction techniques to estimate the $p_z$ component of the neutrino in the $W$ leptonic decay, and to sort out the combinatorics in the resolved channels. Systematic uncertainties based on the ones from the Run 1 analysis are used [83].

Figure 4.21 shows the expected distributions for the signal and the SM backgrounds with 3000 fb$^{-1}$ of data at $\sqrt{s} = 14$ TeV in the boosted channels, which are the most sensitive ones for high $Z'$ boson masses. The corresponding expected limits are displayed in Figure 4.22, compared for $\mathcal{L} = 300$ fb$^{-1}$ and $\mathcal{L} = 3000$ fb$^{-1}$.

The high luminosity of the HL-LHC extends the sensitivity by 1 TeV.

### 4.4 Trigger performance

As mentioned in Chapter 3, the LAr system is expected to provide full granularity information to the new Global Event trigger processors, for cells above some energy threshold. This, combined with the high computing capabilities of the Global Event processors, provides significant gain in trigger performance: this hardware trigger level can use reconstruction techniques and compute shower shape variables which are currently used at the HLT or in...
Figure 4.21: The reconstructed mass spectrum of $t\bar{t}$ pairs selected from signal and background events for a luminosity of 3 000 fb$^{-1}$ in the more sensitive boosted electron (a) and muon (b) channels. The cross sections of the signal samples, $Z'$ (2 TeV) and $Z'$ (3 TeV), are multiplied by 50 for visibility.

Figure 4.22: Expected upper limits set on the cross section $\times$ branching ratio of the Topcolour $Z'$ boson for masses 1 to 7 TeV, with 300 fb$^{-1}$ (a) and 3 000 fb$^{-1}$ (b) of simulated $pp$ collisions at $\sqrt{s} = 14$ TeV. The limit observed in the Run 1 analysis [83] is also displayed for comparison as a vertical dashed line.
offline reconstruction. This allows trigger rates to be significantly reduced while keeping high efficiencies. The following sections describe briefly some of the expected improvements for electrons, jets and $E_T^{\text{miss}}$ triggers. Detailed studies will be available in the Phase-II TDAQ TDR which is in preparation.

### 4.4.1 Electron reconstruction at L0

The Phase-I upgrade will provide the ability to use some shower shape in the reconstruction of electrons by the trigger system. The Global Event processors being developed for the Phase-II upgrade to the trigger and data acquisition system will make it possible to further improve the electron reconstruction performance at the trigger level by providing the ability to calculate new shower shape variables. Two of these shower shape variables particularly important in the reconstruction of electrons are the variables called $R_\eta$ and $E_{\text{ratio}}$. The variable $R_\eta$ describes the transverse shape of the bulk of the electron clusters, and is defined as the ratio of the energy in $3 \times 2$ cells to the energy in $7 \times 2$ cells centred at the electron cluster position, as measured in the middle layer of the EM calorimeter. It can already be computed with good accuracy after the L1 trigger upgrade in Phase-I using Super Cells, which sum 4 cells in the $\phi$ direction. The variable $E_{\text{ratio}}$ describes the transverse structure of the early energy deposits, using the fine segmentation in $\eta$ of the first layer of the EM calorimeter, to separate clusters which are made of several close-by showers. Considering the two local maxima of the energy distribution in the first layer, $E_{\text{ratio}}$ is defined as the ratio of their difference over their sum. As the full granularity of the first layer of the calorimeter is necessary to compute the $E_{\text{ratio}}$ variable, it can only be used in the L0 trigger by the Global Event processors.

Figure 4.23 shows the discrimination power between electrons and jets provided by the two variables $R_\eta$ and $E_{\text{ratio}}$. The distribution of $E_{\text{ratio}}$ is plotted after a cut on $R_\eta$ has been applied, with threshold chosen to provide 99% efficiency. Even at $\langle \mu \rangle = 200$, these two variables alone provide a powerful and complementary discrimination between electrons and jets. While the variable $R_\eta$ provides the ability to reduce contamination from charged pions, the variable $E_{\text{ratio}}$ reduces the neutral pion background.

Figure 4.24 shows the ROC curve obtained for cutting on $E_{\text{ratio}}$ in the Global Event processors. With threshold cut values chosen to achieve an electron identification efficiency of 98%, a fake acceptance of about 35% would be achieved. Figure 4.24 also shows the impact of cutting out cells with energy below a threshold defined as a multiple integer of the expected noise. Excellent efficiency and rejection is obtained even when considering only cells with energy above $2\sigma$ of the noise in the computation of $E_{\text{ratio}}$. The impact of this requirement on the bandwidth requirement between the LASP and the Global Event processors is discussed below in Chapter 8.

The additional rejection of the jet background achieved by a cut on $E_{\text{ratio}}$ while keeping a very high electron identification efficiency translates into a reduction of trigger rates by a
Figure 4.23: Distributions of $R_\eta$ (a) and $E_{\text{ratio}}$ (b) variables for electrons and jets at the HL-LHC with $\langle \mu \rangle = 200$. The $E_{\text{ratio}}$ distribution is shown after a cut of $R_\eta$ with an 99% efficiency.

Figure 4.24: Electron efficiency vs jet fake efficiency of cut on $E_{\text{ratio}}$ in the L0 trigger system obtained by considering cells in the first layer of the calorimeter with absolute energy deposited larger than an integer number of the total noise in the cell.
factor about 3 at a given energy threshold, on top of the reduction by a factor two from the cut on $R_H$. At a fixed trigger rate of 200 kHz, the $E_{\text{ratio}}$ cut at the Global Event processors level allows therefore to lower the trigger threshold by about 7 GeV.

### 4.4.2 $E_{\text{miss}}^T$ reconstruction at L0

The current L0 trigger system designed for Phase-II foresees the ability to reconstruct topological clusters (topoclusters) in Global Event processors, which can then be used to reconstruct jets and $E_{\text{miss}}^T$. Topoclustering algorithms are defined by two energy thresholds, defined relatively to the noise level of the calorimeter cells. The first threshold is used to find seeds for the clusters, while the second is used to add to the clusters all nearby cells which satisfy it. Hence, transmitting all cells with absolute energies larger than 2 times the noise to the Global Event system allows to run a so-called "42" topoclustering algorithm, where all cells with absolute energies above 4 times the noise are used to seed clusters, which are then augmented by all nearby cells with absolute energies above 2 times the noise.

Figure 4.25 shows a comparison of the performance of several $E_{\text{miss}}^T$ reconstruction techniques at trigger level, using as a benchmark the turn-on curves obtained from a $ZH \rightarrow \nu\bar{\nu}b\bar{b}$ signal for a fixed trigger rate of 50 kHz at $\langle \mu \rangle = 200$.

Compared to the “42” topoclustering algorithm which has been described above, the “420” algorithm adds an additional outer layer of cells to the cluster. It is the algorithm currently used in the offline reconstruction of three-dimensional topological calorimeter clusters. This algorithm cannot run in the Global Event processors as the energy of all calorimeter cells will not be available, and is actually performing worse than the “42” algorithm since the last layer of cells added to the topoclusters increase significantly the pileup noise. The “jTowers” are $0.1 \times 0.1$ trigger towers formed using Super Cells that will be available after the Phase-I LAr Calorimeter electronic upgrade (see Section 2.4); these towers will be used by the Jet Feature Extractor (jFEX) [4] in order to identify jets and $\tau$ candidates using finer granularity than that available in Run 2. The reconstruction of missing transverse momentum based on the jTowers in the simulations used in this study, uses an algorithm similar to what is used in the Run 2 calorimetry trigger.

Figure 4.25 shows that the reconstruction of $E_{\text{miss}}^T$ based on “42” topological clusters reconstructed in the Global Event processors, offers a significant performance improvement compared to the other $E_{\text{miss}}^T$ reconstruction methods available in the first trigger level. Thanks to the good pileup suppression of the “42” topoclustering, full efficiency is reached about 50 GeV earlier than $E_{\text{miss}}^T$ triggers based on Super Cells for a fixed trigger rate of 50 kHz. The turn-on is also sharper, demonstrating that the $E_{\text{miss}}^T$ reconstruction based on the “42” topoclusters has a better resolution. More detailed results will be available in the Phase-II TDAQ TDR which is in preparation.
4.4.3 Jet reconstruction at L0

The improvements expected for the jet triggers at L0 are twofold. First, similarly to the $E_T^{\text{miss}}$ trigger, the use of topoclustering techniques is expected to improve significantly the jet energy resolution, leading to sharper turn-on curves.

Independently of the clustering technique, the availability of the full FCal granularity has been shown by preliminary studies to improve significantly the performance of forward jet triggers, which are important for analyses targeting vector boson fusion (VBF) topologies.

Results of detailed studies will be available in the Phase-II TDAQ TDR which is in preparation.
Part II

Implementation
This chapter is an abbreviated summary of chapters 6 to 11, which contain the in-depth technical discussion of the LAr upgrade project. A concise overview the Phase-II implementation is shown in Figure 5.1, a schematic diagram of the Phase-II readout architecture for the LAr calorimeters. The path during data-taking of the electronic signals from the ionization pulse in the calorimeter cells through the trigger and read-out systems are indicated by the arrows. The LAr Trigger Digitizer Boards (LTDB) and the LAr Digital Processing System (LDPS) will already be installed in the Phase-I upgrade and remain operational in the HL-LHC phase to provide Super Cell information to the trigger system.

On-detector, new readout Front-end Boards, abbreviated FEB2, and Calibration Boards (top-left of the figure) will be installed. The FEB2s receive the signals from the calorimeter cells and perform analog processing, including amplification, shaping and a split into two overlapping linear gain scales. Both gain scales are digitized by an ADC, and this digital signal is multiplexed and sent off detector optically. This requires several ASICs, as well as clock and control functionality. The Calibration Boards inject accurate calibrated signals directly to the calorimeter cells.

Off-detector, the new LAr Signal Processor Boards (top-right of the figure) will be installed, providing the signals to the trigger and DAQ systems. The LAr Signal Processor Boards receive the full, digitized data stream from the FEB2s and apply digital filtering to the signals of each LAr calorimeter cell. This is accomplished by an FPGA and allows the determination of calibrated cell energies and signal times with respect to the bunch crossing time (including an active correction of out-of-time pileup). The data are then buffered until a trigger accept signal is received. On a trigger accept the data are sent to the data acquisition (DAQ) system. Finally, this chapter summarizes the power supplies and power distribution on the detector, the Detector Control System (DCS) and the plans for the installation and commissioning of the new electronics.

Readers who are interested mainly in an overview of the LAr upgrade programme are invited to read this summary chapter and skip the technical chapters. Those readers who are interested in the technical details may instead choose to skip this chapter. The following sections follow the order of the technical chapters, starting with the calibration and front-end electronics, and concluding with the installation and commissioning.
Figure 5.1: Schematic block diagram of the LAr calorimeter readout architecture for the Phase-II upgrade. The LAr Trigger Digitizer Board (LTDB) and LAr Digital Processing System (LDPS) will have been installed in the Phase-I upgrade.
5.1 Front-end electronics

The front-end electronics for the Phase-II upgrade consist of two types of boards, one type for readout (FEB2) and the other type for the calibration of the electronics. Both types of boards will be installed in the existing front-end crates (FECs) situated on the LAr calorimeter cryostats. The front-end readout is uniform for all calorimeter sections, apart from the HEC, where the preamplifier signals require a dedicated treatment.

5.1.1 Calibration

The calibration boards [84] are used to inject accurate calibrated signals directly in the liquid argon onto the calorimeter cells. The use of fast shaping for the ATLAS calorimeter implies the need to distribute the calibration signal directly at the input of the detector cell, and not at the input of the preamplifier located outside the cryostat, except in the forward calorimeters for which the signals are sent directly to the input of the FEB2. In order to avoid any active element in the cryostat, a voltage-driven system was chosen for the present calibration board. Since no changes are foreseen inside the cryostat, a similar approach will be used for the new calibration board.

The calibration board aims to produce a pulse with shape as close as possible to the ionization pulse generated by electromagnetic showers in the detector. While the latter is to first order a triangular pulse, described by the typical drift time in the LAr gap, the difficulty of generating a true triangular pulse with an electronic circuit originally led to the choice to produce an exponential pulse, the decay time of which was trimmed to approximate as much as possible the desired triangular shape, at least in the initial portion of the pulse [84]. Even after this optimization, the residual difference in shape between the physics-induced ionization pulse and the calibration pulse needs to be corrected; this can be done by directly measuring the calibration pulse properties and using them in the electronic calibration procedure [85]. The new calibration board will produce an exponential pulse with properties comparable to the current ones, assuming that the electronic calibration procedure could proceed as in Run 1 and Run 2.

Based on the experience with the present system and the new preamplifier needs, some of the requirements of the calibration system are revisited, while the overall design remains quite similar to the existing one. More specifically, the integral non-linearity of the calibration output needs to be better than 0.1% to correct the FEB2 response accurately, the uniformity between channels needs to be better than 0.25%, and the calibration pulse rise time needs to be below 1 ns.

With the exception of the HEC cold preamplifiers, all preamplifiers will have to be replaced for Phase-II in order to avoid saturation (see Chapter 7). To calibrate over the necessary dynamic range, the calibration system should therefore deliver pulses of at least 7.5 V, for which the standard CMOS technologies (e.g. 65 or 130 nm) can not be used, since they...
are limited to 3.3 V. The proposed alternative is an HV-CMOS technology to implement a high-frequency switch ASIC.

The present calibration board uses one 16-bit DAC ASIC whose voltage is distributed on the PCB to 128 switches. In order to keep an excellent output uniformity across the board, the layout of the signals is quite complex, and a different implementation is proposed, integrating one DAC per channel in the new calibration board ASIC, integrated with the high-frequency switch.

The experience with the current calibration board has shown that, even if the DAC input is set to zero, an output signal is observed due to the unavoidable parasitic couplings on the fast transistors used in the switch to select the channel or build the exponential signal. Any inductive path between the two transistors can produce a resonant behaviour on the circuit resulting in a ringing oscillation superimposing on the output pulse especially important at small DAC values.

The XFAB XT018 (180 nm) technology \[86\] is chosen to realize the calibration board ASIC, since it is the only HV-CMOS technology readily available to the ATLAS Collaboration. The feasibility of realizing a high-frequency switch satisfying the requirements discussed above was studied with simulation of the basic structure of the circuit, and assuming different scenarios for the parasitic connection between the switch transistors.

Following the results of simulation, variants of high-frequency switches will be integrated to study the ringing effect in different configurations. The same structures will be used to establish the radiation hardness of the XFAB XT018 technology in irradiation campaigns planned in 2018. In parallel to the ongoing developments with the chosen technology, alternative HV-CMOS technologies are being investigated as a contingency in case the XFAB XT018 process fails to qualify in terms of radiation hardness. In addition, studies are planned to assess the possible alternative calibration approaches using non-HV ASIC technology, should no viable alternative HV-CMOS be found.

Pending the successful results of the switch and DAC test, a complete channel design is scheduled for the end of 2018, with a submission at the beginning of 2019 and a prototype board integrating a small number of channels available for testing from Summer 2019. We consider the possibility of needing of an iteration in the design of the 16-bit DAC, which would result in a delay of 6 to 9 months in the schedule.

Finally, the current board includes eight delay chips with 1 ns steps originally envisioned to be used to correct for differences in cable lengths and to perform the so-called “delay” runs used to measure the calibration pulse waveform. However, in the current system, the Trigger, Timing, and Control (TTC) distribution system is used for the delay calibration runs. The IpGBT system will replace the TTC system, and the delay capabilities of the new system are similarly planned to be employed instead of a dedicated functionality on the calibration board.
5.1.2 Front-end readout board

The front-end readout electronics will be implemented on a new Front-end Board, abbreviated FEB2, that will replace the current FEB boards. As with the current FEBs, each FEB2 will handle 128 calorimeter channels, with a total of 1524 FEB2 boards required to read out the entire LAr system.

For each FEB2 board, two input connectors bring 64 calorimeter signals each from the crate baseplane to the FEB2 board. Preamplifier/shaper ASICs each handle four (or possibly eight) channels, terminating the input lines, and performing analog processing on the signals, including amplification, splitting into two overlapping linear gain scales, and applying a $CR-(RC)^2$ shaping function. Subsequently, octal ADC chips digitize both of the two gain-scale preamp/shaper outputs for four channels each. The ADCs operate at the bunch crossing frequency of 40 MHz and format their outputs, including eight digitized signal streams as well as one word with bunch crossing identification (BCID) information, into 16-bit words and output them serially at 640 Mbps. Serializer chips then receive 14 streams of ADC outputs, and serialize the digital data with a standard protocol into a single bit-stream at 10.24 Gbps. Finally, the serial outputs are converted from electrical to optical signals and transmitted off-detector using optical modules. In addition to the readout dataflow, functionality is provided to distribute clock and control information, and form the analog sums for use in the trigger system.

Analog processing

Analog processing is performed in two steps: the preamplifier provides an active termination of the input cables and amplifies the calorimeter signals, which have a dynamic range of up to 16 bits. The second stage (shaper) has two purposes: first to transform the output of the preamplifier circuit to a multi-gain differential output capable of directly driving the input to the ADC, and second, to add at least one stage of shaping to match the desired signal processing requirements. If required, multiple equivalent shaping stages can be added at a minimal cost in power. The baseline solution is to adopt the same $CR-(RC)^2$ shaping as the current system, but with the shaping time adjusted to account for the increased pileup expected at the HL-LHC.

Both the preamplifier and the shaper will be implemented in a single ASIC. The preamp/shaper ASIC is expected to accommodate either four or eight calorimeter channels. In addition to the signal amplification and shaping, some “peripheral” circuits are needed, such as a test pulse generator, bias circuit, temperature sensor and configuration registers. A configurable summing circuit will provide Super Cell signals to the LAr Trigger Digitizer Boards (LTDB) which will be installed during the Phase-I upgrade (see Section 2.4).

Multiple technologies are under investigation for the implementation of the preamp/shaper ASIC. Early investigations, including those documented in Reference [87], suggest that the
required performance can be achieved using bipolar Silicon-Germanium (SiGe) processes, which allow high speed and low noise configurations but at the cost of relatively high power consumption. While the SiGe approach is kept as a viable backup solution, the focus of current developments is on CMOS technologies, which are more challenging in terms of meeting the analog performance requirements, including 16-bit dynamic range, but using less power. As described below, efforts are underway to implement preamp/shaper prototypes using the 130 nm and 65 nm CMOS processes of TSMC. The final choice between the various technologies will be determined based on the measurements of the performance achieved with the prototypes, and the resultant physics impact.

To assess the preamp/shaper prototypes a common test stand has been developed for both the 65 nm and 130 nm preamp/shaper ASICs, so that the various prototypes can be evaluated in a consistent manner. Preliminary test results are expected by the end of 2017. The test stand consists of a digital readout board, a Front-End Test Board (FETB), a front-end mezzanine to house the analog front-end ASIC, and a toy calorimeter to emulate the detector capacitance.

**Preamp/shaper development in 130 nm CMOS** The LAr preamplifier used on the present FEB is a current amplifier using the 0T scheme [88], built with discrete components. Such a scheme is difficult to integrate in an ASIC because it uses capacitors as large as 1 µF and resistances down to 2.4 Ω. Moreover, several preamplifier types are needed to accommodate the maximal input currents and input impedance, depending on the layer and pseudorapidity region. A new architecture is therefore proposed to provide a versatile 130 nm CMOS ASIC coping with the requirements of all preamplifier types. This new line termination preamplifier, featuring electronically cooled resistance, is made around a resistor, a voltage amplifier and a Super Common Base amplifier (SCB).

This preamplifier design was implemented in the LAUROC0 (Liquid Argon Upgrade Readout Chip) ASIC, which contains eight channels with different transistor sizes and different options for the dynamic range/gains. The chip was submitted to a TSMC 130 nm MPW run in May 2016 and received in September 2016. Deeper characterization of all channels of the LAUROC0 chip are expected over the second half 2017, followed by irradiation campaigns, before submitting a new chip that will also include the shaper stage.

**Preamp/shaper development in 65 nm CMOS** A preamp/shaper design has been developed in the 65 nm CMOS process from TSMC. To optimize the noise performance, the preamplifier uses a fully differential design with passive feedback.

A prototype ASIC, dubbed HLC1, was submitted for fabrication in March 2017 and received in July 2017. It includes preamplifier, shaper, summing and peripheral circuits. The shaper has four poles and one zero for its anti-aliasing filter. The analog front-end has programmable termination to cover both 25 Ω/10 mA and 50 Ω/2 mA detector impedance. At the same
time, a three-bit programmable adjustment ($\pm 3\%$ steps, up to $\pm 5\Omega$) is available to fine-tune the termination. Two different gains (10 mA/600 $\mu$A or 2 mA/60 $\mu$A) can be read out simultaneously to provide full dynamic range coverage and optimum resolution for small signals. Programmable peaking time (30 $\sim$ 50 ns) in the shaper stage can be used to optimize the detector response and noise. The design has a built-in ADC driver to interface to commercial-off-the-shelf (COTS) or ASIC ADCs directly for evaluation tests. Three summing outputs are available to provide summing of either four or eight input channels. This will cover all possible configurations of Super Cell signals to the LTDB. A built-in pulse generator and mask bit for individual channels can be used to calibrate the electronic response and perform crosstalk studies.

HEC front-end

For the HEC, the pre-amplification is already done inside the cryostat, using GaAs ASICs [25]. The amplified signals arriving at the FEB2 have opposite polarity compared to the other LAr subdetectors, and therefore a special treatment of these signals needs to be considered in the design of the front-end ASIC. The range of the HEC signals at the FEB2 input is up to 0.75 V, corresponding to 15 mA current into a 50 $\Omega$ input impedance. A HEC-specific preamplifier on a common ASIC has to be designed. It can be a modification of one of the preamplifier types used for the EMB, provided that the preamplifier is fully differential.

Another HEC-specific feature is that the sampling ratio in longitudinal sections 3 and 4 (rear wheel) is a factor of two lower than in the first two section. To keep the same conversion factor across HEC cells, an additional gain of 2 is introduced for the channels serving these sections. The mapping of HEC connections to the FEB2 boards requires that two amplifiers out of four have this extra gain. These two amplifiers can be channels 1 and 2 of FE ASIC or channels 3 and 4, depending which FEB2 side (bottom or top) the ASIC is placed on. If all the preamp/shaper ASICs are on the same side of the FEB2, then they can be hardware configured for fixed gain. If both sides of the FEB2 are used, then each preamplifier requires individual configuration of its gain. In this case, an additional 4- or 8-bits (if the ASIC handles 4 or 8 channels) must be added to the configuration register for gain selection.

In the present electronics, the analog signals from the HEC are processed by dedicated preshaper electronics [89]. The HEC preshaper implements signal inversion and provides two gains (DC gains of 6 or 12 for front and rear HEC cells correspondingly). In addition, the preshaper equalizes the signal rise time, by pole-zero cancellation adjusted for each type of readout cell (there are 51 different cell dimensions in the HEC). This shape equalization, as well as double gain for rear cells, is needed to generate analog sums for the L0 trigger.

Special studies have been performed to quantify the errors in the total energy reconstruction in the case that the FE ASIC does not provide shape equalization. The conclusion is that the degradation of trigger sums is at an acceptable level, so pole-zero cancellation will not be
implemented in the FE ASIC. Another conclusion is that the double gain for the rear cells is critical for the trigger sums, and therefore it must be implemented.

The baseline solution is to design a HEC version of the preamp/shaper ASIC, with a HEC-specific preamplifier block that provides signal inversion and the required gain (trans-impedance) values. Fine shape equalization will not be implemented. The rest of the ASIC, including the shaper and the analog summing circuit, will be the same as for the other LAr subdetectors. This HEC version of the preamp/shaper chip will be developed in one of the future iterations of the ASIC design.

**Digitization**

The analog signal from each calorimeter cell will be digitized at 40 MSPS, synchronized to the LHC bunch-crossing rate. Studies of an option to digitize at 80 MSPS and use more refined digital filtering led to the conclusion that the possible modest gain in performance was outweighed by the cost and other implications from the resultant twofold increase in the data volume.

To cover the full 16-bit dynamic range, each channel will be digitized on multiple gain scales. The baseline solution is to use an ADC with a 14-bit dynamic range, in which case only two gain scales would be needed. The ADC will need to meet the radiation tolerance requirements described previously, have integral and differential non-linearities below one least significant bit, and consume less than 100 mW of power per detector channel.

Several approaches to the ADC issue are being explored in parallel, either the development of a full custom ADC design in 65 nm CMOS, or the possible development of an ADC that integrates in its core a commercially available “Intellectual Property” (IP) block, or the possible use of a COTS ADC chip. If the analog performance requirements can be achieved, the full custom design has a number of advantages, including low CORE cost, low power, and a design that can be fully customized to the LAr needs. The IP block approach provides an intermediate approach, where one can try purchase and use critical blocks with proven analog performance, while still customizing the digital interface as needed. The COTS approach would have a significantly higher CORE cost, and require additional developments to integrate the commercial ADC chip into the overall FEB2 architecture, and is being investigated as a backup in case the other approaches are not successful. The full custom ASIC option is the baseline choice for the LAr Phase-II electronics upgrade and is discussed in more detail below. More details on the two backup approaches are provided in Section 7.1.2.

There is substantial experience in the LAr community in the development of custom ADC devices. For the Phase-I LTDB, a custom four-channel 12-bit ADC [90] was developed in a 130 nm CMOS process. This ADC uses an architecture of four pipeline stages followed by an 8-bit Successive Approximation Register (SAR) ADC block. The ADC has a latency of about 100 ns, and excellent linearity thanks to digital error correction of the redundant pipeline...
stages. Many of the lessons learned in the development of the Phase-I ADC in 130 nm CMOS are directly transposable to 65 nm technology.

Most ASIC developments for Phase-II are targeting the 65 nm CMOS process from TSMC. CERN has negotiated a frame contract for this process to be available on the Phase-II timescale, and its widespread use in the Phase-II community enables sharing of IP blocks, etc. A collaboration that grew out of the Phase-I ADC effort is now developing a custom ADC for Phase-II in the 65 nm process. Advantages facilitated by the higher speed of this process include lower power and the possibility to implement a 12-bit SAR. The main challenge is extending the dynamic range to 14-bits, particularly given the low value of only 1.2 V for the power rail.

After simulating a number of possible solutions, a 14-bit ADC architecture that was chosen where each preamp/shaper output is connected to a 14-bit ADC that is comprised of two main sections: a Dynamic Range Enhancement (DRE) block that determines the most significant two bits of the 14-bit digital code, followed by a 12-bit SAR block. In the DRE, the input signal is sampled on two paths, one with unity gain and the other of gain four. A comparator determines which gain to use. The signal from the selected DRE gain is presented at the DRE output, which is connected to the input of the 12-bit SAR ADC block. The DRE design has been carefully optimized so that its output preserves the required 12-bit performance. For the SAR, a two-stage SAR architecture is used, exploiting the high speed of the technology while maintaining the SAR input capacitance at a reasonable value.

An ADC testchip, dubbed COLUTA65V1, was designed and submitted for fabrication in May 2017. The testchip includes one channel of DRE plus SAR. Additionally, a testboard has been produced and the chip was received at CERN in August 2017. The testboard will allow precision performance testing of the DRE and SAR, both separately and functioning together as foreseen in the full 14-bit ADC architecture. An additional testboard is being designed to perform radiation testing of the chip, including both total dose measurements and also SEU tests. Assuming promising test results, it is planned to iterate the ADC design and annually submit increasingly complete versions for prototyping, culminating in a full prototype being submitted in 2020.

Serialization and data transmission

Both the custom ADC development and the COTS ADC option involve utilizing ADC chips that each digitize the data from four calorimeter channels. With the baseline choice to use two 14-bit gain scales per channel, each ADC will have eight outputs. Each 14-bit ADC output will be formatted into a 16-bit word and serialized at a bit rate of 640 Mbps. Each 16-bit data word will include 14 bits of ADC data and a parity bit to provide error checking for that word. Given that each FEB2 board reads out 128 calorimeter channels, and that both gain scales will be read out for all channels, the resultant calorimeter data rate will be 256 data streams of 640 Mbps each, for a total data rate from each FEB2 board of 163.84 Gbps.
To guarantee the correct synchronization of the calorimeter data, BCID information will also need to be provided for each ADC chip. It is assumed that, as in the current LAr readout, a Bunch Counter Reset (BCR) signal will be distributed once per LHC orbit, as part of the Clock and Control distribution described in the next section. The BCR will be received on each FEB2 board and fanned out to BCID counters implemented either in each custom ADC chip or, in the case of the COTS ADC, in each digital interface chip.

The ADC data and BCID words need to be serialized and transmitted from the on-detector FEB2 boards to the off-detector LAr Signal Processor (LASP) units using optical links. The data transmission scheme will use lpGBT chips and Versatile Link+ (VL+) [91] optical assemblies. The lpGBT [92], being implemented using 65 nm TSMC CMOS technology, is a low power, higher bandwidth version of the GBT chip [93].

The ADC data serialization rate of 640 Mbps matches the input data rate expected for the so-called ePorts provided in the lpGBT chip. Each lpGBT chip can handle up to 14 such inputs, a poor match to the eight output data streams of each ADC chip. Multiple ADC-lpGBT mappings are being considered to optimize the number of required lpGBT chips and optical links and their utilization, taking into account design complexity, routing and synchronization issues. A scheme where sets of three ADC chips are mapped to twolpGBT chips, with 22 lpGBT chips per FEB2 board, is adopted as the baseline while more investigations are ongoing of the implications of each scheme on the optical fibre plant and on the LASP boards.

Clock and control distribution

Each FEB2 board will need to receive a 40 MHz clock, synchronized to the LHC machine clock, as well as other timing signals, such as the BCR. In addition, each FEB2 will include a large number of devices, including 32 preamp/shaper chips, 32 ADC chips, 22 lpGBT chips used for the data transmission, etc., that need to be configured and monitored. Slow control functions, such as the monitoring of temperatures and voltages on the board, will also be required.

Dedicated lpGBT chips on each FEB2, connected to bidirectional VL+ transceiver modules, will be used to provide the clock and control distribution, as well as the slow control readback. The 2.5 Gbps downlink functionality of these lpGBT chips will be used to provide the clock, timing, and configuration data to each FEB2 board, while their uplinks will provide the readback path. Investigations are being made of the feasibility of providing redundancy by using two dedicated lpGBT chips for this purpose on each FEB2 board.

Given the large number (of order 100) of on-board devices requiring clock and control information, a significant fan-out of the information will be required, as well as a fan-in of the corresponding readback data. A number of options are being considered, including the development of a custom “Config” chip should no other option prove suitable. The solution currently adopted as baseline uses the limited slow control functionality included
in the lpGBT chips, which has the advantage of using multiple copies of a single device, to implement the entire Clock and Control distribution.

An additional requirement on the 40 MHz clock is that it is distributed on the FEB2 with low jitter, both to ensure the stable and robust operation of the many optical links and to achieve 14-bit performance of the ADCs. Once first lpGBT prototype chips are available, tests will need to be made to evaluate the achievable analog performance.

**Trigger summing**

Analog sums are formed to provide input to a fast readout for the trigger system with coarser granularity than is provided by the main readout. In the current system, the analog signals from neighbouring cells in one layer are summed on each FEB to form $0.1 \times 0.1$ trigger towers [94] and sent to a Tower Builder Board (TBB), or to a Tower Driver Board (TDB) in the case of the HEC and FCal. As part of the Phase-I upgrade, these sums will be replaced by sums of smaller “Super Cells” [2], and transmitted to the LTDB. Both the TBB and the LTDB perform further signal processing before the trigger signals are sent off-detector.

The TBB and TDB boards will be decommissioned in 2024 at the latest. However, the LTDB, which will provide signals for the L1 trigger system after the Phase-I upgrade, will be kept in the Phase-II upgrade, with its inputs used by the L0 trigger in the HL-LHC era. Therefore, the FEB2 board will need to provide to the LTDB the required Super Cell analog sums.

For the EMB and EMEC, the Phase-II L0 trigger will have access to the full granularity, high precision readout data. The new FEB2 boards will provide the necessary Super Cell signals. These analog signals will be prepared in the preamplifier/shaper ASIC, or extracted and summed on a dedicated mezzanine card, similar to the present Layer Sum Boards (LSB).

For the HEC signals, the cold Preamplifier and Summing Boards (PSB) already produce the energy sums and therefore the HEC Super Cells are identical to readout cells. Super Cell energies will be sent to the L0/L1 trigger system from the LASP, along with energy sums calculated digitally. For redundancy, analog sums will be formed in the FEB2, digitized in the LTDB and processed in the LDPS, as done for the EM calorimeters.

The same scheme will be implemented for the FCal, where Super Cell energies will be provided by the LTDB-LDPS chain, and in addition energy sums will be calculated in the LASP and sent to L0/L1 processors. The latter sums can have even finer granularity than that of Super Cells, improving the trigger quality, as discussed in Chapter 4.

**FE cooling**

The existing under-pressure front-end cooling system is organized in six cooling loops per calorimeter face. One cooling station located on the ground-floor of UX15 maintains the flow of the water and maintains the under-pressure at the level of the front-end crates. The
returning warm water is cooled through a heat-exchanger connected to the approximately 12 degree cold “mixed” water in UX15.

The distribution to each front-end board is done via custom designed cooling manifolds that are mounted close to the front-end crates and distribute the water flow in parallel to all front-end boards of a crate via flexible pipes. Each front-end board has two custom made cooling plates, one on each face. The new front-end boards described above will be equipped with new custom designed cooling plates, similar to the legacy system. Since the total cooling power will stay approximately the same as for the legacy system, the cooling plant and piping can be re-used. However, some improvements to the current system being studied include the replacement of polypropylene connectors and the improvement of the granularity of the cooling loops in order to allow isolation of a smaller part of the detector in case of a leak.

5.2 Off-detector electronics

5.2.1 Overview of the LAr Signal Processor system

Off-detector, the LASP will receive the digitized waveforms, apply digital filtering to the signals of each LAr calorimeter cell, buffer the data until a trigger decision is received, and transmit the relevant data to the trigger and data acquisition (DAQ) systems. The LASP hardware implementation will be an evolution of the LAr Digital Processing System (LDPS) which will be installed during LS2 for the Super Cell readout [2]. The full data stream of detector signals digitized at 40 MHz will be available in the LASP modules. This will allow a determination of calibrated cell energies and of signal times with respect to the bunch crossing time including an active correction of out-of-time pileup. Corresponding results of digital filter studies are summarized in Chapter 4.

Apart from the regular detector readout to DAQ, the LASP system is foreseen to provide trigger input data to the The Global Event Trigger Processors (GETP) [6] and to the L0Calo FEX system. The Global Event Trigger Processors are planned to receive energies from cells which pass a given threshold defined relative to the total noise expected in each cell. In this way the data bandwidth can be controlled while retaining sufficient information for topological clustering and for electron-hadron separation using the strip layers in EMB and EMEC as input for electron/photon, jet and energy flow measurements. Furthermore, full granularity cell energies for the FCal can overcome certain limitations of the Super Cell readout in the forward region \(3.2 < |\eta| < 4.9\). It is expected that forward electron identification, jet and missing transverse energy measurements implemented in the Global Event Trigger Processors or in dedicated forward jet FEX modules provide an improved performance at highest pileup conditions. The expected performance of the future trigger system using LASP data is documented in Chapter 4. Since the analog input of the pre-shapers of the HEC FEB2 modules to the LTDB will not be fully identical to the signals
available after the Phase-I upgrade using the current FEBs, the LASP system can also provide digitally formed energy sums for constructing HEC Super Cells, if required.

The LASP units require a high input and output bandwidth and flexible programming of data handling, digital filtering and data reduction algorithms. Therefore a realization with Field Programmable Gate Arrays (FPGAs) as the main processing units is foreseen. Apart from the functional task of data reception and precise energy and timing measurement, the LASP system shall be compatible with the ATLAS DAQ and trigger architecture at the HL-LHC [6]. The baseline trigger architecture foresees one hardware trigger with 1 MHz L0 accept rate and 10 µs buffering interval. If required by trigger performance this design may evolve to two hardware trigger levels, L0 and L1, operating at up to 4 MHz L0 accept rate and up to 0.8 MHz L1 accept rate and L0 and L1 buffering intervals of 10 µs and 35 µs, respectively. The maximum latency for inputs to the L0Calo FEX system is 1.7 µs, and the skew between all calorimeter inputs to the FEXes is at most 16 BCs. The LASP system must be able to process 4 L0 accepts in 5 consecutive BCs, 8 L0 accepts in 5 µs and 128 L0 accepts in 30 µs. The first two rate conditions are mainly a requirement on either a derandomizing buffer of sufficient size and access speed implemented in the LASP units, or sufficient output bandwidth in order to deal with temporary trigger rates of up to 32 MHz.

5.2.2 Interface to the LAr calorimeter front-end

The FEB2 boards will connect to the off-detector electronics via optical links driven by lpGBT [92] serializers and VL+ optical converters. In total, data from 31 912 uni-directional links are to be received using the lpGBT protocol with FEC5 forward error correction [92]. Moreover, two fibre pairs per FEB2 are foreseen for clock distribution, control and monitoring (TTC). Since the full LASP firmware is not yet designed and since the FPGA resource usage is only based on estimates, the implementation of the full TTC interface in the same FPGA as the LASP unit may be too complex in firmware design and layout. There are two options considered which can mitigate this design risk. The TTC interface can be implemented in a separate “Main FPGA” on the LASP main board, so that functionalities are well separated, or a set of dedicated LASP boards will handle the TTC signal distribution and monitoring task. In case of the latter option, regular LASP boards can be used since these can provide a large number of links to the front-end. However, more LASP modules will be needed and more space in the ATLAS counting room, USA15. Detailed design studies are thus necessary to select between the baseline TTC distribution via each LASP board, and the alternatives.

5.2.3 Dataflow to the Trigger and DAQ system

The different tasks of the LASP define the dataflow and data buffering until the different trigger accept signals arrive. The raw data are decoded and a configurable remapping allows a grouping of channels that shall be processed in groups for energy summing and
data reduction. The data streams to the Global Event Trigger Processors and to the L0Calo FEX modules run at 40 MHz, while the output to the DAQ is controlled by the trigger accept signals. Raw and processed data arebuffered in memory for building DAQ data fragments.

The interface of the LASPs to the DAQ system is provided by the FELIX network interface modules [5] which are planned to receive and send data with a lpGBT compatible link speed. The data fragments to be sent to the DAQ on a trigger accept signal are composed of several blocks. For triggered events, the result of the precision energy calculation, of the signal time and of a signal quality parameter shall be transmitted, together with the raw data. The size of the data words will be similar to today's readout.

In addition, the LASP units will provide calorimeter information from individual LAr calorimeter cells to the Global Event Trigger Processors at 40 MHz, which will complement the L0Calo trigger which is based on Super Cell measurements.

Buffering on the LASP is necessary since the data transmission to the DAQ is triggered by L0 and L1 accept signals. Assuming that a LASP unit will handle 512 cells, the input data rate is 655.4 Gbps per LASP unit. These data are kept in memory for the full 35 µs buffering time which simplifies the selection of the raw data samples on L0/L1 accept. The memory required for raw data buffering is 22.9 Mbit per LASP unit.

Furthermore, the calculated energies, signal time and signal quality parameters as well as the trigger input energies of the selected cells need to be kept in memory until a trigger accept. The fragments selected by L0 can then be transferred to a second buffer for at most 35 µs until a L1 accept or fast-clear signal or time-out. The memory needs for the two buffering stages are 7.8 Mbit and 2.7 Mbit, respectively, per 512-cell LASP unit.

5.2.4 System requirements

The LASP system, including TTC distribution system, will be installed in the ATLAS counting room USA15. It will replace the LAr ROD system, which currently occupies 8 LHC racks.

The Phase-II LAr off-detector electronics is required to fit into a similar rack space as the current LAr ROD system. An extension of the LHC racks in height and cooling power per rack is under investigation, so that the floor space is reduced.

One general constraint is the available cooling power in USA15. For the future LASP system a maximum power consumption of 177 kW is allocated.
5.2.5 Data processing

The core functionality of the LASP will be the energy reconstruction and time measurement of the LAr signal pulses. Digital filtering algorithms will be used to reduce the effects of electronics noise and pileup noise.

The baseline of the front-end electronics targets a 2-gain 14-bit ADC readout with both gains being sent to the LASP system in order to avoid gain selection in the front-end and allow filtering based on samples from both gains. The selection between the two gain scales can be performed off-detector in the LASP, ideally choosing the highest scale which does not saturate. The selection algorithm is not yet defined and needs to be studied. In the current FEB, thresholds are applied to the peak ADC value in medium gain for the triggered signal pulse. In a free-running 2-gain mode, the full energy and timing reconstruction filter will be run continuously for both gains separately. The low-gain energy result, assuming it will never saturate, can be used to select the optimal gain. The optimal selection depends on the applied calibration scheme in order to avoid gain transitions in energy ranges interesting for physics measurements. The implementation in FPGA firmware provides flexibility to always adapt the gain selection to the calibration needs. Alternative signal filtering using mixed sample sequences from both gains is under investigation, but a consistent calibration scheme is more challenging in this case.

The reconstructed energy in each calorimeter cell from the continuous digital data stream represents the input to the trigger system. Energy values above $2\sigma$ total noise are planned to be sent to the Global Event Trigger Processors, while Super Cell energy sums for the HEC, and all FCal cell energies, can be sent to the L0Calo FEX modules. Depending on the filter algorithm, signal time information will serve to assign the energy measurement to the correct BC, and a signal shape analysis can be used to identify pulses with excessive noise contributions.

5.2.6 Hardware realization and components

The segmentation of the LAr calorimeter readout is mainly determined by the number of channels processed by one FEB2, which is up to 128 cells with 2 gains, i.e. 256 channels. One LASP unit will receive data from 2 to 4 FEB2 boards. The link speed to the Global Event processor is assumed to be 25.78 Gbps. If an FPGA model is not able to provide such high-speed links, the rate may be reduced down to about 15 Gbps, at the cost of about 75% more output links on average to the Global Event Trigger Processors. The HEC/EMEC output to the L0Calo FEX system (eFEX, jFEX, gFEX) assumes the legacy link protocol and speed as implemented during the Phase-I upgrade, while the FCal output to the L0Calo FEX system will take the full readout of the FCal cells into account, as it may be used by dedicated forward FEX processors. All serial links are driven by transceivers of the FPGA. The TTC and Ethernet inputs may also be provided by other I/O connections, like LVDS signals or dedicated PHY chips, respectively, depending on the available FPGA resources.
Modern FPGAs can operate the input and output links of the duplex transceivers at independent speeds. The required number of transceivers of the LASP FPGAs is therefore determined by the number of input links, which always exceeds the number of output links, even for HEC and FCal regions where additional data are transferred to the L0Calo or Global Event trigger systems.

General layout of the LASP hardware

The main building blocks of the LASP system will be the FPGA processing units which will be mounted on a PCB and connected via high-speed links to electro-optical converters. Optical pig-tails lead to the front-panel optical connectors, to which both input and output links will be connected. Since the industrial trend is going for higher link speed rather than for higher fibre counts per connector, a 12-fibre converter can be assumed. In the configuration with 4 FEB2 per LASP FPGA the number of necessary 12-fibre transceiver modules ranges from 10 to 14, depending on the amount of output data that needs to be transmitted, on the implementation of the TTC clock distribution directly in the LASP, and on the available maximum link speed of the FPGA. The link speed at the input does not appear as a limiting factor for concentrating the information of several FEB2 boards into one FPGA unit because the required number of DSP units for multiplier-adder operations, the logic and the necessary memory impose a stronger constraint on the FPGA choices, at least if today’s FPGA models are considered. Also the flexibility of the Global Event processor interface leaves some freedom in the choice of FPGA models concerning the availability of very high-speed links (over 25 Gbps).

LASP form factor

The main characteristics of the LASP defining the form factor are the size and pin-count of the FPGA (typically 4 cm × 4 cm to 5 cm × 5 cm and more than 2 000 BGA pins), the number of FPGAs (372 to 744), the number of fibres connected to each FPGA (up to 140), and the power dissipation. The PCB and board design will require a high density, high-speed, complex signal mapping with long signal tracks and high power consumption. The processor will have to operate with virtually no problem for a long time, typically 15 years, given the fact that the dead-time induced by a failure may have significant negative consequences on the data taking. Therefore, Quality Assurance (QA) considerations have to be taken into account very seriously at an early stage of the design, and should dominate in the choice of the form factor.

The baseline design for the LASP modules is based on the Advanced Telecommunications Computing Architecture (ATCA) form factor. Two LASP units per ATCA blade are foreseen each equipped with a high-performance FPGA and electro-optical receiver and transceiver arrays, as well as additional memory and clock distribution devices. The optical links are routed to Multifibre Push-on (MPO) connectors on the front panel. The main section of
the blade contains a Main FPGA for TTC signal distribution, in case it cannot be directly implemented in the Processing FPGAs, and for preparing Super Cell data from HEC and FCal for the trigger system. The TTC fibres connect to the FEB2 on the LASP front face, like the data input links, while the Super Cell data are sent via the Rear Transition Module (RTM) to the L0Calo FEX systems. The Main FPGA is also foreseen to prepare monitoring data.

The LASP board is planned to be realized as a full-size ATCA blade or, alternatively, with 2 Advanced Mezzanine Cards (AMC) for the processing units and an ATCA carrier blade for the main section. Full-size ATCA boards allow a PCB thickness of 2.4 mm with 24 layers for signal routing and power distribution, while for an AMC based design through-hole plug connectors can be implemented to increase the PCB thickness beyond the standard 1.6 mm. Double-width AMC modules with dedicated DC/DC converters and additional Mezzanine Module Control (MMC) chips will be required. Although a monolithic board design is less modular than the concept with one main board equipped with 2 FPGA mezzanine cards, it provides more freedom in placement of processing FPGAs, optical transceivers, power modules and other components on the board. A detailed comparison of the monolithic and modular blade designs will be performed in the early LASP R&D phase.

Alternatively, the FPGA processing units may also be placed on PCIe cards. These allow a placement of large 5 cm × 5 cm FPGAs, similar to the double-width AMC cards. The board area is also expected to be sufficient for optical transceivers and routing of fibres to external connectors, as shown in other LHC applications [95]. A detailed comparison of the ATCA and PCIe options based on technical feasibility of PCB design, power, and cooling will need to be done.

FPGA candidates

FPGA devices for signal processing are part of a rapidly developing field in industry targeting higher processing capabilities per chip, higher numbers of I/O connections, more memory and lower power. Devices which will be implemented in the final, optimized design of the LASP modules may thus not even be available today. However, some FPGA models already fulfil the requirements of a LASP unit. A survey of modern high-end FPGAs was performed to investigate their available resources and possible margin with respect to the LASP requirements. All of the investigated devices have 2000 to 2500 BGA pins and require up to 5 cm × 5 cm of board area. Depending on the number of available transceivers, DSP blocks and memory, each LASP FPGA can process the input of 2, 3, or 4 FEB2 boards. The advantage of processing a smaller number of FEB2 boards is the reduced power consumption per FPGA which scales with number of channels processed. However, a higher integration factor reduces the total number of FPGAs and allows the implementation of algorithms based on cell information from a larger detector area. In particular, the preparation of Super Cell energy sums for the HEC can then be performed directly in the processing FPGA. In the baseline layout, one LASP FPGA therefore connects to 4 FEB2 boards.
5.2.7 System integration

The LASP system will be installed in USA15, ideally close to the entry point of the detector signal fibres and close to the L0 trigger system. A total of 372 LASP FPGA units will be needed if 4 FEB2 inputs are connected to one unit and ideally 2 FPGAs are mounted on one ATCA main board, which results in 186 ATCA readout boards.

For the complete LASP readout system, due to the power dissipated by the main board, a maximum power budget of 175 kW is obtained if only 2 FEB2 are handled by one LASP FPGA. If 4 FEB2 are connected to each LASP unit, which is the baseline option, fewer ATCA boards are needed and the LASP total power can be reduced to 164 kW. The power per ATCA board is expected to be 720 W for the latter option, and 380 W for the former.

The high processing and power density will also be a criterion for the shelf arrangement within an LHC rack. In case the ATCA shelves are only loaded with 8 boards of 720 W and when placing 2 shelves in each rack, the racks will need to provide 13.7 kW of cooling power. This includes the power of the ATCA fan units and shelf managers (1.1 kW per ATCA shelf). If larger racks can be used with space for 3 ATCA shelves, the cooling power must be at least 20.6 kW per rack for the baseline LASP board configuration.

Since the power density per rack will be independent of the power per board or per shelf, the total number of LASP racks is nearly independent of the LASP board configuration. For the baseline setup, 8 high racks with 3 shelves each or 12 regular racks with 2 shelves each will be needed. If the TTC distribution is implemented on dedicated boards, the 15 to 24 additional LASP blades will require 2 ATCA shelves, and 1 regular LHC rack. The total power of the Phase-II off-detector electronics finally sums to 177 kW and the total space requirements to 26–30 ATCA shelves.

Each unit of the LASP system will be connected to a readout control and monitoring PC via Ethernet connection. These PCs will configure the LASP units and can permanently receive error and warning messages from the system as well as regular monitoring data from the input and output data streams. This will in particular be useful during the commissioning phase of the system, where hardware and firmware functionality and data integrity need to be checked in detail.

5.3 Power supplies and distribution

The voltages to operate the front-end electronics are provided by dedicated Low Voltage Power Supplies (LVPS). Two different systems are needed to distribute the power to the FE electronics. One system provides the low voltage power to all front-end electronics which is located inside crates attached to the cryostat warm walls. Additionally, one system is needed for the HEC, to provide low voltage power to the preamplifiers and summing boards which
are mounted on the HEC detector inside the cryostat. The planned Phase-II upgrades for these two systems are discussed below.

5.3.1 FEC power distribution system

In the present system, AC/DC Main Converters (MC) located in USA15 are used to generate 280 V and are connected through about 70 m-long cables to LVPS mounted in proximity of the FECs. The LVPS contains DC/DC converters which provide the seven low voltages needed, ranging from 4.0 to 11.0 V, including two with negative polarity. The units are custom made to satisfy the size restrictions (approximately 15 cm × 30 cm × 40 cm), have a power of 3 kW and are water cooled. There are 58 MCs feeding one LVPS each: 16 units are used for each side of the barrel calorimeter and 13 units for each of the two endcaps. The low voltages reach the FEC through connections on its sides (short dimension of the crate in the r-z plane) and are distributed to the front-end boards through pin connections on a bus bar running on the long dimension (φ) of the crate.

Low dropout linear regulators on the FEBs (LHC4913 for positive and LHC7913 for negative voltages [96]) handle the final adjustments. On the new trigger board (the LTDB), installed in Phase-I, the power is distributed through a mezzanine board mounted on the main LTDB PCB and connected to the crate power bus. The mezzanine uses some of the existing voltages as input and converts them to the needed values using LTM4619 DC/DC converters for the digital part and again LHC4913 (positive voltage) and LHC7913 (negative voltage) voltage regulators for the analog part.

5.3.2 New power distribution scheme from Main Converters to front-end

For the Phase-II upgrade, the new front-end electronics will mostly use voltages lower than the present ones (between 1 and 4 V). In this situation the existing power distribution scheme will be highly inefficient and will need to be changed. As in the current system, MCs will be used to generate 280 V DC (or similar voltage) which provides the input voltage to the new LVPS. In any case the existing MCs will be replaced as they will be too old at the start of Phase-II. The new units will be located in the racks occupied by the present units and have very similar requirements (see [94]). They will take a three-phase 400 VAC as input, be remote controlled and monitored and, as in the present units, each 280 V supply will be interlocked by a fast hardware signal which turns the units off in case of an alarm (such as cooling water failure or smoke detection in the front-end electronics area). The new LVPS will generate only one intermediate voltage still to be decided (48 V, 24 V or 12 V). The units need to provide a power of about 3 kW as today, and be tolerant to the presence of magnetic field and radiation (up to a level that depends on which of the two options described below is chosen). The units will be remotely monitored and controlled. The output voltages will be monitored both in the front-end crate and internally in the LVPS, to verify that the functionality of each module is within the specification requirements.
The final voltages needed by the front-end electronics will be generated from the intermediate voltage directly on the front-end boards by using Point Of Load (POL) converters.

The two options discussed below are under consideration:

**Option A** The present LVPS are located in a position difficult to access in case there are problems, or servicing is needed. The opening of ATLAS is, in fact, necessary to access the faces of the barrel or endcap cryostat to replace a faulty unit. Although redundancy can be built into the LVPS (as done in the present units), the risk of losing a LVPS and hence a large fraction of the calorimeter acceptance still exists and represents one of the largest single points of failure of the LAr calorimeter. To overcome this limitation it is proposed to relocate the LVPS in a more accessible position that could allow servicing of the units even during data-taking periods with a short access to the experimental cavern.

For the barrel supplies, a possibility would be to use the six so-called “Patch Panel 2” locations where pixel, TRT and other ID services are currently located. The new LVPS positions should be located around the barrel cryostat, as close as feasible to the FECs, so that the units can be distributed uniformly in order to reduce and equalize the cable length. In the endcap a similar solution could be obtained by relocating the LVPS around the external surface of the TileCal modules, in positions that can be accessed also when the ATLAS detector is closed and that do not obstruct the displacement of the endcaps through the Muon Spectrometer when ATLAS is opened.

**Option B** In this approach the intermediate voltage will be generated by new units that will replace the present LVPS and will be located in the same position. These new units might be either a newer generation of the present supply made by Wiener, modified to provide only one voltage instead of seven, or a different LVPS. In both cases the design must be built to provide high redundancy in the units in case of failures as the units in the present locations are not accessible for repair or replacement when ATLAS is closed. A prototype [97] has been developed in collaboration with CAEN, based on a DC/DC Phase Shifted Converter.

The CAEN prototype is not radiation tolerant and work is on going to evaluate the use of GaN devices instead of Si power MOSFETs. The expected radiation doses in this region are given in Table 3.1. Moreover, a maximum magnetic field of 0.1 T in these positions, does not represent a problem as demonstrated by the present Wiener units that are operating correctly in this condition.

Option A is considered the baseline solution for the FEC power distribution system because of its advantages both from a technical point of view and from the point of view of the reliability and maintenance of the detector. Given the different requirements between Options A and B in terms of magnetic field tolerance and radiation levels, it is important that a decision between the two options is taken in relatively short time. By the end of 2018
the plan is to produce a power board of enough power (at least 1 to 1.5 kW) that can be operated successfully in presence of magnetic field. This board would represent the building block of the future LVPS. In addition, confirmation about the feasibility of the proposed placement is expected by that time to be available by ATLAS technical coordination. If both conditions are met by mid-2019, the development of a pre-prototype satisfying most of the requirements will start and a final layout of the powering scheme for both barrel and endcap will be prepared. A full fledged prototype will be produced by mid of 2021. If it is found that it is not possible to continue with Option A, Option B will be pursued by both asking the vendor of the present LVPS to modify the design to fit our new requirements and by finalizing the design of the Phase-II prototype already produced. By 2020 one of these two options will be chosen in order to arrive to produce a prototype end of 2021.

On-board power distribution

Independent of the option chosen, the final voltage step-down is performed by POLs on each front-end board. The supplies can be provided by the use of DC/DC converters like the LTM4619 already in use on the LTDB in Phase-I.

Moreover, we plan to provide adequate filtering with new regulators that replace the LHC4913 which are going to become obsolete. Several commercially available IC devices for voltage regulation were tested for radiation tolerance in the framework of the R&D for the LAr Phase-I new trigger board (LTDB). A good number of devices met or even exceeded the Phase-I radiation requirements. A new radiation study of voltage regulators (positive and negative, if needed) will be performed to select devices that could be used in Phase-II.

The power section of the LTDB is implemented as a mezzanine board mounted through pins on the main LTDB board. The mezzanine takes as input some of the voltages created by the current LVPS and converts them to the voltages needed by the LTDB. For Phase-II, these mezzanine boards will be removed and replaced by mezzanines that, following the new power distribution scheme, will generate all the needed voltages from just one voltage generated by the Phase-II LVPS.

5.3.3 HEC power distribution system

The LVPS for the HEC [11] provide the power for the cold readout electronics [25] and need to be exchanged due to age and higher radiation hardness requirements. The new HEC LVPS can largely follow the design of the current HEC LVPS [98] because the cold readout electronics for the HEC will not be replaced for Phase-II. Each endcap is divided in 4 quadrants with one LVPS serving one quadrant which is divided in 8 φ sectors. Possible changes for the position of the HEC LVPS a different location, more accessible with ATLAS in closed position, are being investigated. Furthermore, possible single-points-of-failure
of the current design will be reviewed and, in case they are deemed necessary, options to mitigate them will be studied.

The HEC LVPS will have to be able to provide three voltages (7.2 V, 3.1 V, and −1.5 V) with double redundancy (two DC/DC converters per output like in the current system, each converter being capable of supporting the full load). They will also have to be remote controllable via the Detector Control System (see below). A backup control system should also be available in case the former fails, a functionality present in the current system via the so-called “LogicChip”, which provides an independent serial interface to monitor and control the LVPS.

A first set of prototype DC/DC converters with exchanged PowerMOSFETs and other components with higher radiation tolerances, but largely following the original design, has been produced by Wiener and is currently under test at MPI Munich. In parallel, a search is ongoing to identify suitable positive and negative Low Voltage Regulators. The devices currently in use (LHC7913 and LHC4913) would be within the specifications but it is not clear if enough are still available. Finally, radiation-hard FPGAs are being considered for the replacement of the LogicChip.

5.4 Detector Control System

The task of the LAr Detector Control System (DCS) is the control and monitoring of the LAr calorimeter, of its subsystems, and its infrastructure, in a coherent and safe way. LAr has four control subsystems; the HV subsystem delivers HV for all LAr calorimeters and purity monitors, the Front-end Crate Low Voltage subsystem (FEC LV) is responsible for the control and monitoring of power for the front end electronics, the HEC Low Voltage subsystem controls and monitors the power of the HEC cold readout electronics, and, finally, there exists a subsystem for the monitoring and control of the off-detector electronics racks. There are also three additional monitoring subsystems: the first monitors the detector module temperatures and the second one monitors the purity of the liquid argon. Finally, a dedicated subsystem monitors the front-end and off-detector electronics temperatures using data points provided by the LAr online software via the DAQ system.

The current LAr DCS follows the paradigm outlined for the central ATLAS DCS [99] architecture which consists of a front-end (FE) system and a back-end (BE) system. The FE includes the DCS hardware such as sensors, power supplies, and I/O devices. In the current configuration, LAr uses the Embedded Local Monitoring Board [100] (ELMB) as a common I/O device. The current ELMB is radiation hard for integrated TID doses up to 140 Gy, NIEL doses up to $4 \times 10^{12} \text{n}_{eq}/\text{cm}^2$, and for up to 1 SEE for $1 \times 10^{11}$ protons/cm$^2$ and thus does not satisfy the radiation tolerance requirements at the HL-LHC. Three LAr DCS subsystems, the HEC LV, FEC LV, and temperature monitoring systems use 170 ELMBs which will be replaced with a new device, dubbed ELMB++.
The ELMB++ will be a central CERN development and consists of an integrated circuit which is a part of the GBT chipset. Its purpose is to distribute control signals to and monitor signals from the front-end electronics. The leading proposal for the design of the ELMB++ calls for two types of devices: A so-called, “Hub”-ELMB++ board will be used as a hub for up to 19 simpler devices, dubbed “Satellite”-ELMB++ connected via electrical links in a star point topology [101]. The Hub-ELMB++ will transmit the DCS data to the BE via an optical link connection to a new network interface board, dubbed ELMB++ FPGA, installed outside the experimental cavern.

The overall architecture of the current DCS system will remain the same for Phase-II, despite the necessary changes in the FE. However, some developments in the BE will be needed for the monitoring of the LAr front-end electronics via the DAQ path, to accommodate changes to the DAQ system. Furthermore, a monitoring and control project for the new shelves housing the off-detector electronics will be developed.

5.5 Installation and commissioning

The installation of the LAr Phase-II Electronics will have to be planned within the boundary conditions of a very tight LS3 schedule for UX15. Whereas the installation and commissioning of the LAr signal processors and the fibre plant in USA15 will be rather independent from the work going on in UX15, the installation of the optical fibres, the HEC low-voltage power supplies, the front-end boards, the calibration boards, and the low-voltage power supplies for the front-end electronics will be driven by the accessibility of the front-end crates, the TileCal finger region and the cable chains. We estimate that three teams of two people (one engineer and one technician each) can perform the installation work within the allocated 3 months per detector face. Before installation, each component will be tested thoroughly. For some parts, reception tests at CERN will be performed prior to installation on the detector.

The installation operation follows the deliverables and covers the different parts of the system, each one with a different degree of difficulty: for the off-detector electronics in USA15 access is essentially always available, so the installation is rather simple and covers the placing of crates, boards, patch panels, fibres, fibre plant, etc. The front-end electronics installation is clearly the most constrained since about 1800 front-end and other boards in 58 FECs must be removed, new front-end and calibration boards installed and all services connected to allow for the final commissioning and sign-off on each complete crate before access is lost. Given the amount of effort and the limited time frame available, it will be imperative to operate with several teams on several FECs simultaneously. For the LVPSs, in the case of the endcap it will be possible to be connected to the existing cooling loops. For the barrel, however, it will most likely not be possible to extend the existing water cooling branches servicing the current LVPSs to the new locations. Under-pressure water cooling will need to be made available and most likely a new dedicated small cooling station will be
necessary. The LVPSs will be needed for the commissioning of the new front-end electronics and will therefore need to be installed prior or in parallel to the board installation. Finally, the laying and routing of the cables will be done by the ATLAS TC team.

The commissioning of the system must take place in parallel with the installation operation. Depending on the overall LS3 installation schedule, access to some front-end locations might become difficult relatively soon after installation. It will therefore be challenging to commission each FEC immediately after installation and test the full functionality. In order to do this, the full infrastructure must be available during commissioning, power (including the new power supplies), DCS, and online software. Beyond this infrastructure, which will be installed by the LAr group, other important prerequisites for the commissioning will be taken care of by technical coordination. The optical fibres will need to be installed before the commissioning can start, and the front-end cooling system must be operational and extended to also serve the LVPSs at their new locations. To achieve that, a close coordination with the technical coordination teams will be essential.

The commissioning of each FEC will then consist of taking calibration runs to measure and analyse quantities like noise, coherent noise, crosstalk, electronics gain, pedestals, pulse-shapes and auto-correlation. It is also crucial to detect any dead readout channels or calibration lines and compare them to the dead-channel lists of the legacy system to determine whether a detected dead channel might be broken inside the detector.
6 Calibration

To take advantage of the stability and uniformity of the ionization signal in liquid argon the readout electronics are provided with a precise calibration system. The following sections describe this system in the current detector and the calibration board for the Phase-II upgrade.

6.1 Overview of LAr electronic calibration

Charged particles in electromagnetic or hadronic showers developing in the LAr calorimeters ionize the liquid argon as they traverse the active gaps. The fraction of the shower energy that is lost by ionization in the LAr gaps generates the device signal. The ionization electrons drift in the field produced in the LAr gap by an applied high voltage, generating a current with an amplitude proportional to the released energy. This current is then amplified, shaped, sampled at the LHC bunch-crossing frequency and then digitized by the readout chain [8, 17].

In order to reconstruct the raw energy deposited ($E_{\text{cell}}$) in a given readout cell, the amplitude of the shaped signal ($A$) is reconstructed as the weighted mean of the signal digitized samples ($s_i [\text{ADC}]$) using the Optimal Filtering (OF) technique [16]:

$$A[\text{ADC}] = \sum_{i=1}^{N_{\text{samples}}} a_i (s_i - p)$$ (6.1)

$$A\tau[\text{ADC} \cdot \text{ns}] = \sum_{i=1}^{N_{\text{samples}}} b_i (s_i - p)$$ (6.2)

where:

- $N_{\text{samples}}$, 5 during the LHC Run 1 and 4 during Run 2, is the number of digitized signal samples used in the OF reconstruction.

- the $a_i$ weights are the OF coefficients (OFC) for the pulse amplitude $A$, while the $b_i$ weights are the OFC to compute the relative time $\tau$, measuring the potential jitter between the expected and actual pulse timing [16]. The $a_i$ and $b_i$ OFC are computed from the normalized ionization signal shape, by requiring the minimization of the resulting noise on the amplitude estimate. Different ingredients are consequently needed for a given cell and readout gain:
the corresponding normalized ionization\(^1\) pulse shape; the knowledge of the ionization pulse with a fine time granularity and of its derivative are needed in order to optimize the OFC \(a_i\) and \(b_i\) so that the reconstructed amplitude \(A\) is only weakly biased in case of small timing misalignment or readout jitter.

- the electronic noise time autocorrelation (see Section 6.1.1); the knowledge of the noise time autocorrelation is needed to optimize the OFC \(a_i\) so that they minimize the noise contribution to the amplitude estimator \(A\) (Equation 6.1), taking into account the correlation among the noise contributions to the signal samples \(s_i\). Depending on the luminosity, the pileup has also to be considered since it modifies the total noise and its autocorrelation.

- the \(p\) value measures the ADC pedestal level for the given readout cell for each readout gain (see Section 6.1.1).

The amplitude \(A\) of the shaped pulse is then converted from ADC units to energy in MeV by the formula:

\[
E_{\text{cell}}[\text{MeV}] = F_{\text{DAC} \rightarrow \mu A} \cdot F_{\mu A \rightarrow \text{MeV}} \cdot \frac{1}{M_{\text{phys}} / M_{\text{cali}}} \sum_{j=0}^{N_{\text{ramps}}} G_j A^j, \tag{6.3}
\]

- The factors \(G_j\) are coefficients of a polynomial of degree \(N_{\text{ramps}}\) in powers of \(A\) that parameterize the cell electronic gain as determined from the calibration runs (Section 6.1.3), and are used to convert the reconstructed ADC units to current units (DAC) as set on the LAr calibration board [84]. Ramp runs are used to extract the response of each cell as a function of the injected current. During the Run 1 and Run 2 operation, only the linear terms \(G_0\) and \(G_1\) were used, thanks to the excellent linearity of the readout electronics. Higher-order term could in principle be applied to correct any residual non-linearity of the electronic response.

- The factor \(M_{\text{phys}} / M_{\text{cali}}\) corrects for the difference between a calibration and an ionization signal’s gain factor \(G_j\) corresponding to the same current [85]; it is obtained during the procedure to predict the ionization pulse shape (see Section 6.1.4).

- The \(F_{\text{DAC} \rightarrow \mu A}\) factor converts the current measured in calibration board DAC units to \(\mu A\) and accounts for the values of the local mother board injection resistor [8, 102].

- The \(F_{\mu A \rightarrow \text{MeV}}\) factor converts the reconstructed current to energy accounting for an average value of the sampling fraction; it returns a raw estimate of the total energy released in both the active and passive part of the calorimeter cell [8, 102].

\(^1\) Using an analogous procedure, \textit{calibration} OFC are computed from the calibration pulse shape and used in the reconstruction of the amplitude of the calibration pulses during the procedure to measure the readout gain (Section 6.1.3)
All the calibration constants used in the cell energy reconstruction, excluding the $F_{\text{DAC} \rightarrow \mu A}$ and $F_{\mu A \rightarrow \text{MeV}}$ factors, are computed from calibration data routinely acquired during dedicated calibration runs. The value of these constants is continuously monitored and validated in order to guarantee the best electronic calibration of the LAr detectors at any given time. The $F_{\text{DAC} \rightarrow \mu A}$ and $F_{\mu A \rightarrow \text{MeV}}$ conversion factors are currently obtained from first principle calculations [102], and then tuned by comparing the detector response to real data from beam tests and in the corresponding Monte Carlo simulations.

In periods without beam, such as the time between LHC fills, a series of dedicated calibration runs are taken in order to equalize the response of the LAr calorimeters. The extraction of the necessary constants requires three types of calibration runs: Pedestals, Delays and Ramps. Pedestal runs measure the baseline level of a cell’s readout electronics and its noise properties; ramp runs measure the readout gains; and delay runs measure the shape of the pulse as a function of time for each readout cell using a known exponential current. An independent set of calibration runs is acquired for each of the three LAr electronic readout gains.

### 6.1.1 Pedestal runs

During a pedestal run, the response of the readout electronics is recorded without any signal injected into the calorimeter cells. This gives values for the electronics baseline level and also allows the computation of the electronic noise and its time autocorrelation.

A pedestal run is typically taken when no collisions are provided by the accelerator, by recording $N_{\text{triggers}} = 3000$ empty events with $N_{\text{samples}}$ (typically 7 or 32) consecutive signal samples spaced by 25 ns digitized for each event. The average pedestal value ($p$) and its noise RMS ($\sigma$) are computed by using all the available statistics ($N_{\text{triggers}} \times N_{\text{samples}}$). This procedure is independent of gain.

The noise autocorrelation matrix measures the correlation between consecutive time samples. For a given channel, the characteristics of this matrix depend on the relative fraction of the different noise components, the electronics gain, the signal shaping, the detector capacitance and the cable lengths. The normalized autocorrelation matrix $C_{ij}$ for a given channel is built as a Toeplitz matrix based on the relevant autocorrelation function:

$$ C_{ij} = \frac{(\text{ADC}_i - p) \times (\text{ADC}_j - p)}{\sigma^2} $$

(6.4)

where $\text{ADC}_{i(j)}$ is the content of a sample $i(j)$, $p$ is the average pedestal and $\sigma$ the cell noise RMS. The autocorrelation matrix is symmetric by time translation, thus all the terms in a given diagonal reflect the noise correlation between any sample with a sample at a given time distance. Since the matrix is normalized to the noise RMS ($\sigma$), the term $C_{ii}$ is always 1, and is therefore not stored in the database. Because of its symmetry properties, the independent
terms of the $C_{ij}$ matrix are stored as a vector of size $N_{\text{samples}} - 1$ reflecting the meaningful part of the normalized autocorrelation function.

The total noise time autocorrelation matrix, including both the electronic and pileup components, can be similarly measured from minimum bias collision data.

The experience of Run 1 and Run 2 [102] suggests that the electronic calibration constants should be routinely changed to follow the possible evolution of the response and properties of the readout electronics. In normal operation conditions, pedestals $p$ can be updated as frequently as once per day.

### 6.1.2 Delay runs

Delay runs measure the response of each readout cell after amplification and shaping to the applied exponential calibration current. In this type of run, calibration pulses of fixed amplitudes are injected as near as possible to the cells in the detector following alternating patterns of cells. This is designed to minimize the overlap between the signal collected in a given pulsed cell and any cross-talk contribution from all the other pulsed cells.

A delay run proceeds as follows. $N_{\text{triggers}}$ 200 events, corresponding to a given injected current, are acquired for each cell; $N_{\text{samples}} = 32$ signal samples are retained for each trigger, and for each sample the $N_{\text{triggers}}$ are averaged, digitized and stored. A time delay is then introduced between the injection of the calibration pulses and the readout acquisition and the pulsing and acquisition procedure repeated. The current calibration boards are equipped with a dedicated delay chip originally intended to introduce such a time difference, but during the Run 1 and Run 2 operation this feature was never used and the time delay is instead set via the triggering TTC\text{rx} system. For each delay step and at each sample, the mean response and RMS over the $N_{\text{triggers}}$ events are computed by the online DSP. The full pulse shape is then reconstructed offline by ordering in time all mean responses corresponding to the different time delay values. For the Run 1 and Run 2 operation, the time difference of 25 ns between two consecutive samples is covered in 24 delay steps spaced by approximately 1.04 ns: therefore, this method allows the reconstruction of the calibration signal pulse with an effective sampling interval of 1.04 ns. At the end of the reconstruction procedure, the baseline of the delay pulses is restored by subtracting the corresponding pedestal ($p$) obtained from the corresponding pedestal run within the same campaign.

### 6.1.3 Ramp runs

Ramp runs are used to extract the response of each cell as a function of the injected current. The values of the current used varies according to the gain of the electronics being probed. A ramp run is taken as follows:
• A series of steps are used to span the full DAC region from DAC = 0 to DAC = 65,500 (the highest value). The number of steps vary with the detector and gain.

• Two hundred events are triggered for each DAC value. For each of the 5 samples which are kept, the DSP computes the average response of the 200 events in ADC counts.

• Offline, the 5 averaged samples are used to reconstruct the maximum amplitude of the pulse \( A_{\text{max}} \) per gain and DAC value. First, all samples in the front layer are corrected for signal leakage into neighbouring cells due to cross-talk. Next, the amplitude \( A_{\text{max}} \) is extracted by combining the samples weighted by calibration OFCs computed from the delay pulse (Equation 6.2). Note all saturating pulses are excluded from this procedure (a pulse is declared saturating when at least one sample measures more than 4,000 ADC counts). Because of this precaution, not all DAC values are used for all layers, since saturation differently affects signals depending on their intrinsic amplitude, which varies with the cell capacitance.

• In the last step, the DAC vs ADC relation is obtained by fitting \( A_{\text{max}} \) as a function of DAC. This gives the gain correction factors \( G_i \) which enter into the cell energy reconstruction as described in Equation 6.3. During the Run 1 and Run 2 operation, given the excellent linearity of the readout electronics, a linear parameterization was used:

\[
\text{DAC} = G_0 + G_1 A_{\text{max}}
\]  

(6.5)

The slope \( G_1 \) parameterizes the electronic gain, while the constant term \( G_0 \) corrects for a possible bias at the origin. The intercept \( G_0 \) is only needed for the EMB for the medium and low gain cases in order to meet the requirement of keeping the non-linearity below 0.1%, in all other cases \( G_0 \) is not used.

The experience of Run 1 and Run 2 [102] suggests that the electronic calibration constants should be routinely changed to follow the possible evolution of the response and properties of the readout electronics. In normal operation conditions, the ramp coefficients \( G_j \) can be updated as frequently as once per day.

6.1.4 Prediction of physics pulses

In a given cell, the ionization pulse shape differs from the calibration pulse shape. The difference is due to the calibration current having an exponential shape instead of the triangular form of the current pulse produced by an ionizing particle in the detector; to the different injection points of the calibration and ionization pulses on the detector; to the parasitic inductances introduced by the cables used to transport the calibration signals. Thus, starting from the calibration pulses, the prediction of the ionization shapes is achieved by the use of an electrical model simulating the detector and its electronic chain, and by deconvolving the previous effects.
To predict ionization pulses for the electromagnetic barrel and endcap calorimeters, a series of constants related to the cell geometry and calibration signal are needed. The cell geometry constants needed are the resonance $L_D C_D$ value (where $L_D$ represents the inductance of the signal path and $C_D$ the cell capacitance), its resistive component $r_D$ (through the parameter $\tau_r = r_D C_D$), and drift time $T_{\text{drift}}$ of the ionization electrons; whereas the necessary calibration signal constants are current decay time ($\tau_{\text{cali}}$) and its offset with respect to the baseline ($f_{\text{step}}$). Some of the necessary constants have been measured directly on the detector or calibration boards. For other constants, their effective values can be extracted from the calibration pulse itself. This is the case for $L_D C_D$, $f_{\text{step}}$, and $\tau_{\text{cali}}$. Additionally, the parameter $\tau_r$ measuring the effective resistive component of the cell can be computed directly. Using these values, the physics pulse can then be predicted along with the expected difference of the maximum amplitude with respect to the normalized calibration pulse (the parameter $M_{\text{phys}}/M_{\text{cali}}$) that accounts for an $\eta$ and $\phi$–modulated correction of the order of a few percent. Details concerning the prediction of physics pulses for the ATLAS electromagnetic calorimeter and presampler can be found in Reference [85].

Physics pulses in the FCal have been measured directly using test beam data [103]. For each channel and event, the 40 MHz sampled signal was normalized to the pulse energy. The samples were then ordered in time, taking into account the event phase with respect to the clock. This provided large statistics which allowed for the reconstruction of the full, normalized pulse per channel. The pulse is reconstructed up to 160 ns only, because of the limited number of samples recorded during the test-beam. During the LHC Run 1 and Run 2 three waves were used, one for each of the three FCal layers and all three gains. This was sufficiently precise to meet the relatively relaxed performance requirements in the FCal. These pulses are combined with the noise autocorrelation extracted from regular pedestal runs to compute physics OFC. Note that for the FCal $M_{\text{phys}}/M_{\text{cali}} = 1$ since calibration data is not used to extract the ionization pulse.

The HEC physics pulses are predicted from the corresponding calibration pulses by using a semi-analytical model of the HEC readout electronics. This model represents the signal chain with a functional form derived from the set of zeros and poles in the cable and the pre-amplifier transfer functions. In the HEC, the calibration chain differs from the EM calorimeters in two main ways. First, the injection point of the calibration pulse is on the cell, versus on the signal collection boards. Because of this, there is no resonance $LC$ value introduced as there is for the EMB and EMEC. As well, due to the large capacity of a HEC cell, more than one calibration pulse is used for each cell. Each of these pulses is used to measure a different part of the cell’s electrodes, and is read out by a different preamplifier. Further details on the HEC pulse prediction can be found in References [104, 105].

In case of stable pileup conditions, e.g. with reasonably constant value of the average number of interactions per bunch crossing $\mu$, no frequent updates of the calibration constants related to the pulse amplitude reconstruction ($M_{\text{phys}}/M_{\text{cali}}$, OFC $a_i$ and $b_i$) are needed. As in Run 1 and
Run 2 operation [102], they could be refreshed once per week. In case of running periods with very different \( \mu \) values, dedicated OFC optimizations are to be foreseen.

### 6.2 Connection to energy calibration of electrons and photons

As mentioned in Chapter 3, the energy associated to electron and photon candidates is measured starting from a cluster of LAr cells in the electromagnetic calorimeters, where the response of each cell have been calibrated to the electromagnetic scale following the procedure outlined in Section 6.1.

The cluster energy is then corrected in subsequent steps in order to obtain the calibrated energy of the candidate, using a combination of simulation-based and data-driven correction factors described in detail in Reference [106]. The simulation-based calibration procedure is typically optimized for each data-taking period, in order to account for the specific detector configuration, and in particular to account for different material budgets associated to the evolving configurations of the inner tracking system. The uniformity corrections and the intercalibration of the longitudinal calorimeter layers are usually unchanged between data taking periods, unless important variations of the detector conditions (e.g. change in the high-voltage setting or the pulse amplitude reconstruction procedure) are introduced.

The calibration procedure is completed by applying data-driven correction factors to the calibrated cluster energy, meant to set the absolute energy scale and determined from \( Z \rightarrow e^+e^- \) events. The energy response resolution is also corrected in simulation to match the energy resolution observed in data. This correction is derived simultaneously with the energy calibration factors using \( Z \rightarrow e^+e^- \) events, by adjusting the electron energy resolution such that the width of the reconstructed \( Z \) boson peak in the simulation matches the width observed in data [107].

In the calibration procedure used by ATLAS during Run 1 and Run 2, the overall energy scale set with \( Z \rightarrow e^+e^- \) events is used for electrons and photons with transverse momenta spanning the whole detector dynamic range, from a few GeV to a few TeV (see Section 3.3 for details). In this configuration, it is therefore crucial that the response linearity of each LAr cell in the electromagnetic calorimeter be measured with great accuracy and corrected for in each readout gain. This approach to the overall energy scale calibration, using \( E_T \) independent correction factors, sets stringent requirements on the intrinsic linearity of the electronic calibration system. In order to meet the physics requirements discussed in Chapter 3, the integral non-linearity of the calibration board, discussed in the following section, needs in fact to be \( O(10^{-4}) \). As demonstrated in Reference [106], such an accurate calibration of the LAr cell response provides an overall linearity of the electron energy response of the order of \( 10^{-3} \) over the whole dynamic range in the central part of the detector and in the forward regions, where the residual differences are associated with a residual imperfection of the calibration of the LAr cell response. Similar performances could in principle be obtained also in the transition regions between the barrel and the endcaps: in Reference [106] the
obtained linearity in this region ranges in fact from $10^{-2}$ at low $E_T$ to $10^{-3}$, but the poorer performance is to be attributed to an imperfect modelling of the upstream material. In the momentum range separating the electrons from $Z$ decay to those from $W$ decays, a linearity of $10^{-4}$ can be achieved.

As discussed in Sections 6.1.2 and 6.1.4, the calibration system is also used to measure the pulse shape response of the calorimeter electronics and to evaluate the ionization pulse predictions used in the signal amplitude reconstruction. It is therefore crucial that the injected calibration pulses have a shape accuracy comparable to the overall linearity of the system, i.e. $O(10^{-4})$. This allows not only to correct for the residual non linearity of the readout electronics gain, but also to evaluate the pulse shape uncertainty over the dynamic range of interest. This is particularly important when an amplitude reconstruction optimized to minimize the impact of pileup is applied. During Run 1, and in particular when measuring the mass of the Higgs boson with the $H \rightarrow \gamma\gamma$ decay with $\sqrt{s} = 7$ TeV and 8 TeV data [108], it was in fact discovered that the residual pulse shape uncertainties, quantified on the order of $O(10^{-2})$, would have a non-negligible effect in the energy reconstruction of electrons and photons in the end-cap regions, when the highest electronic gain was used. When OFC optimized for pileup were introduced for the $\sqrt{s} = 8$ TeV data reconstruction, a bias in the energy reconstruction in the first layer of the EM calorimeter was observed for cells reconstructed in high gain [109], increasing from $0$ at $\eta = 1.8$ to approximately $5\%$ at $\eta = 2.4$. This bias is to be attributed to the ratio of the electronics noise over pileup noise not being the same for different electronic gains: applying an OFC optimization to reduce the total noise leads in fact to significantly different coefficients applied to the time samples in different gains. A systematic uncertainty on the predicted ionization pulse, used to compute the coefficients, induces therefore a gain-dependent bias on the energy measurement. This bias was treated as a subdominant source of systematic uncertainties in the measurement of the Higgs boson mass [106, 108], absorbed in the 0.1% uncertainty associated with the intercalibration of the calorimeter longitudinal layers. On the other hand, it is expected to become more important at larger pileup values for similar pulse shape uncertainties and would therefore need to be properly estimated and corrected for.

6.3 Calibration board

6.3.1 Motivations for upgrading

The calibration boards [84] are used to inject accurately calibrated signals directly onto the calorimeter cells inside the LAr cryostat. Calibration boards are placed in each LAr Front End Crates (FEC) and distribute their adjustable currents through the feed-through (FT). The only exception are the forward calorimeters, for which the signals are sent directly to the input of the FEB. The calibration board has 128 channels, referred to as calibration lines. Each calibration line injects charge simultaneously onto a fixed number of channels, this number
varying from 1 to 32 depending on layer and detector, according to specific injection patterns optimized for each readout layer. Each FEB and calibration board can be addressed with the served FT number, and a number labelling the slot occupied on the FEC and associated to the corresponding FT.

The analog part of the present calibration board was designed using DMILL technology and radiation qualified to levels which are compatible with HL-LHC: in principle, the present board could therefore be used for the LHC Run 3. However, the number of spare components and boards currently available is limited, and, since the DMILL technology is not available anymore, no additional components could be manufactured to repair the current boards in case of failure. Additionally, control of the current boards is done through the SPAC protocol, which will not be available in Phase-II, and replacing only the digital part of the board is not feasible. Finally, the current boards use dedicated voltage lines, which will need to be modified to be compatible with the Phase-II FEB voltage power distribution scheme.

All these considerations lead to a need for the replacement of the current calibration boards.

6.3.2 Principles of operation and requirements

The calibration board aims to produce a pulse with a shape as close as possible to the ionization pulse generated by electromagnetic showers in the detector. While the latter is to first order a triangular pulse, described by the typical drift time in the LAr gap, the difficulty of generating a true triangular pulse with an electronic circuit was originally handled by opting to produce an exponential pulse, with the decay time trimmed to approximate as much as possible the property of the desired triangular shape, at least in the initial portion of the pulse [84]. Even after this optimization, the residual difference in shape between the physics-induced ionization pulse and the calibration pulse needs to be corrected; this can be done by directly measuring the calibration pulse properties and using them in the electronic calibration procedure [85]. The new calibration board will similarly produce an exponential pulse with properties comparable to the current ones, assuming that the electronic calibration procedure could proceed as in Run 1 and Run 2.

The use of fast shaping for the ATLAS calorimeter implies the need to distribute the calibration signal directly at the input of the detector cell, and not at the input of the preamplifier located outside the cryostat. A schematic of the principles of the calibration system is presented in Figure 6.1, where the main components on the calibration board and inside the LAr cryostat are presented. In order to avoid any active element in the cryostat, a voltage-driven system was chosen for the present calibration board. Since no changes are foreseen inside the cryostat, a similar approach will be used for the new calibration board.

In the voltage-driven calibration system, an exponentially decaying voltage signal is made from a precise DC current $I_{DAC}$ by using an inductor $L$. By default the transistor $Q_1$ is on, and the current is flowing in the inductor. When $Q_2$, the command transistor, is closed, the current is diverting to the ground cutting $Q_1$ off. The magnetic energy stored in the
inductor is transferred to the resistance $R_0$, and the cable produces a fast voltage pulse with an exponential decay:

$$-R_0 I_p e^{-\frac{L}{R_0} t} = -R_0 I_p e^{-\frac{t}{\tau_{\text{cal}}}}$$

where $\tau_{\text{cal}} = \frac{2L}{R_0}$. This signal is propagated inside the calorimeter with a cable of impedance $Z_0 = R_0$ terminated on both ends on a per-mille precision resistance network equivalent to $R_0$, in order to reduce any reflection of the signal. The amplitude accuracy is therefore given by the output of the calibration board and the calibration resistor in the cold. As the cable is terminated at both ends, the amplitude does not depend on the cable characteristic impedance to first order. The component providing the inductance $L$ usually has a small resistive component $r$ that alters the exponential waveform baseline. When this is taken into account, the calibration pulse takes the form [85]:

$$-R_0 I_p \left( (1 - f_{\text{step}}) e^{-\frac{t}{\tau_{\text{cal}}}} \right)$$

where $f_{\text{step}} = \frac{r}{r + \frac{L}{R_0}}$, $f_{\text{step}} \in [0, 1]$, and now $\tau_{\text{cal}} = \frac{L}{r + \frac{L}{R_0}}$.

Based on the experience with the present system and the new preamplifier needs, some of the requirements of the calibration system are revisited, while the overall design remains quite similar to the existing one. In particular:

- the integral non-linearity of the calibration output needs to be better than 0.1% to correct the FEB response accurately;
• the uniformity between channels needs to be better than 0.25%;
• the calibration pulse rise time needs to be below 1 ns.

The major changes with respect to the present design are listed below.

1. In some regions of the calorimeter, 1 mA and 5 mA preamplifiers will be replaced by, respectively, 2 mA and 10 mA preamplifiers in order to avoid saturation (see Chapter 7). To calibrate over the necessary dynamic range, the calibration system should deliver pulses of at least 7.5 V. To deliver signals up to 7.5 V, the standard CMOS technologies (e.g. 65 or 130 nm) cannot be used, since they are limited to 3.3 V. The proposed alternative is an HV-CMOS technology to implement the high-frequency switch ASIC: preliminary simulations of the high-frequency switch circuit, represented in Figure 6.1 by the transistors $Q_1$ and $Q_2$, are presented in Section 6.3.4 using the XFAB XT018 technology.

2. While the pulse decay times ($\tau_{cal}$) were specified to be within ±2% to ensure a negligible dependence on the amplitude after shaping, the electronic calibration procedure currently corrects for this effect by directly measuring $\tau_{cal}$ and $f_{step}$ [85]. Consequently, ±5% inductances can in principle be used.

3. Keeping a low offset and small injected charge are some of the main difficulties of the calibration switch [84]. The LAr calibration data collected during Run 2 are analysed in Section 6.3.3 to quantify the impact of the offset and injected charge of the present calibration board on the energy response calibration, and used to specify the requirements of these quantities for the new card.

4. The current board includes eight delay chips with 1 ns steps to make the calibration pulses synchronous (correcting for different cable lengths) and measure waveforms that are needed for the determination of the optimal filtering coefficients. However, these chips have not been used as the timing adjustment has been performed during Run 1 and Run 2 via the TTC system. A similar approach is foreseen for Run 3, and delay chips are thus not planned for the new version of the calibration board. The lpGBT system will replace the TTC distribution currently used for the calibration delay runs.

5. The present calibration board uses one 16-bit DAC ASIC whose voltage is distributed on the PCB to 128 switches. In order to keep an excellent output uniformity across the board, the layout of the signals is quite complex, and a different implementation is proposed, integrating one DAC per channel in the switch ASIC.

6. The lpGBT system will replace the SPAC control system used on the present board.

Figure 6.2 schematically shows the foreseen schematics of the new calibration board. The components grouped represented in orange boxes will be realized as an ASIC in the HV-CMOS technology discussed in Section 6.3.4. The board will receive the clock and control
signals via the new lpGBT system. The drivers injecting the rectangular command pulses onto the switch will be selected as COTS.

### 6.3.3 Calibration pulse properties

The experience with the current calibration board has shown that, even if the DAC input is set to zero, an output signal is observed due to the unavoidable parasitic couplings on the fast transistors used in the switch to select the channel or build the exponential signal. This output signal was observed to be initiated by a positive spike, referred to as *command feed-through*, appearing when the command pulse is applied to the transistor $Q_2$ and correlated with the collector-base capacitance, followed by a negative spike, referred as *parasitic injected charge*, having a charge about three times larger than the previous effect, and associated to the capacitive coupling between the collector and the emitter of $Q_1$. These two effects are strongly anti-correlated, and behave as a slow first derivative of the signal [84].

The effect of this parasitic pulse after shaping is typically of a few hundred MeV at the peak of the signal, for a cell of the middle calorimeter layer. If not properly taken into account, its impact on the signal reconstruction could potentially introduce a non-linearity in the calibrated energy response of a few per-mil. In the following, the calibration data collected with the current calibration board between end of 2015 and beginning of 2017 are analysed to estimate the size of the residual bias associated to this parasitic pulse after the treatment in the signal reconstruction procedure.

**Analysis of time stability of Ramp run intercept**

Ramp calibration runs are routinely taken by injecting the detector with pulses of increasing amplitude, and measuring the corresponding response by mimicking the full signal reconstruction procedure. The response of the readout electronics is parameterized in Run 1 and Run 2 with a linear function, describing the evolution of the pulse peak, measured in
ADC counts, as a function of the injected current, measured in units of DAC. Details of this procedure are discussed in Reference [110].

The linear parameterization of the electronic response includes a constant term, potentially different from zero for when the response is extrapolated to no injected current (DAC = 0). This intercept term in the ramp fit is associated both to the command feed-through and parasitic injected charge, and, to a lesser extent, to the small non-linearity of the readout electronics that is not completely captured by the linear fit. The stability over time of the intercept term is therefore an important indicator of the quality of the calibration board switch circuit.

Ramp runs taken between the end of 2015 and the beginning of 2017 are analysed to verify the stability of the intercept term in time [111]. Runs taken in high electronic gains have the largest sensitivity to the intercept term, and are used in this analysis. The average value of the reconstructed calibration pulse amplitude $A_{\text{max}}$, corresponding to an injected current associated to a given DAC value, are fitted as:

$$A_{\text{max}}[\text{ADC}] = A_0 + A_1 \times \text{DAC}$$  \hspace{1cm} (6.8)

Figure 6.3 shows an example of the time stability of the intercept parameter $A_0$ for a selection of ten cells in the LAr Barrel Middle layer, corresponding to two distinct calibration lines (line 4 and 5 in FT 0). Similar results are obtained for all pulsed cells in the LAr EM Barrel and Endcaps. As expected, the intercept parameter $A_0$ in high gain groups by calibration line because of their correlation with the line command feed-through and parasitic injected.
charge. In general, all lines show an excellent time stability, and no significant drift is observed even for those lines sporting the largest values of the intercept parameters [111].

Comparable performance would need to be achieved by the new calibration board, in particular for what concerns the parasitic injected charge and command feed-through. The design of the high-frequency switch will determine the amplitude and impact of the command feed-through and parasitic injected charge on the future signal reconstruction. The requirements listed in Reference [84] will therefore be used as reference, while a potential drift under irradiation will be studied with test structures discussed in Section 6.3.4.

Analysis of small-DAC delay runs

In order to better understand the difference of intercepts between calibration lines observed in the analysis described in the above section, dedicated Delay runs [110] were taken in 2017. In these runs, additional values of injected current, corresponding to small DAC settings, are injected into the detector cells, and the corresponding pulses are recorded. The DAC values used are 5, 10, 15, 20, 25, 30, 100, 250, 500, 750, with the resulting pulse recorded in high gain. Using these pulses, it is possible to parameterize the ADC response as a function of the injected DAC value for each delay time, and to therefore obtain the evolution of the ramp parameter, either in a linear or quadratic parameterization, as a function of time. This analysis, also described as a Master Waveform approach, allow to study the evolution of the residual injected pulse for DAC = 0 as a function of time. In the following, a quadratic parameterization of the dependence of the ADC response as a function of the DAC values is used, in order to also explore possible non-linear effect that would not be measured by the simpler linear ramp fits discussed in the previous paragraph:

\[
A(t)[\text{ADC}] = A_0(t) + A_1(t) \times \text{DAC} + A_1(t) \times \text{DAC}^2
\]  

(6.9)

where \(A_0(t)\) is measured in ADC counts, \(A_1(t)\) in ADC DAC\(^{-1}\), and \(A_2(t)\) in ADC DAC\(^{-2}\).

Figure 6.4 show the results of the Master Waveform analysis of the special delay run using the quadratic parameterization of Equation 6.9 for a selection of cells in the EM Barrel Middle and Back layers. As expected, the \(A_0(t)\) curve resemble the expected shape of the command feed-through and parasitic injected charge [84], while the \(A_1(t)\) represent the average pulse shape scaled by the electronic gain. The \(A_2(t)\) shape correlates with the \(A_0(t)\) evolution: if the ADC outputs corresponding to low DAC inputs are strongly disturbed by the parasitic injected charge, the second-degree term \(A_2(t)\) would in fact tend to account for part of the effect.

The presence of the command feed-through and parasitic injected charge is currently accounted for in the signal reconstruction procedure by ignoring low DAC pulses in the ramp linear fit, and correcting for the fit intercept when calibrating the electronic response effect [110]. There might be an additional affect associated to the distortion of the calibration pulse shape associated to the feed-through and parasitic injected charge, that could bias
Figure 6.4: Master Waveform analysis of the special delay run using the quadratic parameterization of Equation 6.9 for a selection of cells in the EM Barrel Middle (left) and Back (right) layers: $A_0(t)$ (top), $A_1(t)$ (middle) and $A_2(t)$ (bottom) coefficients. The results correspond to cells sharing the same calibration lines (4, 5, 6, 21, 20, 7 in FT 28 for Middle layer; 46, 31, 28, 44, 29 in FT 20 for Back layer). Middle layer cells are connected to FEB in FT 28 and slot 11, Back layer cells to FEB in FT 20 and slot 9.

Chapter 6: Calibration
the measurement of the electronic gain through the bias induced on the calibration OFC computed from a pulse corresponding to a specific DAC value, that would suffer from the command feed-through and parasitic injected charge in a different way than the smaller DAC pulses. In order to estimate the impact of this effect, the \( A_0(t) \) pulses obtained by the Master Waveform analysis are subtracted from the ramp pulse at all DAC values, and the ramp fit is performed again to compare the obtained electronic gain with the default values. Differences smaller than 0.01\% are observed for the linear gain parameter \( A_1 \).

The values of command feed-through and parasitic injected charge in the current calibration board are therefore tolerable, and the current electronic calibration procedure is capable to correct for these effects. The requirements listed in Reference [84] will therefore be used as reference in the development of the new high-frequency switch.

### 6.3.4 Characterization of high-frequency switch ASIC technology

As mentioned in Section 6.3.3, the main difficulty in realizing the high-frequency switch is minimizing the parasitic couplings between the transistors \( Q_1 \) and \( Q_2 \) in order to avoid an excessive parasitic signal. Any inductive path, either between the connection between the two transistors, in case the command transistor \( Q_2 \) is implemented as an external high-frequency transistor, or associated to the gate of \( Q_1 \), can produce a resonant behaviour on the circuit when coupled with the capacitive coupling on the command transistor, resulting in a ringing oscillation superimposing on the output pulse especially important at small DAC values.

The XFAB XT018 (180 nm) technology [86] is chosen to realize the calibration board ASIC, since it is the only HV-CMOS technology readily available to the ATLAS Collaboration. The feasibility of realizing a high-frequency switch satisfying the requirements discussed above using the XFAB XT018 technology is studied with simulation of the basic structure of the circuit, by assuming different scenarios for the parasitic connection between the switch transistors. Figure 6.5 shows the generic schematic used for the switch simulation, while Figure 6.6 shows the actual implementation for the simulation studies in XFAB XT018, including the parasitic components that could affect its behaviour. The potential inductive path between the transistors is implemented as \( L_{\text{drain}} \); the possible inductive behaviour of \( Q_1 \)’s gate is implemented as \( L_{\text{gate}} \), while \( Q_1 \) resistive path enters the simulation as \( R_{\text{gate}} \).

Figure 6.7 shows the result of the switch simulation for a configuration with \( L_{\text{gate}} = 0.5 \text{ nH} \), \( R_{\text{gate}} = 0 \), \( L_{\text{drain}} = 0 \), and \( C_{\text{load}} = 10 \text{ pF} \). The output voltage is shown as a function of time for increasing input currents. The ringing effect is clearly visible on top of the parasitic injected charge. Figure 6.8 shows the result of the switch simulation for a configuration with \( L_{\text{gate}} = 3 \text{ nH} \), \( R_{\text{gate}} = 5 \text{ \Omega} \), \( L_{\text{drain}} = 0 \), and \( C_{\text{load}} = 10 \text{ pF} \). This configuration corresponds to a larger version of \( Q_1 \), that might be needed to guarantee the required output range (up to 7.5 V, and thus 300 mA). The ringing frequency is reduced, while larger command feed-through and injected charge are observed.
Figure 6.5: Generic schematic used for the simulation of the calibration board high-frequency switch.

Figure 6.6: Implementation of the calibration board high-frequency switch for its property simulation in XFAB XT018.
Figure 6.7: Result of the high-frequency switch circuit simulation in XFAB XT018 technology, corresponding to the $L_{\text{gate}} = 0.5 \, \text{nH}$, $R_{\text{gate}} = 0$, $L_{\text{drain}} = 0$, and $C_{\text{load}} = 10 \, \text{pF}$ configuration.

Following the results of this simulation, variants of HF switches will be integrated, both with internal NMOS transistor and with external Ne856 transistor to study the ringing effect in different configurations. The same structures will be used to establish the radiation hardness of the XFAB XT018 technology.

6.3.5 Radiations hardness considerations and DAC development

Being located in the crate on the detector cryostat, the calibration board ASIC will need to withstand the radiation level foreseen in that location. The technology of choice for the HF switch and the 16-bit DAC will have to qualify as rad-hard. The radiation hardness issue is different for the HF switch and the DAC:

- **HF switch.** As discussed before, this component needs to be designed in a HV technology, and the XFAB XT018 technology is the preferred choice. On the other hand, this technology is not validated for radiation hardness, and tests will be needed to ensure that the switch can withstand the foreseen dose levels. The risk that might not happen are very low: on one hand, the technology characteristic themselves (gate thickness, Deep Trench Isolation) are very promising in achieving the needed radiation tolerance; on the other hand, the HF switch circuit itself is not supposed to be very sensitive.
Figure 6.8: Result of the high-frequency switch circuit simulation in XFAB XT018 technology, corresponding to the $L_{\text{gate}} = 2 \text{nH}$, $R_{\text{gate}} = 5 \Omega$, $L_{\text{drain}} = 0$, and $C_{\text{load}} = 10 \text{pF}$ configuration.

to radiation, since it is not prone neither to $V_T$ drift under irradiation nor to leakage currents.

- **16-bit DAC.** This component delivering the DC current to the HF switch is potentially sensitive to radiation: we therefore foresee two options to face the issue:

1. Develop a DAC prototype in XFAB 018 and test it for radiation hardness in order to fully qualify the HV technology.

2. Develop a DAC prototype in TSMC 130 nm, a technology that is already qualified for radiation hardness and for which we already have experience for other ASIC in this project, and interface it to the HF switch developed in XFAB 018 via a current mirror (Figure 6.9).

The second option requires some care in order to achieve the needed uniformity of the calibration lines, but would dramatically mitigate the risk associated to the radiation hardness, and would also allow to reduce the production costs.
6.3.6 R&D milestones

Key elements of the switch will be designed by the second half of 2017, in order to test different solutions (e.g. different transistor sizes and routing) and their impact on the circuit ringing behaviour. A first submission of these test structures is scheduled at the end of September 2017, while a dedicated testing board will be designed by the end of 2017. The turnaround for the XFAB XT018 engineering runs is 6 months, the switch test structure are therefore expected by March 2018, when they could be packaged and added to the testing board. Irradiation studies to gauge the radiation hardness of these test ASICs will be conducted between March and July 2018. During the same period, measurements of the pulse properties of the different switch implementations will also be performed.

The development of the 16-bit DAC will happen current 2018. At the time of writing solution 2. seems preferred: a DAC prototype in TSMC 130\(\mu\)m is begin developed and will be submitted for production by June 2018, and will ideally be ready by August 2018 to be test for functionalities and radiation hardness.

Pending the successful results of the switch and DAC tests, a complete channel design is scheduled for the end of 2018, with a prototype board integrating 8 to 16 channels available for testing from Summer 2019. We consider the possibility of needing of an iteration in the design of the 16-bit DAC, that would result in a delay of 6 to 9 months in the schedule.

At the same time, studies will be conducted to assess the possible alternative calibration approaches should the use of non-HV ASIC technology be imposed by the failure of qualification of XFAB XT018 and alternative HV technologies. These approaches comprise the design of a double pulser circuit capable to separately cover the full dynamic range and the offline extrapolation of the calibration obtained by a pulser circuit only capable to deliver...
up to 5 V. While neither of these approaches is desirable, they will anyway be explored to guarantee a viable alternative in case of failure of the preferred option. We plan to have results capable to assess the loss in performance should any of these options be chosen by the end of 2018. In case of failure of the radiation qualification of the XFAB XT018 technology, the channel redesign will require from six additional months. A submission of an alternative design in non-HV technology could take place by mid 2019.

Over the 2018 period, studies are also foreseen to investigate whether additional feature on the card can improve the electronic calibration procedure, in particular that of cell with large capacitance or impacted by large cross-talk. Possible options include the implementation of a second pulser circuit, with different pulse rising time or alternative \( \tau_{\text{cal}} \) value; the inclusion of system to measure the pulse forms at the card output, to be directly used in the procedure to predict the ionization pulses from the shaped calibration waveforms.

In case of successful validation of the XFAB XT018 technology and of the channel development, a first 128-channel prototype of the calibration board is scheduled to be completed in 2020, ideally at the beginning of the year, but potentially later should an iteration in the DAC design be need. A FDR would be therefore scheduled current 2021, and a PRR in the first half of 2022.
The front-end readout of the LAr calorimeters will be accomplished by Front-end Boards, abbreviated FEB2, mounted in the existing Front-end Crates on the LAr cryostat. The FEB2 will contain a number of commercial-off-the-shelf (COTS) and ASIC devices, water cooled by six under-pressure loops per calorimeter face. The FEB2 will be connected to the off-detector readout through optical fibres. Section 7.1 describes the overall FEB2 design and individual component development and prototype testing efforts. The specifics of the front-end electronics implementation for the HEC, are also discussed. Finally, the plans for the cooling of the front-end electronics, as well as the mapping to optical fibres and their routing, are presented in Sections 7.2 and 7.3, respectively.

### 7.1 Front-end board

The front-end readout electronics will be implemented on the FEB2, which will replace the current FEB boards. As for the current FEBs, each FEB2 will handle 128 calorimeter channels, and a total of 1 524 FEB2 boards will be required to read out the entire LAr system.

A block diagram illustrating the high-level architecture of the FEB2 board is shown in Figure 7.1. The dataflow, from bottom to top of the figure, is as follows:

- Two input connectors bring 64 calorimeter signals each from the crate baseplane to the FEB2 board;
- Preamplifier/shaper ASICs each handle four (or possibly eight) channels, terminating the input lines, and performing analog processing on the signals, including providing amplification, splitting into two overlapping linear gain scales, and applying a \( CR-(RC)^2 \) shaping function;
- Octal ADC chips digitize both of the two gain-scale preamp/shaper outputs for four channels each. The ADCs operate at the bunch crossing frequency of 40 MHz and format their outputs, including eight digitized signal streams as well as one word with bunch crossing identification (BCID) information, into 16-bit words, and output them serially at 640 Mbps.
- IpGBT Serializer chips receive 14 streams of ADC outputs, and serialize them with a standard protocol into a single bit-stream at 10.24 Gbps.
• the serial lpGBT outputs are converted from electrical to optical signals and transmitted off-detector, using optical modules developed by the Versatile Link+ (VL+) project [91].

• in addition to this dataflow, additional functionality that is required includes distribution of Clock and Control information, and the formation of analog sums for use in the trigger system.

![Diagram](Figure 7.1: Block diagram illustrating the overall architecture of the FEB2 board.)

The following sections provide more information about the main blocks of FEB2 functionality, with the analog processing described in Section 7.1.1, followed by the digitization in Section 7.1.2, the serialization and transmission of the digital data in Section 7.1.3, the clock and control distribution in Section 7.1.4, and the trigger summing in Section 7.1.5.

### 7.1.1 Analog processing

Analog processing is performed in two steps: the preamplifier provides an active termination of the input cables (both 25Ω and 50Ω versions are needed) and amplifies the calorimeter signals, which have a dynamic range of up to 16 bits. The second stage (shaper) has two...
purposes: first to transform the output of the preamplifier circuit to a multi-gain differential output capable of directly driving the input to the ADC, and second to add at least one stage of shaping to match the desired signal processing requirements. Multiple equivalent shaping stages can be added at a minimal cost in power. The baseline solution is to adopt the same CR-(RC)^2 shaping as the current system, but with the shaping time adjusted to account for the higher pileup level expected at the HL-LHC.

Both the preamplifier and the shaper will be implemented in a single ASIC. The preamp/shaper ASIC is expected to accommodate either four or eight calorimeter channels. In addition to the signal amplification and shaping, some “peripheral” circuits are needed, such as a test pulse generator, bias circuit, temperature sensor and configuration registers. A configurable summing circuit will provide Super Cell signals to the LTDB which will be installed during the Phase-I upgrade (see Section 2.4).

Multiple technologies are under investigation for the implementation of the preamp/shaper ASIC. Early investigations, including those documented in Reference [87], suggest that the required performance can be achieved using bipolar Silicon-Germanium (SiGe) processes, which allow high speed and low noise configurations but with relatively high power consumption. While the SiGe approach is kept as a viable backup solution, the focus of current developments is on CMOS technologies, which are more challenging in terms of meeting the analog performance requirements, including 16-bit dynamic range, but would offer lower power and other benefits. As described below, efforts are underway to implement preamp/shaper prototypes using the 130 nm and 65 nm CMOS processes of TSMC. The final choice between the various technologies will be determined based on the measurements of the performance achieved with the prototypes, and the resultant physics impact. A common preamp/shaper test system has been designed and produced, so that the various prototypes can be evaluated in a consistent manner.

Preamp/shaper development in 130 nm CMOS

The LAr preamplifier used on the present FEB is a current amplifier using the 0T scheme [88], built with discrete components. Such a scheme is difficult to integrate in an ASIC since it uses capacitors as large as 1 µF and resistances down to 2.4 Ω. Moreover, several preamplifier types are needed to accommodate the maximal input currents and input impedance, depending on the layer and pseudorapidity region. A new architecture is therefore proposed to provide a versatile 130 nm CMOS ASIC coping with the requirements of all preamplifier types. The schematic of this new preamplifier design is shown in Figure 7.2(a). This new line termination preamplifier, featuring electronically cooled resistance, is made around a resistor (R_0), a voltage amplifier and a Super Common Gate amplifier (SCG). This architecture has two main advantages:

- the voltage gain is made using capacitors (C_1 and C_2 and G=C_1/C_2), which are noiseless, and the equivalent noise of R_0 is divided by the square of the gain,
4kTR₀/(1+|G|^2), leading to a noise level equivalent to that of a resistance of less than 10 Ω;

- the input impedance is given by \((R₀+Z_{in\ (SCG)})/(1+|G|)\). The 25 Ω or 50 Ω impedance, given mainly by \(R₀\), can be precisely tuned to match the cable by adjusting the capacitor ratio. The feedback also ensures that the input impedance does not vary with the signal amplitude.

The maximal preamplifier input current is given by the resistance \(R₀\) while the resistance \(R_f\) is used to define the high gain dynamic range. For large detector currents, the saturation of the high gain affects the linearity of the low gain preamp. To avoid this effect, a discriminator on the low gain signal amplitude is used to activate a switch that shorts \(R_f\), keeping the transistors properly biased in the current conveyor.

The preamplifier design was implemented in a chip called LAUROC0 (Liquid Argon Upgrade Readout Chip), a diagram of which is displayed in Figure 7.2(b). The LAUROC0 chip contains eight channels with different transistor sizes and different options for the dynamic range/gains. The chip was submitted to a TSMC 130 nm MPW run.

Figure 7.2: (a) Schematic illustrating the design of the line terminating preamplifier. (b) Layout of the LAUROC0 chip.

The preamplifier was simulated using the 130 nm CMOS kit from TSMC, with the parameters defined in Table 7.1 for the 25 Ω and 50 Ω configurations. The results from simulation fulfill
the ATLAS requirements:

- For the 50Ω configuration, the input noise is about 0.36 nV/√Hz, equivalent to 8Ω. At the output of the shaper this gives an ENI of 46 nA. For the 25Ω configuration, an ENI of 150 nA is expected. These numbers are similar to the noise performance of the preamplifier used on the present FEB. The noise is dominated by R₀ and the NMOS transistors.

- The integral nonlinearity is about 0.1% for the high gain range and 0.2% for the low gain range, as illustrated in Figure 7.3.

- The impedance is flat versus input frequency from 10 kHz to 10 MHz and remains constant within a few Ω as a function of the input current, as shown in Figure 7.4.

Table 7.1: Parameters used in the simulation of the LAUROC0 preamplifier. An ideal cable (25 ns propagation time) and an ideal CR-(RC)^2 shaper with a time constant of 15 ns are used behind the preamplifier.

<table>
<thead>
<tr>
<th>Parameters</th>
<th>25 Ω</th>
<th>50 Ω</th>
</tr>
</thead>
<tbody>
<tr>
<td>R₀</td>
<td>100Ω</td>
<td>500Ω</td>
</tr>
<tr>
<td>Gain G</td>
<td>3</td>
<td>9</td>
</tr>
<tr>
<td>Max current</td>
<td>10 mA</td>
<td>2 mA</td>
</tr>
<tr>
<td>R.vocab</td>
<td>1 kΩ</td>
<td>5 kΩ</td>
</tr>
<tr>
<td>Detector capacitance</td>
<td>1.4 nF</td>
<td>400 pF</td>
</tr>
</tbody>
</table>

Preliminary measurements of the LAUROC0 chip have been performed. Up to now, only one 25Ω channel has been examined. The measurement results include:

- The linearity of the 25Ω low gain, shown in Figure 7.5(a), is better than 0.5% up to 7 mA, with a small non-linearity at the end of the dynamic range. The high gain’s non-linearity is within a few per-mil.

- The impedance is within a few Ω as a function of the input current, as expected. As shown in Figure 7.5(b), the input impedance can be tuned easily with the C<sub>2</sub> capacitor.

- The ENI has been measured to be about 300 nA, a factor two larger than expected. Larger noise has been traced back to come from the input transistor. A new transistor was designed, submitted and a 30% reduction in the noise of this transistor was measured. A new version of LAUROC will be submitted with this improved transistor design.

Deeper characterization of all channels of the LAUROC0 chip have been conducted, followed by irradiation campaigns, to prepare for submission of a new chip that will also include the shaper stage.
Preamp/shaper development in 65 nm CMOS

A preamp/shaper design has been developed in the 65 nm CMOS process from TSMC. To optimize the noise performance, the preamplifier uses a fully differential design with passive feedback, as shown in Figure 7.6(a).

A prototype ASIC, dubbed HLC1, was submitted for fabrication in March 2017 and received in July 2017. The HLC1 layout is shown in Figure 7.6(b). It includes preamplifier, shaper, summing and peripheral circuits. The shaper has four poles and one zero for its anti-aliasing filter. The analog front-end has programmable termination to cover both 25 Ω/10 mA and 50 Ω/2 mA detector impedance. At the same time, a three-bit programmable adjustment (±3% steps, up to ±5 Ω) is available to fine-tune the termination. Two different gains (10 mA/600 μA or 2 mA/60 μA) can be read out simultaneously to provide full dynamic range coverage and optimum resolution for small signals. Programmable peaking time (30 ∼ 50 ns) in the shaper stage can be used to optimize the detector response and noise. The design has a built-in ADC driver to interface to COTS or ASIC ADCs directly for evaluation tests. Three summing outputs are available to provide summing of either four or eight input channels. This will cover all possible configurations of Super Cell signals to the LTDB. The original aim for the test chip was to provide summing for eight input channels, however, the summing of four channels is a more natural number for the FEB2 mapping and, in addition, would facilitate the cooling of the chips. Finally, a built-in pulse generator and mask bit for individual channels can be used to calibrate the electronic response and perform crosstalk studies.
Figure 7.4: LAUROC0 preamplifier impedance, as obtained in simulation for the $25 \, \Omega$ configuration, as a function of (a) the frequency and (b) the input current.

Figure 7.5: (a) Measurement of the LAUROC0 $25 \, \Omega$ preamplifier integral nonlinearity. (b) Tuning of the LAUROC0 impedance, using the $C_2$ capacitor. Measurements are shown in green, while the calculations are shown in red.

The prototype HLC1 chips have been fabricated and delivered in July 2017. It is packaged in a 128-pin $14 \, \text{mm} \times 14 \, \text{mm}$ LQFP package. Test boards have been assembled with HLC1 chips for the evaluation test, as shown in Figure 7.7. The HLC1 test board will be mating with FETB as shown in Figure 7.11, to be tested with a common analog front-end test stand, described below.

Measurements of the HLC1 chip have been carried out in the second half of 2017. The functionality has been checked and the performance has been characterized with the common
Figure 7.6: (a) Fully differential preamplifier design implemented in the HLC1 chip. (b) Layout of the HLC1 preamplifier/shaper test chip.

analog front-end test stand described in the following subsection. A summary of the test results are below.

- The main functionality of the HLC1 chip has been verified, including the dual gain outputs with a differential driver for the ADC interface, the programmable peaking time, the programmable termination with fine adjustment, the 4-ch and 8-ch summing outputs and the internal pulser generator. The output signal of one HLC1 channel in the low gain configuration with four peaking time settings is shown in Figure 7.8(a).

- The ENI has been characterized and is shown in Figure 7.8(b). The ENI for the high gain output with a peaking time of about 50 ns is approximately 225 nA with 1.5 nF Cd and a 25 Ω termination, and approximately 82 nA with 330 pF Cd and a 50 Ω termination.

- The integral nonlinearity (INL) has been measured to be better than 0.3% for the full dynamic range in the high gain setting. In the low gain setting the INL is better than 0.3% for 90% of the full dynamic range, and better than 1% for the full dynamic range. The INL of the high gain output of one HLC1 channel with a 25 Ω termination is shown in Figure 7.9(a), and the INL of the low gain output of the same channel is shown in Figure 7.9(b).

- The crosstalk has been measured to be less than 0.5% for the 25 Ω termination, and less than 2.6% for the 50 Ω termination outputs.

A few issues were identified during the testing and will be further investigated and addressed in the next revision of the chip.
• The operation of the neighbouring channels of HLC1 has large impact on the noise performance of the channel under test.

• Summing output has low saturation point (approximately 0.1 mA) for 50 Ω termination inputs.

• One of four configuration bits of the internal pulse generator is not functioning as expected.

Analog front-end test stand

A common test stand, shown schematically in Figure 7.10, has been developed for both the 65 nm and 130 nm preamp/shaper ASICs, aiming to get preliminary test results by the end of 2017. The test stand consists of a digital readout board, Front-End Test Board (FETB), a front-end mezzanine to house the analog front-end ASIC, and a toy calorimeter to emulate the detector capacitance.

The front-end mezzanine will be different for the two ASICs, since they have different requirements for power input and signal output. The input and output connectors of the front-end mezzanine have been chosen to facilitate the test of Axon cold cables with either...
Figure 7.8: (a) The output signal of one HLC1 channel in low gain configuration with four different peaking time settings. (b) The ENI for high gain output with peaking time setting of 1 (about 50 ns) is approximately 225 nA with 1.5 nF Cd and 25 Ω termination, and approximately 82 nA with 330 pF Cd and 50 Ω termination.

Figure 7.9: (a) The INL of the high gain output of one HLC1 channel with 25 Ω termination. (b) The INL of the low gain output of one HLC1 channel with 25 Ω termination.
Figure 7.10: Block diagram of the analog front-end ASIC evaluation test stand. In the diagram, DIFF x 16 represents 16 differential pairs, SIN x 12 represents 12 single-ended signals. The ADC driver circuit consists of and ADA4899 and an ADA4932. Finally, two calibration pulse generators are implemented; the first one is based on the LAL low-offset amplifier ASIC and the second one is based on the commercial low-offset amplifier OPA735.

25 Ω or 50 Ω impedance, and also provide a common interface to the digital readout board FETB. The FETB has a built-in calibration circuit to inject a test pulse in the toy calorimeter, an ADC driver circuit and two AD9249 chips, which are 16-channel 14-bit 40 MSPS ADCs. The ADC driver circuit can be configured as a shaper for performance studies.

There are in total 32 ADC channels available on FETB to digitize analog channels with two different gains, plus summing channels. Some ADC channels can be reconfigured to digitize either single ended or differential output signals from the ASIC. A picture of FETB is shown in Figure 7.11.

The control and data acquisition is realized with a Xilinx ZC706 FPGA evaluation board, which is used to send control signals to FETB and front-end mezzanine, and acquire data from ADC chips on FETB. The Zynq FPGA with embedded ARM processor on the ZC706 board makes the test stand versatile to be adapted to different analog front-end chips, with help of flexible software control. An analog front-end test stand with ZC706, FETB and
The two CMOS analog front-end ASIC designs are currently being evaluated. The plan is to evaluate the front-end performance of both ASICs with a common test stand, and converge on a single architecture for the analog front-end design.

**HEC Front-End**

For the HEC, the preamplification is already done inside the cryostat, using GaAs ASICs [25]. The amplified signals arriving at the FEB2 have opposite polarity than the other LAr sub-detectors, and therefore a special treatment of these signals needs to be considered in the design of the front-end ASIC. The range of the HEC signals at the FEB2 input is up to 0.75 V, corresponding to 15 mA current into a 50 Ω input impedance. A HEC-specific preamplifier on a common ASIC has to be designed, however, it could possibly be a modification of one of the preamplifier types used for the EMB.
Another HEC-specific feature is that the sampling ratio in longitudinal sections 3 and 4 (rear wheel) is a factor of two lower than in the first two sections. To keep the same conversion factor across HEC cells, an additional gain of 2 is introduced for the channels serving these sections. The mapping of HEC connections to the FEB2 boards requires that two amplifiers out of four have this extra gain. These two amplifiers can be channels 1 and 2 of FE ASIC or channels 3 and 4, depending which FEB2 side (bottom or top) the ASIC is placed on. If all the preamp/shaper ASICs are on the same side of the FEB2, then they can be hardware configured for fixed gain. If both sides of the FEB2 are used, then each preamplifier requires individual configuration of its gain. In this case, an additional 4 or 8 bits (if the ASIC handles 4 or 8 channels) must be added to the configuration register for gain selection.

In the present electronics, the analog signals from the HEC are processed by dedicated preshaper electronics [89]. The HEC preshaper implements signal inversion and provides two gains (DC gains of 6 or 12 for the front and rear HEC cells, respectively). In addition, the preshaper equalizes the signal rise time, by pole-zero cancellation adjusted for each type of readout cell (there are 51 different cell dimensions in the HEC). This shape equalization, as well as the double gain for rear cells, is needed to generate analog sums for the L0 trigger.

Special studies have been performed to quantify the errors in the total energy reconstruction in the case that the FE ASIC does not provide shape equalization. The conclusion is that the degradation of trigger sums is at an acceptable level, so pole-zero cancellation will not be
implemented in the FE ASIC. Another conclusion is that the double gain for the rear cells is critical for the trigger sums, and therefore must be implemented.

The baseline solution is to design a HEC version of the preamp/shaper ASIC, with a HEC-specific preamplifier block that provides signal inversion and the required gain (trans-impedance) values. Fine shape equalization will not be implemented. The rest of the ASIC, including the shaper and the analog summing circuit, will be the same as for the other LAr subdetectors. This HEC version of the preamp/shaper chip will be developed in one of the future iterations of the ASIC design and studies on more precise requirements are starting.

### 7.1.2 Digitization

The analog signal from each calorimeter cell will be digitized at 40 MSPS, synchronized to the LHC bunch-crossing rate. Studies of an option to digitize at 80 MSPS and use more refined digital filtering led to the conclusion that the possible modest gain in performance was outweighed by the cost and other implications of the resultant twofold increase in the data volume.

To cover the full 16-bit dynamic range, each channel will be digitized on multiple gain scales. The baseline solution is to use an ADC with a 14-bit dynamic range, in which case only two gain scales would be needed. The ADC requirements are summarized in Table 7.2. The ADC will need to meet the radiation tolerance requirements described previously and consume less than 100 mW of power per detector channel.

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>Technology</td>
<td>TSMC 65 nm or 130 nm</td>
</tr>
<tr>
<td>Channels/chip</td>
<td>8 preferred, 4 minimum</td>
</tr>
<tr>
<td>Sampling Frequency</td>
<td>40 MSPS</td>
</tr>
<tr>
<td>Dynamic Range</td>
<td>14 bits</td>
</tr>
<tr>
<td>Precision</td>
<td>11 ENOB</td>
</tr>
<tr>
<td>Power</td>
<td>&lt;100 mW/channel</td>
</tr>
<tr>
<td>Input</td>
<td>2 V differential</td>
</tr>
<tr>
<td>Output</td>
<td>E-link interface operating at 640 Mbps</td>
</tr>
</tbody>
</table>

Several approaches to the ADC issue are being explored in parallel, either the development of a full custom ADC design in 65 nm CMOS, or the possible development of an ADC that integrates in its core a commercially available “Intellectual Property” (IP) block, or the possible use of a COTS ADC chip. If the analog performance requirements can be achieved, the full custom design has a number of advantages, including low CORE cost, low power, and a design that can be fully customized to the LAr needs. The IP block approach
provides an intermediate approach, where one can try purchase and use critical blocks with proven analog performance, while still customizing the digital interface as needed. The COTS approach would have a significantly higher CORE cost, and require additional developments to integrate the commercial ADC chip into the overall FEB2 architecture, and is being investigated as a backup in case the other approaches are not successful. More details about these approaches are provided in the following three subsections.

**Full custom ADC development**

There is substantial experience in the LAr community in the development of custom ADC devices. For the Phase-I LTDB, a custom four-channel 12-bit ADC [112] was developed in a 130 nm CMOS process. This ADC uses an architecture of four pipeline stages followed by an 8-bit Successive Approximation Register (SAR) ADC block. The ADC has a latency of about 100 ns, and excellent linearity thanks to digital error correction of the redundant pipeline stages. Many of the lessons learned in the development of the Phase-I ADC in 130 nm CMOS are directly transposable to 65 nm technology.

Most ASIC developments for Phase-II are targeting the 65 nm CMOS process from TSMC. CERN has negotiated a frame contract for this process to be available on the Phase-II timescale, and its widespread use in the Phase-II community enables sharing of IP blocks, etc. A collaboration that grew out of the Phase-I ADC effort is now developing a custom ADC for Phase-II in the 65 nm process. Advantages facilitated by the higher speed of this process include lower power and the possibility to implement a 12-bit SAR. The main challenge is extending the dynamic range to 14-bits, particularly given the low value of only 1.2 V for the power rail.

After simulating a number of possible solutions, the 14-bit ADC architecture that was chosen is illustrated conceptually in Figure 7.13(a). Each preamp/shaper output is connected to a 14-bit ADC that is comprised of two main sections: a Dynamic Range Enhancement (DRE) block that determines the most significant two bits of the 14-bit digital code, followed by a 12-bit SAR block.

The design of the DRE is shown schematically in Figure 7.13(b). The input signal is sampled on two paths, one with unity gain and the other of gain four. A comparator determines which gain to use. The signal from the selected DRE gain is presented at the DRE output, which is connected to the input of the 12-bit SAR ADC block. The DRE design has been carefully optimized so that its output preserves the required 12-bit performance.

More details of the SAR design are shown in Figure 7.13(c). Following current state-of-the-art ADC development techniques, a two-stage SAR architecture is used, exploiting the high speed of the technology while maintaining the SAR input capacitance at a reasonable value. Since capacitor matching in this technology might not meet the precision required, the ADC will use bit redundancy, i.e. determine more bits than its actual output, and the redundant bits will be used to both calibrate the ADC and produce correct output codes.
Such procedures are well understood and applied to both pipeline [112] and SAR [113] ADCs using foreground or background calibration techniques. Single event effects mainly affect smaller capacitors, and an important goal of the forthcoming test chip will be to determine the SEU cross section as a function of capacitor size to ensure the final design meets the SEU specifications.

Figure 7.13: (a) Block diagram depicting the connection of one LAr channel to the preamp/shaper chip, followed by the 14-bit ADC comprised of DRE plus 12-bit SAR ADC. (b) Block diagram of the DRE architecture. (c) Block diagram depicting the two-stage SAR design.

An ADC testchip, dubbed COLUTA65V1, was designed and submitted for fabrication in May 2017 and received in September of 2017. The layout of the testchip, which includes one channel of DRE plus SAR, is shown in Figure 7.14, which also includes the layout of the testboard produced for testing the chip. The testboard allows precision performance testing of the DRE and SAR, both separately and functioning together as foreseen in the full 14-bit ADC architecture. An additional testboard (not shown) was produced to perform radiation testing of the chip, including both total dose measurements and also SEU tests.

The DRE and SAR blocks of the COLUTA65V1 were first tested independently. Measurements were made of the SAR precision using the sine-wave Fast Fourier Transform method. An effective number of bits (ENOB) of 11.6 bits at 20 MSPS (after calibration) is shown in
Figure 7.15(a). Similar measurements at 40 MSPS do not match the expected performance and additional testing and simulation indicates that the layout of the connection between the first SAR stage and the amplifier is not optimal. Similar results were observed with the DRE performance and again simulation indications improvements are possible in the layout. The next submission of the chip, planned for spring 2018, will incorporate this work in the iteration of the design. Both DRE and SAR were successfully integrated, and a simulated calorimeter pulse digitized by the full-chain is shown in Figure 7.15(b). The COLUTA65V1 was irradiated in October 2017 up to a TID of approximately 0.9 MRad, with no degradation in performance. Measurements of the SEU rate were also made, with promising preliminary results.

It is planned to iterate the ADC design and annually submit increasingly complete versions for prototyping, culminating in a full prototype being submitted in 2020.

![Figure 7.14: (a) View of the layout of the COLUTA65V1 ADC testchip, measuring 2 mm × 2 mm, and submitted for fabrication in May 2017. The main DRE and SAR blocks are indicated on the figure, as well as some of the secondary clock and control blocks. (b) Layout of the testboard (measuring 13.2 cm × 15.5 cm) designed to perform precision performance testing of the COLUTA65V1 testchip.](image)

**IP block option**

Development of an ADC chip that integrates a commercial ADC IP block is also being investigated. There are several IP blocks on the market with characteristics already meeting most of the requirements of the ATLAS LAr calorimeter upgrade (digitization speed, power consumption), and close to meeting the requirements in terms of effective number of bits. IP blocks either already exist or are close to being silicon-proven for the TSMC 65 nm and 130 nm technologies.
The use of a core ADC IP block shares with the full custom approach the advantage that it is possible to include in the overall ADC architecture the features required to integrate the ADC seamlessly into the FEB design. The IP block could also be tailored to the ATLAS radiation needs, such as minimizing the quantity of ancillary logic and introducing triple-redundant logic to minimize the sensitivity to SEE.

It is planned in the coming months to evaluate, on the basis of simulations and of data provided by the designers, the performance of existing IP blocks, and how far they could be customized to the ATLAS needs. To this end, several firms have been contacted and discussions are underway to set up a collaborative effort toward realizing a suitable IP block in 65 nm CMOS, with the goal to design a first test chip by the end of 2018.

**Commercial ADC option**

As part of a search for COTS ADC candidates for use in the Phase-I or Phase-II LAr upgrades, a number of commercial ADC chips were subject to radiation tests [114].

A promising candidate is Texas Instruments’ ADS5294 [115], an octal 14-bit ADC, fabricated in a 180 nm process and consuming, when operated at 40 MSPS, about 60 mW per channel from its 1.8 V power supply. The tests [114] show that this device could survive the integrated HL-LHC radiation levels. The on-chip digital logic is susceptible to single-event effects (SEE). The observed SEE events included transient upsets that corrupt the digital data, usually for one sample (and occasionally up to five samples) in either one or several
channels. In addition, Single Event Functional Interrupt (SEFI) events, which corrupt the configuration logic and thereby cause the ADC to stop functioning properly, were also observed. Recovering from a SEFI event requires that the device be re-configured, a process that takes about 5 µs.

One ADS5294 chip could be used to digitize the two gain scales of four calorimeter channels, so a total of approximately 50K ADS5294 chips would be required to read out the entire LAr system. For this highest HL-LHC instantaneous luminosities, the measured SEE and SEFI cross sections correspond (without safety factors) to roughly 10 SEE events and one SEFI event per minute in the complete LAr system. The system implications of coping with such events require further study. In addition, while the tests did not show any instances of more problematic events where it would be necessary to cycle the power to the ADC in order to recover, further testing to higher fluences would be required to more precisely specify the corresponding cross section, below the current upper limit of about an order of magnitude smaller than that measured for SEFI events.

The custom ADC development described previously is the baseline approach. However, should it prove not possible to achieve 14-bit dynamic range in the 65 nm design, the COTS ADC provides an attractive option to achieve the desired analog performance. In addition to further consideration being given to coping with the various upset rates, other issues to be factored into the choice include the higher CORE cost for the COTS ADC approach.

For the COTS ADC to be used, it would be necessary to develop a custom digital ASIC to interface the ADC to the lpGBT Serializer chip (see below). Tasks of this interface chip would include receiving each of the eight serialized ADC outputs at 560 Mbps (14 bits × 40 MSPS), reformatting the 14-bit ADC data into 16-bit words, transmitting those 16-bit words serially at 640 Mbps to the lpGBT, and generating and providing the associated BCID information. Special care would be needed since the ADC outputs use LVDS levels, with a common mode voltage of 1.25 V; therefore, the receivers on the interface chip would need to use higher voltage levels than the nominal 1.2 V power rail for 65 nm CMOS. Also, the interface chip would need to provide the logic required to map from the I2C interface provided by the lpGBT to control other devices to the Serial Peripheral Interface (SPI) protocol required by the COTS ADC.

The COTS ADC is being considered as a backup solution, in case the full custom and IP block approaches do not meet the performance requirements. Given the FEB2 schedule constraints, a decision of whether or not to use the COTS ADC would need to be made by 2020.

### 7.1.3 Serialization and data transmission

Both the custom ADC development and the COTS ADC option involve utilizing ADC chips that each digitize the data from four calorimeter channels. With the baseline choice to use two 14-bit gain scales per channel, each ADC will have eight outputs. Each 14-bit ADC
output will be formatted into a 16-bit word and serialized at a bit rate of 640 Mbps. Each 16-bit data word will include 14 bits of ADC data and a parity bit to provide error checking for that word. Given that each FEB2 board reads out 128 calorimeter channels, and that both gain scales will be read out for all channels, the resultant calorimeter data rate will be 256 data streams of 640 Mbps each, for a total data rate from each FEB2 board of 163.84 Gbps.

To guarantee the correct alignment of the calorimeter data, BCID information will also need to be provided for each ADC chip. It is assumed that, as in the current LAr readout, a Bunch Counter Reset (BCR) signal will be distributed once per LHC orbit, as part of the Clock and Control distribution described in the next section. The BCR will be received on each FEB2 board and fanned out to BCID counters implemented either in each custom ADC chip or, in the case of the COTS ADC, in each digital interface chip. These counters will locally generate the appropriate BCID information and insert this information into the data stream. The baseline solution is to include the BCID information, including also a Frame bit for alignment purposes and a Parity bit, in a 16-bit BCID word that will be provided in parallel to the corresponding ADC values.

The ADC data and BCID words need to be serialized and transmitted from the on-detector FEB2 boards to the off-detector LASP boards using optical links. The data transmission scheme will use lpGBT chips and VL+ optical assemblies. The lpGBT [92], being implemented using 65 nm TSMC CMOS technology, is a low power, higher bandwidth version of the GBT chip [93]. Using the high speed, “FEC5” mode of the lpGBT, the available user payload is 8.96 Gbps (out of 10.24 Gbps total bandwidth). The lpGBT specifications are summarized in Table 7.3 The VL+ project is expected to deliver optical assemblies in a number of versions, including a version that provides four transmitter channels which will be suitable for the FEB2-to-LASP data transmission.

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>Technology</td>
<td>TSMC 65 nm</td>
</tr>
<tr>
<td>Bandwidth</td>
<td>10.24 Gb/s</td>
</tr>
<tr>
<td>User Bandwidth (FEC5)</td>
<td>8.96 Gb/s</td>
</tr>
<tr>
<td>Links/chip (FEC5)</td>
<td>14 (E-links)</td>
</tr>
<tr>
<td>Bandwidth/link (FEC5)</td>
<td>640 Mb/s</td>
</tr>
<tr>
<td>Radiation</td>
<td>200 MRad, SEU robust</td>
</tr>
<tr>
<td>Power</td>
<td>750 mW at 10.24 Gb/s</td>
</tr>
</tbody>
</table>

The ADC data serialization rate of 640 Mbps matches the input data rate expected for the so-called ePorts provided in the lpGBT chip. Each lpGBT chip can handle up to 14 such inputs, a poor match to the eight output data streams of each ADC chip. Multiple ADC-lpGBT mappings are being considered:
• The baseline solution, assuming two 14-bit gain scales, is to map sets of three ADC chips to two lpGBT chips. In this scheme, illustrated in Figure 7.16, the “middle” ADC chip of each set of three would provide four of its output channels to each of two lpGBT chips. The fourteen lpGBT input streams would be fully assigned, connected to eight channels and BCID from one ADC, plus four channels and BCID from a second ADC. Using multiple instantiations of this three-to-two mapping as one moves in from the outer edges of the FEB2 board, 30 ADC chips could be handled by 20 lpGBT chips. Each of the final two ADC chips, near the centre of the FEB2, would need to be connected to a single lpGBT. Therefore, a total of 22 lpGBT chips are required per FEB2 board.

In this scheme, most lpGBT chips must correctly and reliably receive data from two different ADC chips, requiring some care be paid to inter-chip timing and synchronization issues. It is felt that there exists sufficient flexibility in the lpGBT specifications, which includes fully automated phase detection and alignment for the ePort inputs, to be confident that this issue can be addressed. In addition, each ADC chip would need to provide two copies of its BCID output, so that one could be routed to each of the two lpGBT chips to which it could be connected. This scheme provides a compromise between minimizing the number of lpGBT chips (and therefore optical links), while maintaining a “clean” FEB2 architecture without introducing significant synchronization and routing issues, and therefore is selected as the baseline mapping option.

• Each ADC chip could be connected to a single lpGBT chip, requiring 32 lpGBT chips per FEB2 board. This “one-to-one” mapping would be the simplest to implement on the FEB2. However, since only nine of the 14 inputs of each lpGBT chip would be utilized (eight for calorimeter data plus one for BCID), the use of the optical bandwidth is rather inefficient.

• Another option would be to map seven ADC chips to four lpGBT chips. Moving in from the outer edges of the FEB2 boards, using multiple instantiations of this seven-to-four mapping, 28 ADC chips could be handled by 16 lpGBT chips. Each of the final four ADC chips, near the centre of the FEB2, would be connected to a single lpGBT. Therefore, a total of 20 lpGBT chips would be required per FEB2 board.

This scheme results in the fewest number of optical links, namely 20 per FEB2 board compared to 22 for the baseline option. However, in this case, the lpGBT inputs would be fully utilized by the calorimeter data streams, with no inputs available for separate BCID words. Instead, some limited BCID information would have to be encoded within the 16-bit ADC words. However, given that for some cases the lpGBT inputs would include only two channels from a particular ADC chip, there is only one bit available (in addition to a Frame bit required for alignment), assuming one maintains the assignment of one Parity bit per 16-bit word. Therefore, there are concerns about the robustness of such an arrangement. In addition, this scheme adds considerable
complexity to the FEB2 design, which would incorporate some lpGBT chips connected to single ADC chips, some connected to two ADC chips, and even some connected to three different ADC chips.

![Block diagram illustrating the connections involved for mapping three custom ADC chips to two lpGBT chips.](image)

While the three-to-two mapping scheme, with 22 lpGBT chips per FEB2 board, is adopted as the baseline, more investigations are ongoing of the implications of each scheme on the optical fibre plant and on the LASP boards.

### 7.1.4 Clock and control distribution

Each FEB2 board will need to receive a 40 MHz clock, synchronized to the LHC machine clock, as well as other timing signals, such as the BCR. In addition, each FEB2 will include a large number of devices, including 32 preamp/shaper chips, 32 ADC chips, 22 lpGBT chips used for the data transmission, etc., that need to be configured and monitored. Slow control
functions, such as the monitoring of temperatures and voltages on the board, will also be required.

Dedicated lpGBT chips on each FEB2, connected to bidirectional VL+ transceiver modules, will be used to provide the clock and control distribution, as well as the slow control readback. The 2.5 Gbps downlink functionality of these lpGBT chips will be used to provide the clock, timing, and configuration data to each FEB2 board, while their uplinks will provide the readback path. Investigations are being made of the feasibility of providing redundancy by using two dedicated lpGBT chips for this purpose on each FEB2 board.

Given the large number (of order 100) of on-board devices requiring clock and control information, a significant fan-out of the information will be required, as well as a fan-in of the corresponding readback data. A number of options are being considered:

- the lpGBT ASIC includes a limited subset of slow control functionality included in the GBT-SCA (GBT Slow Control Adaptor) chip developed as part of the GBT chipset in 130 nm CMOS for the Phase-I upgrade. While the GBT-SCA (see more details below) provides a lot of flexibility, studies continue of whether the limited lpGBT functionality would allow a “tree” using only lpGBT chips to meet all FEB2 requirements.

  This solution has the advantage of using multiple copies of a single device, the lpGBT chip, to implement the entire Clock and Control distribution, and is adopted as the baseline solution. More development is needed to verify that this solution meets all of the FEB2 requirements.

- the 130 nm CMOS GBT-SCA chip was developed for Phase-I with the purpose of distributing control and monitoring signals to the on-detector front-end electronics and performing monitoring operations of detector environmental parameters. The GBT-SCA functionality includes one SPI master, 16 independent I2C masters, one JTAG master, and 32 general-purpose I/O signals with individually programmable direction and interrupt generation functionality. It also includes 31 analog inputs multiplexed to a 12-bit ADC, as well as four analog output ports controlled by four independent 8-bit DACs. Tests would need to be performed to verify the claim that the data transmission levels between the 65 nm lpGBT and the 130 nm GBT-SCA are compatible, despite their somewhat different specifications (e.g. common mode voltages).

- if neither of the options above prove suitable, a custom chip would need to be developed. (The Config chip of the current FEB was developed for just such a reason.)

An additional requirement on the 40 MHz clock is that it is distributed on the FEB2 with low jitter, both to ensure the stable and robust operation of the many 10 Gbps optical links and to achieve 14-bit performance of the ADCs. Given the LAr pulse shapes, preliminary estimates are that the RMS jitter should be at the level of 2 ps or less in order to not degrade the ADC performance. The lpGBT specifications include a statement that the RMS jitter on the clock will be less than 5 ps. Once first lpGBT prototype chips are available, tests will need to be made to evaluate the achievable analog performance.
7.1.5 Trigger summing

Analog sums are formed to provide input to a fast readout for the trigger system with coarser granularity than is provided by the main readout. As discussed in Chapter 2, in the current system, the analog signals from neighbouring cells in one layer are summed on each FEB to form $0.1 \times 0.1$ trigger towers [94] and sent to a TBB, or to a TDB in the case of the HEC and FCal. As part of the Phase-I upgrade, these sums will be replaced by sums of smaller “Super Cells” [2], and transmitted to the LTDB. Both the TBB and the LTDB perform further signal processing before the trigger signals are sent off-detector.

The TBB and TDB boards will be decommissioned in 2024 at the latest. However, the LTDB, which will provide signals for the L1 trigger system after the Phase-I upgrade, will be kept in the Phase-II upgrade, with its inputs used by the L0 trigger in the HL-LHC era. Therefore, the FEB2 board will need to provide to the LTDB the required Super Cell analog sums.

**EMB and EMEC**

For EMB and EMEC, the Phase-II L0 (and L1, if implemented) trigger will have access to the full granularity, high precision readout data. The new FEB2 boards will provide the necessary Super Cell signals. These analog signals will be prepared in the preamplifier/shaper ASIC, or extracted and summed on a dedicated mezzanine card, similar to the present Layer Sum Boards (LSB).

In the present system, noise in the trigger chain is limited by the linear mixers and LSBs, and care needs to be taken in the replacement circuits to avoid excessive noise in the Super Cell signals. In addition, the ability to remove specific channels from the sums sent to the trigger system has proven to be very valuable to control noisy channels, and this functionality should be maintained.

Saturation of signals fed into the L0 trigger can lead to misidentification of the bunch crossing to be triggered on. The preamp/shaper trigger outputs will have to have saturation behaviour which will not compromise the capability to handle this.

**HEC and FCal**

For the HEC signals, the cold preamplifier and Summing Boards (PSB) already produce the energy sums and therefore the HEC Super Cells are identical to readout cells. Super Cell energies will be sent to the L0/L1 trigger system from the LASP, along with energy sums calculated digitally. For redundancy, analog sums will be formed in the FEB2, digitized in the LTDB and processed in the LDPS, as done for the EM calorimeters.

The same scheme will be implemented for the FCal, where Super Cell energies will be provided by the LTDB-LDPS chain, and in addition energy sums will be calculated in the
LASP and sent to L0/L1 processors. The latter sums can have even finer granularity than that of Super Cells, improving the trigger quality, as discussed in Chapter 4.

7.2 Front-end cooling

7.2.1 Existing front-end cooling system

The existing under-pressure front-end cooling system is organized in six cooling loops per calorimeter face. One cooling station located on the ground-floor of UX15 maintains the flow of the water and keeps the under-pressure at the level of the front-end crates. The returning warm water is cooled through a heat-exchanger connected to the approximately 12 degree cold “mixed” water in UX15.

The distribution to each front-end board is done via custom designed cooling manifolds that are mounted close to the front-end crates and distribute the water flow in parallel to all front-end boards of a crate via flexible pipes. Each front-end board has two custom made cooling plates, one on each face. The LTDBs which will be installed during the Phase-I Upgrade will also be equipped with the same two cooling plates each. Additionally to the cooling of the boards in the front-end crates, the under-pressure system is also used to cool the DC/DC converters currently situated between the TileCal “fingers”.

7.2.2 Planned upgrades of the existing system

The new front-end boards described above will be equipped with new custom designed cooling plates (similar to legacy system). The total cooling power will approximately stay the same as for the legacy system, therefore the cooling plant and piping can be re-used. However, some improvements of the current system are being studied:

- The connectors of the cooling manifolds for the flexible pipes to the front-end boards are made of synthetic material (polypropylene) and will need to be replaced. It is being studied whether to replace these pieces with similar synthetic pieces or whether to use metallic connectors.

- The existing system has one cooling loop for two or three front-end crates (six cooling loops per calorimeter face). In case of a large leak preventing the under-pressure to be maintained large areas of the calorimeter would be concerned. It is therefore studied how this granularity could be reduced to one front-end crate. Additional remote-controlled (or accessible) valves and bypasses would need to be installed.

As described in Chapter 9, the current baseline is to move the DC/DC converters supplying power to the front-end crates further away into zones that could be accessible during short accesses without moving the calorimeters. In that case cooling will be necessary at these
new locations. A small additional dedicated cooling plant will possibly have to be installed on UX15 to serve this electronics.

### 7.3 Optical fibres

Optical fibre cables will need to be installed to dispatch the optical link signals from UX15 to USA15. Similar to what was done for the main ATLAS installation, the most convenient repartition is to route one or two cables to each front-end crate, with enough fibres (and spares) to serve all connections. Each fibre cable would serve 14 front-end boards with 26 fibres each. Thus a normal cable would need $14 \times 26 = 364$ fibres (including spares) to connect all front-end boards in that crate. The choice of the fibres themselves is guided by radiation tests which have been performed for the ATLAS ID group [116].

It is planned that these fibres will be directly routed through the holes in the UX15-USA15 wall. The fibre cables from the endcap calorimeters will need to be placed in the Sector 9 cable chain (which is the shortest) and from there traverse the holes to USA15. Preliminary studies have shown a possibility to place such fibres in the cable chain space that will be freed after the decommissioning and deinstallation of the legacy analog trigger cables. Some special effort might be needed to install these cables on inaccessible parts of the chains due to muon chambers, for example pulling the cables while moving the calorimeters and chains to their end-positions. The installation procedure is currently under study by ATLAS TC.

In order to best use the available space in the cable chain, it is crucial that the new fibre cables have the same diameter as the legacy analog trigger cables (12.5 mm). Commercial cables exist with such dimensions and up to 432 fibres for example made of 36 tubes with 12 fibres each (fibre diameter of 250 µm).

The length of these cables is well known from the original ATLAS installation and cables can be ordered complete with connectors. The ends of the cables with the connectors are protected during the placement.
8 Off-detector Electronics

Off-detector, the LAr Signal Processors (LASP) will receive the digitized waveforms, apply digital filtering to the signals of each LAr calorimeter cell, buffer the data until a trigger decision is received, and transmit the relevant data to the trigger and data acquisition (DAQ) systems. The LASP hardware implementation will be an evolution of the LAr Digital Processing System (LDPS) which will be installed during LS2 for the Super Cell readout [2]. The full data stream of detector signals digitized at 40 MHz will be available in the LASP modules. This will allow a determination of calibrated cell energies and of signal times with respect to the bunch crossing time including an active correction of out-of-time pileup. It is foreseen to process 512 cells in each LASP unit. Corresponding results of digital filter studies are summarized in Chapter 4.

Apart from the regular detector readout to DAQ, the LASP system is foreseen to provide trigger input data to the The Global Event Trigger Processors (GETP) [6] and to the LoCalo FEX system. The Global Event Trigger Processors are planned to receive energies from cells which pass a given threshold defined relative to the total noise expected in each cell. In this way the data bandwidth can be controlled while retaining sufficient information for topological clustering and for electron-hadron separation using the strip layers in EMB and EMEC as input for electron/photon, jet and energy flow measurements. Furthermore, full granularity cell energies for the FCal can overcome certain limitations of the Super Cell readout in the forward region (3.2 < |\eta| < 4.9). It is expected that forward electron identification, jet and missing transverse energy measurements implemented in the Global Event Trigger Processor or in dedicated forward jet FEX modules provide an improved performance at highest pileup conditions. The expected performance of the future trigger system using LASP data is documented in Chapter 4. Since the analog input of the pre-shapers of the HEC FEB2 modules to the LAr Trigger Digitizer Boards (LTDB) will not be fully identical to the signals available after the Phase-I upgrade using the current FEBs, the LASP system can also provide digitally formed energy sums for constructing HEC Super Cells, if required.

The LASP modules require a high input and output bandwidth and flexible programming of data handling, digital filtering and data reduction algorithms. Therefore a realization with Field Programmable Gate Arrays (FPGAs) as the main processing units is foreseen.
8.1 General requirements

Apart from the functional task of data reception and precise energy and timing measurement, the LASP system shall be compatible with the ATLAS DAQ and trigger architecture at the HL-LHC [6]. The baseline trigger architecture foresees one hardware trigger with 1 MHz L0 accept rate and 10 µs buffering interval. If required by trigger performance this design may evolve to two hardware trigger levels, L0 and L1, operating at up to 4 MHz L0 accept rate and up to 0.8 MHz L1 accept rate and L0 and L1 buffering intervals of 10 µs and 35 µs, respectively. The maximum latency for inputs to the L0Calo FEX system is 1.7 µs, and the skew between all calorimeter inputs to the FEXes is at most 16 BCs. The LASP system must be able to process 4 L0 accepts in 5 consecutive BCs, 8 L0 accepts in 5 µs and 128 L0 accepts in 30 µs. The first two rate conditions are mainly a requirement on either a derandomizing buffer of sufficient size and access speed implemented in the LASP modules, or sufficient output bandwidth in order to deal with temporary trigger rates of up to 32 MHz.

8.1.1 Interface to the LAr calorimeter front-end

The FEB2 boards will connect to the off-detector electronics via optical links driven by lpGBT [92] serializers and VL+ [91] optical converters. A concentration of the data on 22 links per FEB2 appears feasible. In total, data from 31 912 uni-directional links are to be received using the lpGBT protocol with FEC5 forward error correction [92]. Each link provides 224 user bits per 256 bit frame transmitted at 40 MHz, i.e. a user bandwidth of 8.96 Gbps out of 10.24 Gbps total. The LASP must therefore implement the lpGBT protocol for decoding and adapt to the ADC-to-link mapping discussed above in Chapter 7.

Moreover, two fibre pairs per FEB2 are foreseen for clock distribution, control and monitoring (TTC), in total $4 \times 1542 = 6168$ fibres. In the baseline layout, the fibres shall be connected to those LASP boards which provide the FEB2 readout, i.e. 22 + 4 = 26 fibres per FEB2 are connected. Fibre groups shall be arranged in multiples of 12 or 24 to match the commercially available fibre connector types. In the baseline design, 4 FEB2 are read out by one LASP unit, i.e. 96 input and 8 output fibres are needed in total. Since the full LASP firmware is not yet designed and since the FPGA resource usage is only based on estimates, the implementation of the full TTC interface in the same FPGA as the LASP unit might turn out to be too complex in firmware design and layout. There are two options considered which can mitigate this design risk. The TTC interface can be implemented in a separate “Main FPGA” on the LASP main board, so that functionalities are well separated, or a set of dedicated LASP boards will handle the TTC signal distribution and monitoring task. In case of the latter option, regular LASP boards can be used since these can provide a large number of links to the front-end (up to 104, depending on the hardware solution, see Section 8.3). However, more LASP modules will be needed and more space in the ATLAS counting room, USA15. Detailed design studies are thus necessary to select between the baseline TTC distribution via each LASP board, and the alternatives.
8.1.2 Dataflow to the Trigger and DAQ system

The different tasks of the LASP define the dataflow and data buffering until the different trigger accept signals arrive. Figure 8.1 gives an overview of the functional blocks and data streams. The raw data are decoded and a configurable remapping allows a grouping of channels that shall be processed in groups for energy summing and data reduction. The data streams to the Global Event Trigger Processor and to the L0Calo FEX modules are running at 40 MHz, while the output to the DAQ is controlled by the trigger accept signals. Raw and processed data are furthermore buffered in memory for building DAQ data fragments.

Interface to the DAQ

The interface of the LASPs to the DAQ system is provided by the FELIX network interface modules [5] which are planned to receive and send data with a lpGBT compatible link speed. The data fragments to be sent to the DAQ on a trigger accept signal are composed of several blocks. For triggered events, the result of the precision energy calculation, of the signal time and of a signal quality parameter, e.g. a $\chi^2$ comparison to the ideal waveform, shall be transmitted, together with the raw data. The total data size per event will be similar to today’s readout:

- 16 bits for energy from the high-gain signal in all cells, plus 2 bits for error or signal quality flag;
- $2 \times 32$ bits for energy, $2 \times 16$ bits for time, $2 \times 16$ bits for the signal quality parameter, for both gains in case the measured absolute energy value in a cell is above $3 \sigma$ total noise, which corresponds to an average readout fraction of 0.55%;
• up to 24 samples of $2 \times 14$ bit of raw ADC data from both gains, again if a $3\sigma$ total noise threshold is passed.

In total, 18 bits will be sent for each event, while for high-energy cells 784 bits are needed. This results in an average of 24 bits to be read out for each detector cell, which sums to 12.3 kbit per event for 512 cells. Moreover, the data sent to the trigger streams also need to be stored for all triggered events for later cross-checks and monitoring of the trigger system. Since the Global Event Trigger Processor input depends on a $2\sigma$-above-noise energy threshold, the average size of the trigger readout fragment for 512 cells amounts to about 2 kbit per event, and increases to about 7 kbit per event in case the HEC/EMEC or FCal FEX input data are added.

In the evolution of the TDAQ system, there are two possibilities for sending the readout data to FELIX. If data are transmitted always on the latest trigger accept signal, i.e. at L0 accept at 1 MHz and at L1 accept at 0.8 MHz in the second development phase, the data fragments need to be buffered for up to 35 $\mu$s in the LASP units. If the readout is activated always on L0 accept, i.e. at 1 MHz and at 4 MHz, the buffer size can be smaller, but four times more output links are needed and four times more FELIX modules are required on the receiving side. The first solution is therefore preferred since it will require less additional hardware and buffering of the readout data on the LASP unit only needs a modest additional amount of memory, as specified in more detail below.

**Interfaces to the trigger system**

The LASP modules will provide calorimeter information from individual LAr calorimeter cells to the Global Event Trigger Processor at 40 MHz, which will complement the L0Calo trigger which is based on Super Cell measurements. An important requirement of the digital signal reconstruction is the correct bunch crossing assignment of the energy measurements sent to the trigger system. One calibrated energy value packed in a 10 bit word is foreseen for each calorimeter cell which passes a $2\sigma$ threshold above total noise. On average, this corresponds to a fraction of cells of $5.5\%$, which has been verified using minimum bias events at $\mu = 200$ and is slightly larger than expected from a Gaussian distribution. However, for certain event topologies, e.g. high-energy jets or local noise bursts in the LAr endcap calorimeters, the fraction of high-energy cells can exceed this average value. Examples of expected LASP occupancy for events with high-energy jets or high-$p_T$ electrons are shown in Figure 8.2 and compared to the occupancy for minimum bias events. In order to have some contingency, a readout fraction of $30\%$ corresponding to 153 out of 512 cells is assumed for bandwidth estimates. Moreover, two solutions are proposed in case also this fraction is exceeded: the LASP may send all cells ordered by energy until the output bandwidth saturates, or large event fragments may be sent in asynchronous mode to the Global Event Trigger Processor, where an input buffer rebuilds the complete event. The latter solution will cope with high-occupancy, low-rate events, while it will not prevent bandwidth saturation during noise bursts. Noise burst events appear mainly in the endcap calorimeters and may...
drive all cells in the affected region above the $2\sigma$ noise threshold. Active noise burst flagging is performed regularly during ATLAS data taking [117], however it relies on the detection of irregular signal pulses either in larger detector areas than available in a single LASP or during long data sequences at µs scale. Local noise burst flagging thus requires more dedicated studies, as well as the additional latency needed for cell energy ordering.

Figure 8.2: Channel occupancy per LASP unit for minimum bias events, high-energy dijet events, and high-mass $Z' \rightarrow tt$ events at $\mu = 200$. (a) LASP occupancy in the EMEC region $1.6 < |\eta| < 2.4$. (b) Occupancy of a LASP unit covering $1.0 < |\eta| < 1.4$ of the EMB front layer and $|\eta| < 1.4$ of the EMB back layer.

If only cell energies above threshold are sent to the Global Event Trigger Processor a bit pattern needs to be provided which reflects the cell hit pattern. The bit pattern size is 512 bits for 512 cells per LASP. For the given target occupancy of 30% this method uses less bandwidth than providing each energy value with a 9-bit address. With a data fragment size of $10 \text{ bit} \times 512 \times 30\% = 1536 \text{ bit}$, adding the bit pattern and assuming a 25% encoding overhead, the bandwidth of each LASP unit to the Global Event Trigger Processor amounts to 102.4 Gbps. The data encoding may include forward error correction, like for the front-end links.

The format of the trigger information for the L0Calo global FEX (gFEX) modules that is sent for the HEC shall be unchanged with respect to the implementation of the Phase-I upgrade. In order to minimize changes to the other existing FEX modules, the total number of HEC fibres from the LASPs to the FEX system will remain the same although the distribution of data on these may change. In total, 640 fibres are needed for the HEC data stream to the FEX system. The HEC Super Cell energies will be calculated from sums of individually calibrated cell energies in the LASP units, while the Phase-I Super Cell readout is based on analog summing.

The FCal trigger input to the Global Event Trigger Processor or to dedicated forward FEX modules will contain energy values packed in 10-bit words from all FCal cells. Like for the
Global Event input, a correct bunch crossing assignment is fundamental for all energy values sent to the FEX systems. With 512 cells per LASP unit and a 25% encoding overhead, the additional output bandwidth for the FCal data is 256 Gbps per unit.

The link speeds with which the LASP modules will connect to the TDAQ system are foreseen to be:

- FELIX interface: 10.24 Gbps with 8.96 Gbps payload, i.e. lpGBT compatible link speed
- FEX interface: 11.2 Gbps
- Global Event Trigger Processor interface: 25.78 Gbps

**8.1.3 Data buffering**

The dataflow and data buffering scheme is shown in Figure 8.1. Buffering on the LASP is necessary since the data transmission to the DAQ is triggered by L0 and L1 accept signals. Assuming that a LASP module will handle 512 cells, the raw ADC data per event from both gains is $512 \times 2 \times 16 \text{ bit} = 16384 \text{ bit}$ which results in an input data rate of 655.4 Gbps per LASP. These data are kept in memory for the full 35 µs buffering time which simplifies the selection of the raw data samples on L0/L1 accept. The memory required for raw data buffering is 22.9 Mbit per LASP. An early rejection of raw data samples does not reduce the memory needs because up to 24 samples of each signal pulse shall be buffered for readout while the trigger system accepts every 10th to 40th event.

Furthermore, the calculated energies, signal time and signal quality parameters as well as the trigger input energies of the selected cells need to be kept in memory until a trigger accept. The maximum fragment size containing these reconstructed quantities for 512 cells is 19.5 kbit per event. For the quantities calculated in the processing units, the requirements on total memory size can be reduced if these data are first stored for 10 µs until L0 accept, an optional fast-clear signal or time-out. The time-out can also be launched for all events which belong to earlier BC times than the triggered event, since the trigger accept signals are expected to arrive ordered in time, respectively ordered by event number. The fragments selected by L0 can then be transferred to a second buffer for at most 35 µs until L1 accept or fast-clear signal or time-out. The memory needs for the two buffering stages are 7.8 Mbit and 2.7 Mbit, respectively, per LASP 512-cell unit.

**8.1.4 System requirements**

The LASP system, including TTC distribution system, will be installed in the ATLAS counting room USA15. It will replace the LAr ROD system, which is currently occupying 8 LHC racks.
The Phase-II LAr off-detector electronics is required to fit into a similar rack space as the current LAr ROD system. An extension of the LHC racks in height and cooling power per rack is under investigation, so that the floor space is reduced.

One general constraint is the available cooling power in USA15. For the future LASP system a maximum power consumption of 177 kW is allocated.

### 8.2 Data processing

The core functionality of the LASP will be the energy reconstruction and time measurement of the LAr signal pulses. Digital filtering algorithms will be used to reduce the effects of electronics noise and pileup noise.

The optimal filter \cite{16}, which is currently used in the LAr calorimeter readout, shows the best performance for electronics noise suppression and corrects in-time and out-of-time pileup on average. However, in case of bipolar shaping, the gaps in the LHC bunch structure \cite{118} lead to a pedestal shift and therefore an amplitude mismeasurement. This can be corrected by applying energy corrections which depend on the bunch position in the LHC orbit, as is done in the L1Calo trigger and foreseen for the Super Cell readout. The corrections can be determined and updated regularly during data taking in order to take luminosity variations into account. Information from the 3 564 orbit positions must be stored in the FPGA memory for each readout channel. The corrections are then applied in real time. The typical OF implementation is using two 5-tap FIR filters for energy and time measurement, as well as a $\chi^2$-like signal quality parameter based on 5 samples. The usage of an OF with more taps does not significantly improve the energy resolution and precision \cite{17, 37}.

As mentioned in Chapter 4, digital filters with active out-of-time pileup correction such as Wiener filter and extended optimal filter (EOF) are under development. Such filters have stronger hardware requirements than the optimal filter. Typical implementations of Wiener filters with active correction combine different FIR filters with up to 16 taps in total \cite{119}, while EOF implementation show good performance with 24-tap FIR filters for energy determination. Detailed results on the resource usage for an EOF implementation are provided in Table 8.1.

Although the active out-of-time pileup correction should ideally compensate the pedestal shift at the beginning of LHC bunch trains, a small remaining shift is still observed \cite{37, 39} in the implementations available today. Therefore, a pedestal correction, as for the OF, may still be necessary to obtain an unbiased energy reconstruction (see Figure 8.3).

The trigger requires that the energy measurement in each cell is assigned to the correct bunch crossing. Since analog signal saturation will be avoided in the upgraded readout system the main cause of incorrect bunch crossing assignment is expected to be out-of-time signal pileup. Various identification algorithms are under investigation. If an OF based algorithm is applied for energy reconstruction the bunch crossing of interest can be identified either
Table 8.1: Resource usage of an EOF implementation for energy and signal time calculation for 512 channels in an ALTERA Arria-10 FPGA assuming 6-fold time multiplexing. The number of Adaptive Logic Modules (ALM), registers and DSP blocks, as well as the memory size are given. One ALTERA DSP block contains two multiplier-adder units, which are used in the filter implementations. If two gains are read out per calorimeter cells like in the baseline design, the given filter resource estimates need to be multiplied by two.

<table>
<thead>
<tr>
<th></th>
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<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Energy</td>
<td>Time</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>4 tap</td>
<td>4 tap</td>
<td>68K</td>
<td>159K</td>
<td>7</td>
</tr>
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<td>16 tap</td>
<td>8 tap</td>
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<td>8 tap</td>
<td>171K</td>
<td>205K</td>
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<td>32 tap</td>
<td>8 tap</td>
<td>199K</td>
<td>387K</td>
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</tr>
</tbody>
</table>

Figure 8.3: Missing transverse energy determined from LAr calorimeter cell energies calculated with the Optimal Filter and the Extended Optimal Filter. The EOF is able to reduce the effect of pedestal shift at the beginning of a LHC bunch train. This shift is due to missing contributions from the negative lobe of preceding waveforms for the first signal pulses in a bunch train. The bipolar shaping thus leads to an overcompensation of out-of-time pileup contribution and strong positive shift of reconstructed energies.
by an energy maximum within the data stream or by using the reconstructed signal time. However, a maximum search prevents an identification of energy deposits in consecutive bunch crossings. Methods with active pileup correction, like the EOF or a Wiener filter with forward signal correction [37], allow energy measurements in each bunch crossing but show a different performance in noise suppression and energy resolution (see Section 4.1). Quantitative studies of the efficiency of correct bunch crossing assignment and its impact on the energy reconstruction are foreseen in order to select between the different algorithms.

The baseline of the front-end electronics targets a 2-gain 14-bit ADC readout with both gains being sent to the LASP system in order to avoid gain selection in the front-end and allow filtering based on samples from both gains. The selection between the two gain scales can be performed off-detector in the LASP, ideally choosing the highest scale which does not saturate. The selection algorithm is not yet defined and needs to be studied. In the current FEB, thresholds are applied to the peak ADC value in medium gain for the triggered signal pulse. In a free-running 2-gain mode, the full energy and timing reconstruction filter will be run continuously for both gains separately. The low-gain energy result, assuming it will never saturate, can be used to select the optimal gain. The optimal selection depends on the applied calibration scheme because gain transitions between energy ranges interesting for physics need to be avoided. The implementation in FPGA firmware provides flexibility to always adapt the gain selection to the calibration needs. Alternative signal filtering using mixed sample sequences from both gains is under investigation, but a consistent calibration scheme is more challenging in this case.

The reconstructed energy and time in each calorimeter cell from the continuous digital data stream represents the input to the trigger system. Energy values above $2\sigma$ total noise are planned to be sent to the Global Event Trigger Processor, while Super Cell energy sums for the HEC and all FCal cell energies can be sent to the L0Calo FEX modules. Depending on the filter algorithm, the time information will serve to assign the correct BC to the energy measurement and can be used to identify pulses with excessive noise contributions.

The LASP modules will store the raw data until the trigger decisions arrive. Additional digital filters can thus be applied to the sampled waveforms for triggered events. In particular, signal quality criteria in comparison with ideal pulse shapes can be performed once more, with the hypothesis that the correct bunch-crossing is identified.

The LASP data processing is foreseen to include monitoring functions and error detection mechanisms. Since the LASP will see the full LAr calorimeter data stream, noise monitoring and data integrity checks are planned to be implemented. Function errors of the front-end and optical transmission will be flagged in order to allow an automatic error handling, e.g. disabling of readout channels. Histograms and counters read out by slow-control data links are foreseen to provide information of the live status of the readout system.

The implementation of the data processing requires hardware resources for algorithms and storage of filter constants and of pedestal correction parameters. Based on performance studies the following resource baseline has been developed:
• 24+12 multiplexed multiplier-adder units per detector cell and gain for energy and time measurement with active out-of-time pileup suppression using the full input data stream at 40 MHz;

• $3 \times 10$ multiplexed multiplier-adder units per detector cell and gain for noise-optimized energy, time and signal quality parameter calculation for triggered events at up to 4 MHz;

• $36 \times 3564$ bit per detector cell and gain for pedestal correction at each position of the LHC orbit;

• storage area for filter constants with one value per filter element.

### 8.3 Hardware realization and components

#### 8.3.1 Summary of hardware requirements

The segmentation of the LAr calorimeter readout is mainly given by the number of channels processed by one FEB2, which is up to 128 cells with 2 gains, i.e. 256 channels. One LASP unit will receive data from 2 to 4 FEB2 boards. A possible mapping of FEB2 boards to LASP units is given in Appendix A. The overall readout configuration assuming 22 data fibres per FEB2 board and four FEB2 boards connected to each LASP FPGA is shown in Table 8.2. The link speed to the Global Event Trigger Processor is assumed to be 25.78 Gbps and a 25% data encoding overhead. If, for reasons of power dissipation, an FPGA model needs to be chosen which will not provide such high-speed links, the rate may be reduced down to about 15 Gbps, at the cost of about 75% more output links on average to the Global Event Trigger Processor. The HEC/EMEC output to the L0Calo FEX system (eFEX, jFEX, gFEX) assumes the legacy link protocol and speed as implemented during the Phase-I upgrade, while the FCal output to the L0Calo FEX system is taking the full readout of the FCal cells into account, as it may be used by dedicated forward FEX processors. All serial links are driven by transceivers of the FPGA. The TTC and Ethernet input may also be provided by other I/O connections, like LVDS signals or dedicated PHY chips, respectively, depending on the available FPGA resources.

Modern FPGAs can operate the input and output links of the duplex transceivers at independent speed. The required number of transceivers of the LASP FPGAs is therefore determined by the number of input links, which always exceeds the number of output links, even for HEC and FCal regions where additional data are transferred to the L0Calo or Global Event trigger systems.

Signal processing in FPGAs can be implemented by exploiting time-multiplexing, i.e. the FPGA clock frequency will be a multiple of 40 MHz. Implementations of the extended optimal filter algorithms in FPGA test hardware (ALTERA Arria-10) reach 240 MHz in a
Table 8.2: Readout configuration for 22 data fibres per FEB2 board and nominally four FEB2 boards connected to each LASP FPGA, assuming fast 25.78 Gbps links to the Global Event Trigger Processor and legacy FEX links to LoCalo. The number of LASP units is summed for both detector sides.

<table>
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<th>LASP ID</th>
<th>No. of Cells per LASP</th>
<th>No. of LASPs</th>
<th>Links per LASP</th>
<th>Input</th>
<th>Output</th>
<th>Bidirectional</th>
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<td>810</td>
<td>3048</td>
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</table>

realistic environment, i.e including transceiver I/O, channel remapping and energy summing at the output stage. With the filter configuration discussed above, the number of multiplier-adder units per cell for two gains needs to be: $2 \times ((24 + 12) \times 40 \text{ MHz}/240 \text{ MHz} + (3 \times 10) \times 4 \text{ MHz}/240 \text{ MHz}) = 13$.

In summary, the LASP FPGA units need to provide:

- 22 input links per FEB2;
- 2 pairs of TTC links per FEB2;
- 1 bidirectional link per FEB2 for FELIX data readout and TTC data exchange at 10.24 Gbps;
- 1 fast output link at 25.78 Gbps per FEB2 to the Global Event Trigger Processor system or, alternatively, 2 links at a speed below 17 Gbps per FEB2;
• up to 6 output links for HEC and FCal FEX data transmission at 11.2 Gbps per FEB2; since the forward FEX configuration is not yet fully defined further links to the forward FEX modules may be needed to cover a larger area of the endcap calorimeters for forward jet reconstruction;

• 1 full-duplex 10 Gbps Ethernet connection for monitoring and control;

• 13 multiplier-adder units per calorimeter cell;

• 0.295 Mbit of memory per calorimeter cell, including buffer space for raw data, calculated quantities, filter constants and pedestal correction.

In the baseline configuration with 4 FEB2 and 512 calorimeter cells connected to 1 LASP unit, this corresponds to 88 data input links, up to 10 TTC FEB2 link pairs, 2 to 3 bidirectional readout and TTC links, 12 to 23 FEX output links and 1 Ethernet full-duplex link, together with 6656 multiplier-adder units and 151 Mbit of memory.

8.3.2 General layout of the LASP hardware

The main building blocks of the LASP system will be the FPGA processing units which will be mounted on a PCB and connected via high-speed links to electro-optical converters. Optical pig-tails lead to the front-panel optical connectors, to which both input and output links will be connected. Since the industrial trend is going for higher link speed rather than for higher fibre counts per connector, a 12-fibre converter can be assumed. In the configuration with 4 FEB2 per LASP FPGA the number of necessary 12-fibre transceiver modules ranges from 10 to 14, depending on the amount of output data that needs to be transmitted, on the implementation of the TTC clock distribution directly in the LASP and on the available maximum link speed of the FPGA for data transmission to the Global Event Trigger Processors. The link speed at the input does not appear as a limiting factor for concentrating the information of several FEB2 boards into one FPGA unit because the required number of DSP units for multiplier-adder operations, the logic and the necessary memory impose a stronger constraint on the FPGA choices, at least if today’s FPGA models are considered. Also the flexibility of the Global Event Trigger Processor interface leaves some freedom in the choice of FPGA models concerning the availability of very high-speed links (over 25 Gbps).

8.3.3 LASP form factor

The main characteristics of the LASP defining the form factor are the size and pin-count of the FPGA (typically 4 cm × 4 cm to 5 cm × 5 cm and more than 2 000 BGA pins), the number of FPGAs (372 to 744), the number of fibres connected to each FPGA (up to 140), and the power dissipation. The PCB and board design will require a high density, high-speed, complex signal mapping with long signal tracks and high power consumption. The processor will
have to operate with virtually no problem for a long time, typically 15 years, given the fact that the dead-time induced by a failure may have significant negative consequences on the data taking. Therefore, Quality Assurance (QA) considerations have to be taken into account very seriously at an early stage of the design, and should dominate in the choice of the form factor.

The baseline design for the LASP modules is based on the Advanced Telecommunications Computing Architecture (ATCA) form factor. A functional layout of the LASP ATCA blade is sketched in Figure 8.4. The 2 LASP units are each equipped with a high-performance FPGA and include electro-optical receiver and transceiver arrays operating at different link speeds as well as additional memory and clock distribution devices. The optical links are routed to Multifibre Push-on (MPO) connectors on the front panel. The main section of the blade contains a Main FPGA for TTC signal distribution in case it can not be directly implemented in the Processing FPGAs and for preparing Super Cell data from HEC and FCAL for the trigger system. The TTC fibres connect to the FEB2 on the LASP front face, like the data input links, while the Super Cell data are sent via the Rear Transition Module (RTM) to the LOCALO FEX systems. The Main FPGA is also foreseen to prepare monitoring data. An Ethernet switch provides a fast Ethernet connection (10G or 40G) from the ATCA base plane to the FPGAs for configuration and control. ATCA blade control is implemented by an Intelligent Platform Management Control chip (IPMC).

The LASP board is planned to be realized as a full-size ATCA blade or, alternatively, with 2 Advanced Mezzanine Cards (AMC) for the processing units and an ATCA carrier blade for the main section. Full-size ATCA boards allow a PCB thickness of 2.4 mm with 24 layers for signal routing and power distribution, while for an AMC based design through-hole plug connectors can be implemented to increase the PCB thickness beyond the standard 1.6 mm. Double-width AMC modules with dedicated DC/DC converters and additional Mezzanine Module Control (MMC) chips will be required. Although a monolithic board design is less modular than the concept with one main board equipped with 2 FPGA mezzanine cards, it provides more freedom in placement of processing FPGAs, optical transceivers, power modules and other components on the board. A detailed comparison of the monolithic and modular blade designs will be performed, including the aspect of enabling a collaborative design effort.

As will be discussed in more detail below, the constraints due to high power dissipation also influence the integration density of processing units per board. If two FPGAs from the lower range of the high-performance devices (with order of 5 000 DSPs) will be used the power per ATCA board is expected to stay below the 400 W limit per ATCA shelf slot which is given by the PICMC 3.0 specification. However, for very high-performance devices chosen for the baseline design (with order of 10 000 DSPs) the ATCA shelf must allow up to 800 W per slot, as foreseen in the recent PICMC 3.7 standard. Equipping a full-size ATCA board with 2 (or more) FPGAs increases the potential costs in case of board failure, both during production and operation. However, the design flexibility due to larger board area is expected to compensate such risks. Furthermore, there are companies that specialize
in the replacement of high BGA-pin-count FPGAs which have reached a sufficiently high replacement efficiency such that the repair of full-size ATCA cards, and also of AMC and carrier cards, appears feasible.

Figure 8.4: Layout overview of a LASP module in full-size ATCA format with sufficient space for FPGA and optical transceiver placement. The two processing units can be either implemented as mezzanine cards or simply define areas on the main board. In the monolithic board design the DC/DC converters and Modular Management Controller (MMC) interfaces on the processing units can be omitted. For the optical transceivers the number of links, the link speed in Gbps and the direction (Tx/Rx) is indicated. The Rear Transition Module (RTM) provides the optical links to the L0Calo FEX modules.

Alternatively, the FPGA processing units may also be placed on PCIe cards. These allow a placement of large 5 cm × 5 cm FPGAs, similar to the double-width AMC cards. The board area is also expected to be sufficient for optical transceivers and routing of fibres to external connectors, as shown in other LHC applications [95]. The PCB thickness can be enhanced by thinning the PCB at the edges for compatibility with PCIe connector thickness. Detailed comparison of the ATCA and PCIe options based on technical feasibility of PCB design, power and cooling will need to be done.
8.3.4 Electro-optical transceivers, pigtails and connectors

The transceiver signals of the FPGA are routed to electro-optical converters on board. Optical fibre pig-tails will connect the converters to fibre connectors at the LASP front panel. The optical transceivers used in Phase-I applications (LATOME [120], FEX [121, 122]) are not ideal concerning mechanical fibre connections and heat dissipation. Recently available optical modules, like SAMTEC Firefly [123], show improved performance concerning these parameters and also integrate 12 fibres in one device for link speeds up to 16 Gbps. Although high-speed (higher than 25 Gbps) optical modules are only available in 4-fibre versions today, it is expected that also 12-fibre modules will be accessible at the time of LASP construction if needed. Front-panel multi-push-on optical (MPO/MTP) connectors with 48 fibre connections require a width of about 30 mm [120] so that enough space is available if two FPGAs are mounted on one full-size ATCA board. The relative placement of converters and connectors is important in order to avoid mechanical stress on the pig-tail fibres. Mechanical guiding elements shall ensure environmental protection of the fibres.

8.3.5 FPGA candidates

FPGA devices for signal processing are part of a rapidly developing field in industry targeting higher processing capabilities per chip, higher number of I/O connections, more memory and lower power. Devices which will be implemented in the final, optimized design of the LASP modules may thus not even be available today. However, some FPGA models already fulfil the requirements of a LASP unit. Table 8.3 shows a survey of modern high-end FPGAs with their available resources in comparison to the LASP requirements. Most of the models provide a resource margin which allows flexibility in the firmware design and the possibility to add further functionality at a later stage of the system design and even during operation. All of these devices have 2,000 to 2,500 BGA pins and require up to 5 cm × 5 cm of board area. Depending on the number of available transceivers, DSP blocks and memory, each LASP FPGA can process the input of 2, 3, or 4 FEB2 boards. The advantage of processing a smaller number of FEB2 boards is the reduced power consumption per FPGA which scales with number of channels processed. However, a higher integration factor reduces the total number of FPGAs and allows the implementation of algorithms based on cell information from a larger detector area. In particular, the preparation of Super Cell energy sums for the HEC can then be performed directly in the processing FPGA. In the baseline layout, one LASP FPGA therefore connects to 4 FEB2 boards.

It is interesting to note that a higher link speed at the input, i.e. data rates beyond the 10.24 Gbps of the lpGBT, would not allow a further increase of channel number per FPGA because the corresponding number of DSPs and amount of logic and memory would reach the resource limit of the FPGA. Moreover, the speed grade of the FPGA device is a potential cost saving factor. Devices with large DSP, logic and memory resources may be available with slower transceiver versions (e.g. all below 25 Gbps), but would require a significant
Table 8.3: Examples of FPGA devices which match the LASP resource requirements and even provide some margin with respect to the current estimates. In ALTERA devices one DSP block provides two multiplier-adder units (DSP units). In the baseline layout, one FPGA shall process the input of four FEB2 boards.

<table>
<thead>
<tr>
<th>Device</th>
<th>Xilinx</th>
<th>ALTERA</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Kintex</td>
<td>Virtex Stratix 10</td>
</tr>
<tr>
<td></td>
<td>Ultrascale</td>
<td>Ultrascale+ GX 1650 GX 2500 GX 2800</td>
</tr>
<tr>
<td></td>
<td>KU115</td>
<td>VU9P VU11P</td>
</tr>
<tr>
<td>Duplex</td>
<td>&lt; 25 Gbps</td>
<td>64 0 0 32 32 32</td>
</tr>
<tr>
<td>Transceivers</td>
<td>&gt; 25 Gbps</td>
<td>0 104 96 64 64 64</td>
</tr>
<tr>
<td>DSP blocks</td>
<td>5520</td>
<td>6840 9 216 3 145 5 760</td>
</tr>
<tr>
<td>Memory [Mbit]</td>
<td>76</td>
<td>345 340 114 195 229</td>
</tr>
<tr>
<td>Logic units [K]</td>
<td>1450</td>
<td>2586 2835 1624 2005 2422</td>
</tr>
<tr>
<td>FEB2 per FPGA</td>
<td>2</td>
<td>4 4 3 4 4</td>
</tr>
<tr>
<td>Total no. of FGPs</td>
<td>744</td>
<td>372 372 496 372 372</td>
</tr>
<tr>
<td>Resource usage</td>
<td></td>
<td>Links 69% 85% 92% 69% 92% 92%</td>
</tr>
<tr>
<td></td>
<td>DSPs 60% 97% 72% 79% 66% 58%</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Memory 99% 44% 44% 99% 77% 66%</td>
<td></td>
</tr>
</tbody>
</table>

increase in number of output links to the Global Event Trigger Processor assuming e.g. only 15 Gbps per link. All other I/O links are anyway operated at lower speeds of 10 to 13 Gbps. The final choice of the FPGA model will be based on prototype tests and realistic firmware implementations of the full LASP functionality.

8.4 Experience with the Phase-I Digital Processing System

Several functional blocks required in the LASP are already needed in the Phase-I LDPS system. A series of full LDPS system tests using LATOME prototype boards connected to data sources and L1Calo FEX modules have been performed. The following components are already implemented in firmware and successfully tested in hardware: GBT link decoding, configurable channel remapping, a framework for digital filter algorithms, output summing, interfaces to DDR3 RAM, FEX interfaces and Ethernet connection. The data buffering and DAQ interface to FELIX are in an advanced development stage. FPGA control functionality is implemented based on the IPbus [124] protocol. For firmware development, a full software and simulation based test bench has been created with all external interfaces. Firmware and
system testing is being performed with commercial test cards, prototype LATOME and LAr Carrier (LArC) [125] boards.

The LDPS is designed to fulfil the strict latency requirements of the current L1 trigger. Adding data reduction algorithms, like summing or application of thresholds usually can be realized in a few FPGA clock-cycles, so that also the LASP is expected to meet the future L0 latency constraints. The LDPS firmware and hardware can thus be considered as a full prototyping system for the LASP development.

The LATOME board, shown in a prototype version in Figure 8.5, has an architecture similar to the proposed LASP module. An Arria-10 FPGA with 66 full duplex transceivers is connected to eight 12-fibre µPod electro-optical converters so that 48 input and 48 output links are realized.

Figure 8.5: Picture of a prototype of a Phase-I LATOME processing board in Advance Mezzanine Card format, with a central FPGA, eight 12-fibre µPod connections and infrastructure components, like powering, clock and control interface. The LATOME board itself does not fulfil the resource requirements of the LASP unit, but will serve as a Phase-II development and firmware prototyping platform.

A pre-prototype of the LDPS, the ABBA board [126], is being operated in a demonstrator system of the Phase-I Super Cell readout. Although it does not directly use firmware blocks of the LATOME, it will be useful to validate firmware and algorithms for continuous real-time processing and active pileup correction since Super Cell pulse shapes are similar to those of individual LAr calorimeter cells.

The resources used in the LATOME FPGA have been measured for digital processing of 320 channels during a dedicated hardware and firmware test. The test configuration was based on an ALTERA Arria-10 FPGA and included 48 input (Rx) and 48 output (Tx) links, a channel remapping module, an energy summing module at the output stage, and a digital filter module running at 240 MHz (i.e. 6-fold multiplexing) with one 5-tap Optimal Filter per channel. It does not include yet a buffering module for raw signals and calculated energy values, which is expected to additionally occupy 20% of the total memory. Table 8.4 summarizes the results. The main output data stream of the LATOME is the FEX trigger.
Table 8.4: FPGA resources used in the LATOME Arria-10 FPGA during a hardware and firmware test for processing 320 input channels. One ALTERA DSP block provides two $18 \times 18$ multiplication-adder units used in the digital filter module. The logic is given in units of “Adaptive Logic Modules” (ALMs). The Phase Lock Loop (PLL) units are used in clock signal distribution.

<table>
<thead>
<tr>
<th>Resource</th>
<th>Used</th>
<th>Available</th>
<th>Fraction</th>
</tr>
</thead>
<tbody>
<tr>
<td>Rx transceivers</td>
<td>49</td>
<td>66</td>
<td>74%</td>
</tr>
<tr>
<td>Tx transceivers</td>
<td>49</td>
<td>66</td>
<td>74%</td>
</tr>
<tr>
<td>DSP blocks</td>
<td>248</td>
<td>1518</td>
<td>16%</td>
</tr>
<tr>
<td>Logic (ALMs)</td>
<td>163K</td>
<td>427K</td>
<td>38%</td>
</tr>
<tr>
<td>Registers</td>
<td>277K</td>
<td>1708K</td>
<td>16%</td>
</tr>
<tr>
<td>Memory</td>
<td>25.7 Mbit</td>
<td>55.6 Mbit</td>
<td>46%</td>
</tr>
<tr>
<td>I/O pins</td>
<td>262</td>
<td>650</td>
<td>40%</td>
</tr>
<tr>
<td>PLL</td>
<td>73</td>
<td>138</td>
<td>53%</td>
</tr>
</tbody>
</table>

data. The data sent to DAQ are mainly for validating the correct functioning of the trigger system with the input provided by the LDPS. The LATOME memory and output bandwidth for the DAQ readout task may require a data reduction scheme in order to cope with the higher trigger rates and longer latencies in the HL-LHC phase. The LASP unit is therefore expected to require more digital processing resources per channel ($\times 11$) together with more logic units, as well as more memory for buffering and pedestal correction. The total number of I/O links per processing unit is comparable, although the LASP will have a ratio of input to output data bandwidth between 2.5 (for HEC and FCal) and 11 (for EMB and EMEC), while for the LATOME input and output bandwidth are about equal.

8.5 Latency

The L0Calo and Global Event trigger systems expect input from the LAr calorimeters after 1.7 $\mu$s, at most. With the proposed readout structure and components this requirement can be met without loss of functionality. Table 8.5 summarizes the different latency contributions of the Phase-II readout system until a digitized signal is received by either the L0Calo FEX modules or the Global Event Trigger Processors. The largest single contribution to the total latency is due to the optical cable between the FEB2 and LASP boards for which a direct path of up to approximately 75 m is foreseen (see Section 7.3). The latency estimate for energy calculation includes the bunch crossing assignment. The total latency sums to 1.270 ns, corresponding to 50.8 LHC bunch-crossings, if the data are sent directly by the LASP units. However, the FEX trigger data of pairs of LASP FPGAs covering the HEC/EMEC detector may need to be concentrated into one output stream by the corresponding Main FPGAs in order to be backward-compatible with the Phase-I Super Cell readout. In that
case, additional time for one serialization-deserialization step and for building of new data fragments will be needed, which increases the total latency to 1 470 ns (58.8 BC), still within the requirement of the trigger system [6]. The Phase-I Super Cell readout will continue to provide input to the FEX modules within 1 105 ns (44.2 BC).

Table 8.5: Estimated latency contributions along the signal path of the LAr calorimeter readout. The values are based on simulations and measurements with prototype ASICs and devices of the FEB2 and LASP systems, as well as on final prototypes of the Phase-I Super Cell readout which implements similar functionalities. For parts of the FEX data, a data transmission between LASP FPGAs and Main FPGA is necessary and the total latency is increased by the time for serialization-deserialization and fragment building.

<table>
<thead>
<tr>
<th>Contribution</th>
<th>Latency [ns]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Time of flight at $</td>
<td>\eta</td>
</tr>
<tr>
<td>Cable to preamp</td>
<td>30</td>
</tr>
<tr>
<td>Preamp and shaper</td>
<td>10</td>
</tr>
<tr>
<td>Digitization</td>
<td>125</td>
</tr>
<tr>
<td>Multiplexing</td>
<td>50</td>
</tr>
<tr>
<td>Serializer</td>
<td>25</td>
</tr>
<tr>
<td>Optical cable 75 m</td>
<td>375</td>
</tr>
<tr>
<td>Deserializer</td>
<td>50</td>
</tr>
<tr>
<td>Demultiplexing</td>
<td>25</td>
</tr>
<tr>
<td>Configurable remapping</td>
<td>40</td>
</tr>
<tr>
<td>Pedestal subtraction</td>
<td>25</td>
</tr>
<tr>
<td>Energy calculation</td>
<td>125</td>
</tr>
<tr>
<td>Digital summation</td>
<td>50</td>
</tr>
<tr>
<td>Data reduction</td>
<td>100</td>
</tr>
<tr>
<td>Multiplexing</td>
<td>25</td>
</tr>
<tr>
<td>Serializer</td>
<td>50</td>
</tr>
<tr>
<td>Optical cable to FEX/Global Event</td>
<td>150</td>
</tr>
<tr>
<td><strong>Total in ns</strong></td>
<td><strong>1270</strong></td>
</tr>
<tr>
<td><strong>Total in BC</strong></td>
<td><strong>50.8</strong></td>
</tr>
<tr>
<td>Additional serialization-deserialization</td>
<td>150</td>
</tr>
<tr>
<td>Fragment building</td>
<td>50</td>
</tr>
<tr>
<td><strong>Total in ns (FEX)</strong></td>
<td><strong>1470</strong></td>
</tr>
<tr>
<td><strong>Total in BC (FEX)</strong></td>
<td><strong>58.8</strong></td>
</tr>
</tbody>
</table>
8.6 System integration

The LASP system will be installed in USA15, ideally close to the entry point of the detector signal fibres and close to the L0 trigger system. As shown in Table 8.2 and 8.3, 372 LASP FPGA units will be needed if 4 FEB2 inputs are connected to one unit and ideally 2 FPGAs are mounted on one ATCA main board, which results in 186 ATCA readout boards.

The arrangement of these boards in ATCA shelves and racks in USA15 is mainly driven by the power dissipation and the cooling capabilities in the shelves and racks. The power per board is estimated from measurements with the LATOME, jFEX and gFEX prototype cards. Figure 8.6 shows the percentage of FPGA logic, memory and DSP blocks as a function of length of a filter implementation for 320 channels processed with data received and sent on in total 96 input and output fibres, together with the corresponding power consumption. From these data, a power dissipation of 0.014 W per processed channel and 0.42 W per transceiver link is derived, where the latter includes the power used by the µPod devices. However, the filter implementation does not make a lot of use of FPGA logic elements, which typically are the dominant power consumers. Measurements performed on a jFEX prototype card with algorithms with more intense use of FPGA logic show that more power per channel is indeed needed. This comparison, together with information from a power estimation tool provided by a FPGA vendor, yields a power dissipation per processed LAr calorimeter cell of 0.47 W taking account that 13 DSP units with corresponding logic elements are needed. Similarly, a different configuration of transceiver and µPod units, as implemented on a gFEX test board, resulted in 0.86 W per link for a link speed of 11.2 Gbps. The power estimation tool indicates that the transceiver power scales linearly with link speed, so that for high speed 25.78 Gpbs, about 2 W per link are assumed. Furthermore, the power consumed by the ATCA main board components are estimated from the power measurement with a LDPS carrier card (LArC [125]), which was measured to be 40 W including a post-processing FPGA which receives data from the processing units and activated data transfer to monitoring PCs.

For the complete LASP readout system, due to the power dissipated by the main board, a maximum power budget of 175 kW is obtained if only 2 FEB2 are handled by one LASP FPGA. If 4 FEB2 are connected to each LASP unit, fewer ATCA boards are needed and the LASP total power can be reduced to 164 kW. Since future FPGA models are expected to consume less power for the same functionality, these estimates can be considered as conservative.

The power per ATCA board is expected to be 720 W for the 4 FEB2 per FPGA option, which is the baseline, and 380 W in case of 2 FEB2 per FPGA. The 720 W per ATCA slot exceeds the ATCA PICMC 3.1 standard, which allows a maximum of 400 W per slot. The higher processing density will only be possible when adapting to the PICMC 3.7 standard, which provides up to 800 W per slot. ATCA shelves which follow this standard are commercially available, but shelves with horizontal cooling, as required to be used in the LHC racks in USA15, need to be developed. Such a development has successfully been done for the 400 W
Figure 8.6: Number of DSP blocks, FPGA logic and memory used during a LATOME test with 320 input channels as a function of depth of an FIR filter implementation (a), and the corresponding power dissipation (b).

The high processing and power density will also be a criterion for the shelf arrangement within a LHC rack. In case the ATCA shelves are only loaded with 8 boards of 720 W and when placing 2 shelves in each rack, the racks will need to provide 13.7 kW of cooling power. This includes the power of the ATCA fan units and shelf managers (1.1 kW per ATCA shelf). If larger racks can be used with space for 3 ATCA shelves, the cooling power must be at least 20.6 kW per rack for the baseline LASP board configuration.

Since the power density per rack will be independent of the power per board or per shelf, the total number of LASP racks is nearly independent of the LASP board configuration. For the baseline setup, 8 high racks with 3 shelves each or 12 regular racks with 2 shelves each will be needed. In case of only 2 FEB2 per LASP FPGA, the number of racks increases only by 25% since more blades can be placed in one shelf yielding a similar power density.

If the TTC distribution is implemented in dedicated boards, the 15 to 24 additional LASP blades will require 2 ATCA shelves, and 1 regular LHC rack. Since the power estimate of the LASP readout system already takes the TTC link power into account, no significant additional power consumption is expected by the TTC distribution system, apart from the 2 kW for the ATCA shelves themselves.

The total power of the Phase-II off-detector electronics finally sums up to 177 kW and the
total space requirements to 26–30 ATCA shelves.

Each unit of the LASP system will be connected to a readout control and monitoring PC via Ethernet connection. These PCs will configure the LASP units and can permanently receive error and warning messages from the system as well as regular monitoring data from the input and output data streams. This will in particular be useful during the commissioning phase of the system, where hardware and firmware functionality and data integrity need to be checked in detail.

### 8.7 R&D milestones

The development of the LASP hardware foresees the design of test boards, a full prototype and pre-production modules before production is started. This includes the main board, the integrated processing units and the rear transition module. One test board is planned to implement the full-size ATCA blade form factor and the selected candidate FPGAs and optical transceivers. It will serve as a platform to study the design choices and possible technical challenges. The form factor, i.e. the realization of a complex PCB design with high-performance and high-power active components and verification of its robustness, is a key element. In parallel, the ATCA AMC and carrier concept will be investigated in detail, as well as the PCIe option. For these more modular designs the available number of PCB layers and connectivity need to be studied. Corresponding test boards are planned to be developed and evaluated. The power consumption of the processing and main FPGAs loaded with realistic firmware and of the optical transceivers are planned to be measured. This will be needed to determined the power dissipation per ATCA slot and to establish that the ATCA infrastructure is compatible with the environment in USA15. Close interaction with ATLAS Technical Coordination is needed in case a solution is preferred which requires a power density beyond 400 W per ATCA slot, established for the Phase-I electronics upgrade. Furthermore, the TTC distribution needs to be integrated into the main FPGA or the processing FPGA of the LASP test module. In case of success, the data and TTC links of the FEB2 can both be routed to the LASP modules avoiding a dedicated TTC distribution system. Data transmission protocol and link speed to FEX and FELIX modules are already implemented and tested in the Phase-I LATOME and LArC hardware and firmware. The output to the Global Trigger Event Processor, however, targets at a higher link speed of 25.78 Gbps. This is planned to be demonstrated using the test boards equipped with the selected FPGAs and high-speed transceiver arrays.

Firmware is a crucial ingredient in all system development steps. Several firmware modules as well as the firmware simulation framework can evolve from the existing Phase-I LATOME and LArC firmware project, as discussed in Section 8.4. Other tasks, like the TTC distribution or low-level interfaces to high-speed links, require the development of dedicated IP blocks. This is planned to be started in parallel to the test board design using commercial FPGA evaluation and development boards and existing LATOME and LArC prototype hardware.
Experience shows that a collaborative effort is also needed in the firmware domain and a mini-series of test boards shall allow the distribution of test setups to the different working groups. Integration tests, including test implementations of the front-end and trigger interfaces, will complete the test board design phase.

In this way, a baseline design can be established in an early stage of the development phase. The schedule, shown in more detail in Section 12.3, allows for a test board iteration in case modifications are required for selecting between crucial design options, possibly at the cost of a shorter first integration period. The initial R&D phase is planned to be concluded by a Preliminary Design Review.

In the second R&D phase, further refinement of the hardware and firmware will follow, together with the design and construction of a full prototype. For the final design, the channel mapping and all interfaces and physical fibre connections to the trigger and DAQ systems must be defined. This requires close interaction with the ATLAS TDAQ community. The goal is to implement the full complexity of the LASP system and perform extensive integration test. Evaluation of the board production quality and selection of final hardware components shall be part of the process. After a Final Design Review, pre-production modules are planned to be built. Those shall pass final production qualification tests including performance tests in a full-shelf system. After a Production Readiness Review the hardware production of the LASP blades and rear transition modules is planned to be launched, accompanied by quality control and followed by installation and commissioning in USA15.
9 Power Supplies and Distribution

The voltages to operate the front-end electronics are provided by dedicated Low Voltage Power Supplies (LVPS). Two different systems are needed to distribute the power to the front-end electronics. One system provides the low voltage power to all front-end electronics which is located inside crates attached to the cryostat warm walls. Additionally one system is needed for the HEC, to provide low voltage power to the preamplifiers and summing boards which are mounted on the HEC detector inside the cryostat. In Section 9.1, the current front-end crate power distribution system and the plans to upgrade it are discussed. Section 9.2 presents the plans to upgrade the HEC power distribution system. Finally, Section 9.3 discusses the R&D milestones on the path to the proposed implementations.

9.1 FEC power distribution system

In the present system, AC/DC Main Converters (MC) located in USA15 are used to generate 280 V and are connected through about 70 m-long cables to LVPS mounted in proximity of the FECs. The LVPS, located between the so-called TileCal fingers\(^1\), contains DC/DC converters which provide the seven low voltages needed, ranging from 4.0 to 11.0 V, including two with negative polarity. The units are custom made (to fit the size of the fingers: approx. 15 cm \(\times\) 30 cm \(\times\) 40 cm), have a power of 3 kW and are water cooled. There are 58 MCs feeding one LVPS each: 16 units are used for each side of the barrel calorimeter and 13 units for each of the two endcaps. The low voltages reach the FEC through connections on its sides (short dimension of the crate in the \(r-z\) plane) and are distributed to the boards (FEBs, calibration boards, \ldots) through pin connections on a bus bar running on the long dimension (\(\phi\)) of the crate.

Low dropout linear regulators on the front-end boards (LHC4913 for positive and LHC7913 for negative voltages [96]) handle the final adjustments. On the new trigger board (the LTDB), installed in Phase-I, the power is distributed through a mezzanine board mounted on the main LTDB PCB and connected to the crate power bus. The mezzanine uses some of the existing voltages as input and converts them to the needed values using LTM4619 DC/DC converters for the digital part and again LHC4913 (positive voltage) and LHC7913 (negative voltage) regulators for the analog part.

\(^{1}\) the “fingers” are extensions of the outer girder of the TileCal modules, which contain and protect services for the TileCal electronics. The gaps between the fingers are used for cables and services and some of them host the LAr LVPS.
9.1.1 New power distribution scheme from Main Converters to front-end

For the Phase-II upgrade, FEBs and calibration boards will be replaced with new units that will mostly use voltages lower than the present ones (between 1 and 4 V). In this situation the existing power distribution scheme will be highly inefficient and so will need to be changed.

Just like today, MCs will be used to generate 280 V DC (or similar voltage) which provides the input voltage to the new LVPS. In any case the existing MCs will be replaced as they will be too old at the start of Phase-II. The new units will be located in the racks occupied by the present units and have very similar requirements (see [94]). They will take a three-phase 400 VAC as input, be remote controlled and monitored and, as in the present units, each 280 V supply will be interlocked by a fast hardware signal which turns the units off in case of an alarm (such as cooling water failure or smoke detection in the front-end electronics area).

The new LVPS will generate only one intermediate voltage still to be decided (48 V, 24 V or 12 V). The units need to provide a power of about 3 kW as today, and be tolerant to the presence of magnetic field and radiation (up to a level that depends on which of the two options described below is chosen). The units will be remotely monitored and controlled. The output voltages will be monitored both in the front-end crate and internally in the LVPS, to verify that the functionality of each module is within the specification requirements.

The final voltages needed by the front-end electronics will be generated from the intermediate voltage directly on the front-end boards by using Point Of Load (POL) converters.

The two options discussed below are under consideration.

Option A

The present LVPS are located in a position difficult to access in case there are problems, or servicing is needed. The opening of ATLAS is, in fact, necessary to access the faces of the barrel or endcap cryostat and replace a faulty unit. Although redundancy can be built in the LVPS (and is built also in the present units), the risk of losing a LVPS and hence a large fraction of the calorimeter acceptance still exists. This represents one of the largest single points of failure of the liquid argon calorimeter.

To overcome this limitation it is proposed to relocate the LVPS in a more accessible position that could allow servicing of the units even during data-taking periods with a short access to the experimental cavern.

For the barrel supplies, a possibility would be to use the six PP2 locations (the “Patch Panel 2” locations of pixel, TRT and other ID services) inside the toroids (or similar locations). The new LVPS positions should be located around the barrel cryostat, as close as feasible to the FECs, so that the units can be distributed more or less uniformly in order to reduce
and equalize the cable length. Given the power involved, assuming a cable length of 20 m and a voltage drop of 5% along the cable, the optimal solution seems to be using 24 V as intermediate voltage on a cable of cross section of 95 mm$^2$. The choice of 24 V as intermediate voltage would also match the input range of candidate DC/DC converters such as the LTM4619 (see Section 9.1.2). Smaller intermediate voltages, e.g. 12 V, would make the cable size unmanageable. Smaller cross section cables can be used if the intermediate voltage is increased to 48 V. However, this intermediate voltage would make the choice of POLs more difficult.

In the endcap a similar solution could be obtained by relocating the LVPS around the external surface of the TileCal modules, in positions that can be accessed also when the ATLAS detector is closed and that do not obstruct the displacement of the endcaps through the Muon Spectrometer when ATLAS is opened.

In this configuration the MCs will remain in their present position (USA15) but their cables will need to be rerouted to reach the LVPS in their new locations. For the barrel LVPS, a completely new positioning of the cables from the MC to the LVPS will be needed. Most likely a new dedicated cooling station, with the usual under-atmospheric-pressure operation will need to be built, installed and connected to the new LVPS. In the endcap, the existing cables can be likely reused (including the path in the cable chains) and only the last part of the cable path will be modified to reach the new LVPS positions. In these locations the new LVPS can have a more standard form factor and be engineered as modules in a 4U-like Eurocrate like, e.g. the solution that is being developed for the NSW in Phase-I, or in a current pixel PP2-like box, whose size is about 33 cm (W) × 43 cm (L) × 23 cm (H). With respect to the present position the LVPS would be exposed to lower radiation doses (see Table 3.1) but a potentially (depending on the chosen position) higher magnetic field (up to 0.55 T).

Possible positions for the new LVPS are being discussed with ATLAS Technical Coordination. A site inspection from both Liquid Argon and Technical Coordination personnel has been performed and no fundamental drawback to this option has been found. A few locations where both barrel and endcap LVPS could be positioned have been identified. It seems also possible to reroute the 32 (including the return lines) cables per barrel side from USA15 to the new LVPS as well as lay down an analogous number of cables from the LVPS to the front-end crates. In the endcap, as already said, the routing of the cable should not pose any problem. The next step in pursuing this option would be to prepare technical drawings illustrating the proposed solution.

As the system is made of three power “regions” (the AC/DC conversion in the MC, the DC/DC conversion in the LVPS and the voltage regulation in the POLs) connected by cables of significant length, the presence of resonances needs to be avoided. Tests will be performed with prototypes of the system to allow a validation of the design.
Option B

In this approach the intermediate voltage will be generated by new units that will replace the present LVPS and will be located in the same position. These new units might be either a newer generation of the present supply made by Wiener, modified to provide only one voltage instead of seven, or a different LVPS. In both cases the design must be built to provide high redundancy in the units in case of failures as the units in the present locations are not accessible for repair or replacement when ATLAS is closed. A prototype [97] has been developed in collaboration with CAEN, based on a DC/DC Phase Shifted Converter. The prototype converts 280 V to 12 V at a switching frequency of 100 kHz, providing 4.5 kW of power. The unit is made of three independent units of 1.5 kW each wired in a voting 2oo3 scheme in which the availability of two units out of three is required for the system to operate.

The CAEN prototype is not radiation tolerant and work is on going to evaluate the use of GaN devices instead of Si power MOSFETs. The expected radiation doses in this region are given in Table 3.1. Moreover, a maximum magnetic field of 0.1 T in these positions, does not represent a problem as demonstrated by the present Wiener units that are operating correctly in this condition.

9.1.2 On-board power distribution

Independent of the option chosen, the final voltage step-down is performed by POLs on each front-end board. The supplies can be provided by the use of DC/DC converters like the LTM4619 already in use on the LTDB in Phase-I. The LTM4619 is a dual-output non-isolated switching mode DC/DC converter. It can deliver up to 4 A (DC current) for each output with few external input and output capacitors. This module provides precisely regulated output voltages programmable via external resistors from 0.8 VDC to 5.0 VDC with 4.5 V to 26.5 V input voltages.

Moreover, we plan to provide adequate filtering with new regulators that replace the LHC4913 which are going to become obsolete. Several commercially available IC devices for voltage regulation were tested for radiation tolerance in the framework of the R&D for the Phase-I LTDB. A good number of devices met or even exceeded the Phase-I radiation requirements. A new radiation study of voltage regulators (positive and negative, if needed) will be performed to select devices that could be used in Phase-II.

The power section of the LTDB is implemented as a mezzanine board mounted through pins on the main LTDB board. The mezzanine takes as input some of the voltages created by the current LVPS and converted them to the voltages needed by the LTDB. For Phase-II, these mezzanine boards will be removed and replaced by mezzanines that, following the new power distribution scheme, will generate all the needed voltages from just one voltage generated by the Phase-II LVPS.
9.2 HEC power distribution system

The LVPS for the HEC [11] (HEC LVPS) provide the power for the cold readout electronics [25] and need to be exchanged due to age and higher radiation hardness requirements.

In the area of the HEC LVPS (between the TileCal fingers at $650 \text{ cm} < |z| < 690 \text{ cm}; 385 \text{ cm} < r < 425 \text{ cm}) the estimated radiation levels are reported in Table 3.1 assuming a total integrated luminosity of $4000 \text{ fb}^{-1}$. The devices need to operate in magnetic fields of 0.03 T.

The new HEC LVPS can largely follow the design of the current HEC LVPS [98] because the cold readout electronics for the HEC will remain unchanged since radiation tests [24] showed that the cold preamplifiers will remain operational under the projected HL-LHC conditions. In total there are 160 Preamplifier and Summing Boards (PSB) per endcap side. Each side is divided in 4 quadrants with one LVPS (LV power box) serving one quadrant which is divided in 8 $\phi$ sectors (wedges) each with 5 PSBs for a total of 40. Possible changes for the position of the HEC LVPS to other places, more accessible with ATLAS in closed position, between the TileCal fingers are being investigated. In addition, possible single-points-of-failure of the current design will be reviewed and, in case they are deemed necessary, options to mitigate them will be studied.

Some components of the current power supplies do not satisfy the radiation hardness requirements for the HL-LHC while some components are no longer available. Based on measurements with the (cold) readout electronics of the HEC which will remain unchanged for Phase-II the following specifications can be defined:

- 3 supply voltages per PSB with the following voltages and currents at the input of each PSB:
  - 7.2 V and up to 0.75 A
  - 3.1 V and up to 0.35 A
  - −1.5 V and up to 0.15 A.

  Further information on these 3 supply voltages are provided in Appendix B.

- 1 LVPS per quadrant
- 40 PSBs or channels per quadrant (320 in total)
- output redundancy (two DC/DC converters per output like in the current system, each converter being capable to support the full load)
- remote controllable via ELMB++ (see below)
- a backup control system with reduced functionality in case the ELMB++ is not working
Critical components to select for radiation hardness and compatibility with the operational requirements given above are:

**PowerMOSFETs:** The heart of the DC/DC converters are PowerMOSFETs. Some radiation tests with neutrons have been performed and a number of devices were found to be radiation tolerant enough to replace those in the converters of the current power supplies.

**Low Voltage Regulators:** positive and negative Low Voltage Regulators (LVR) are needed. The devices currently in use (LHC7913 and LHC4913 [96]) are within specs and will be acquired through CERN.

**ELMB++:** a successor for the current ELMB, steering and monitoring the power supply. The ELMB++ is discussed in Chapter 10. For the HEC LVPS the size of the ELMB++ should not be larger than the ELMB due to space constraints, and it must fulfil the radiation specs in Table 3.1.

**LogicChip:** a successor of the current chip that serves both as control and monitor of the low voltage regulators and of the serial interface that provides redundant control in case any of the ELMB++ fail. This can be a radiation hard FPGA.

A first set of prototype DC/DC converters with exchanged PowerMOSFETs and other components but largely following the original design has been produced by Wiener and is currently under test at MPI Munich.

### 9.3 R & D Milestones

Option A is considered the baseline solution for the FEC power distribution system because of its advantages both from a technical point of view and from the point of view of the reliability and maintenance of the detector. Given the different requirements between Options A and B in terms of magnetic field tolerance and radiation levels, it is important that a decision between the two options is taken in relatively short time. By the end of 2018 the plan is to produce a power board of enough power (at least 1 to 1.5 kW) that can be operated successfully in presence of magnetic field. This board would represent the building block of the future LVPS. Moreover, detailed technical drawings from Technical Coordination showing whether the positioning of the LVPS outside of the Tile fingers is feasible should be available. If both conditions are met by mid-2019, the development of a pre-prototype satisfying most of the requirements will start (this will include the modules and also a crate to host them) and a final layout of the powering scheme for both barrel and endcap will be prepared. A full fledged prototype will be produced by mid of 2021. If it is found that it is not possible to continue with Option A, Option B will be pursued by both asking the vendor of the present LVPS to modify the design to fit our new requirements and by finalizing the design of the Phase-II prototype already produced. By 2020 one of these two options will be chosen in order to arrive to produce a prototype end of 2021.
For what concerns the HEC LVPS, the design of new power boards with new DC/DC converters is already in an advanced stage. Radiation tolerant PowerMOSFETs have already been selected and are included in the design. First prototypes have been produced and will be tested by MPI Munich, including in-situ tests under irradiation at the end of 2017. Depending on the outcome of the irradiation tests the design of the DC/DC converters can either be accepted or needs a further iteration.

Radiation tests for selecting the needed FPGAs are planned for 2018. By end of 2019 the final decision on the FPGA choice should be taken.

Mechanics and components provided by CERN (ELMB++, optical links) need to be integrated by middle of 2020 and by the end of 2020 final full prototypes for the entire HEC LVPS boxes can be tested under irradiation.

In 2021 the full system can be reviewed and final production is planned for 2021-2022.
10 Detector Control System

The task of the LAr Detector Control System (DCS) is the control and monitoring of the LAr calorimeter, of its subsystems, and its infrastructure in a coherent and safe way. In this chapter, the current implementation of the LAr DCS system and its components are briefly discussed in Section 10.1. For the Phase-II upgrade, the LAr DCS system design and architecture are not expected to change dramatically; the necessary modifications that are foreseen are outlined in Section 10.2, followed by an overview of the R&D milestones towards the implementation of the upgraded system in Section 10.3.

10.1 Current LAr DCS system

LAr has four control subsystems; the HV subsystem delivers HV for all LAr calorimeters and purity monitors. The subsystem controls approximately 5000 HV channels and 23 HV crates. The Front-end Crate Low Voltage subsystem (FEC LV) is responsible for the control and monitoring of power for the front end electronics distributed in 56 front end crates; the HEC Low Voltage system controls and monitors the power of the HEC cold readout electronics; the VME crate subsystem controls and monitors the LAr TTC and ROD crates. There are also three additional monitoring subsystems: the first one monitors the detector module temperatures using approximately 450 precision PT 100 probes and the second one monitors the purity of the liquid argon using 30 dedicated monitors containing radioactive sources. Finally, the dedicated DAQMON subsystem monitors FEB and ROD G-link temperatures using data points provided by the LAr online software.

An additional level of monitoring and safety interlocks is provided by the independent ATLAS Detector Safety System (DSS). The DSS system is complementary to the DCS system and is centrally operated and maintained by ATLAS. The DSS employs a large number of dedicated sensors which detect safety hazards including fire, smoke, and water leaks and covers all LAr systems. No significant changes to the current DSS system are foreseen for the Phase-II upgrade and any incremental upgrades will be organized with ATLAS Technical Coordination.

The current LAr Detector DCS follows the paradigm outlined for the central ATLAS DCS [99] architecture which consists of a front-end (FE) system and a back-end (BE) system. The FE includes the DCS hardware such as different sensors, power supplies, and I/O devices. In the current configuration, LAr uses the Embedded Local Monitoring Board [100] (ELMB) as...
a common I/O device. The ELMB provides 64 analog and 24 digital channels as well as a CAN bus interface. It is radiation hard for integrated TID doses up to 140 Gy, NIEL doses up to $4 \times 10^{12}$ neq/cm$^2$, and for up to 1 SEE for $1 \times 10^{11}$ protons/cm$^2$. As a consequence, it does not satisfy the radiation tolerance requirements at the HL-LHC (see Table 3.1). Three LAr DCS subsystems, the HEC LV, FEC LV, and temperature monitoring subsystems use 170 ELMBs.

For the BE, the industrial Supervisory Control and Data Acquisition (SCADA) system SIMATIC WinCC OA serves as base of the back-end software. The subsystem control, monitoring, and data acquisition and visualization in the LAr DCS is currently organized as 14 WinCC OA projects running on 11 PCs.

### 10.2 Modifications for the Phase-II upgrade

For the Phase-II upgrade, the main architecture and design of the LAr DCS system will be kept as currently is. As mentioned above, a few elements of FE and BE hardware implementation would have to be replaced. In addition, the monitoring via the DAQ path will be replaced and improved.

The ELMBs will be replaced with a new device, dubbed ELMB++. The GBT-Slow Control Adapter ASIC [127] (SCA) will be used as a base for the new ELMB++ device. The device consists of an integrated circuit (Figure 10.1) built in a commercial 130 nm CMOS technology and is the part of the GBT chipset, the purpose of which is to distribute control signals to and monitor signals from the front-end electronics embedded in the detectors. It is connected to a dedicated electrical port on the GBTX ASICs through 80 Mbps dual redundant bidirectional electrical datalinks, dubbed “E-links”.

The ELMB++ will be a central CERN development. The final design of this device has not yet been fixed, but there exists a proposal to build two types of ELMB++ devices which must fulfill the radiation tolerance requirements outlined in Table 3.1. The first type would be a simpler “Satellite”-ELMB++ board that would comprise two GBT-SCAs and a DC/DC converter and would provide either one or two E-links, 62 analog input channels, 16 analog output channels, and JTAG, I2C, and SPI interfaces which will be available for the user. The second ELMB++ type is a radiation hard “Hub”-ELMB++. This device will be used as a hub for up to 19 Satellite-ELMB++ devices connected in a star point topology [101]. The Hub-ELMB++ will include a GBTX and a VTRX to send DCS data to the back-end via an optical link connection to a new network interface board, dubbed ELMB++ FPGA, installed outside the experimental cavern. A diagram showing the connections between the elements of the proposed ELMB++ architecture is shown in Figure 10.2.

Power for the Satellite-ELMB++ can be provided via the E-links. For the Hub-ELMB++, depending on their eventual installation location, the options of either using the existing cable routes, or installing new dedicated power supplies close to the detector, are being
1 SPI serial bus master channel with 8 individual slave select lines. The Serial Peripheral Interface (SPI) channel implements a full duplex synchronous serial bus master with a single transaction length of up to 128 bits and a programmable transfer rate up to 20 MHz. It supports all the standard SPI bus operating modes: 00, 01, 10 and 11. It also integrates 8 independent slave-select lines. The bus frequency spans from 156KHz up to 20MHz in 128 user programmable steps. The SPI channel is implemented around a 128-bit shift register that serializes and de-serializes the bit-streams between the MISO and MOSI SPI lines and the internal parallel bus. The SPI channel is protocol agnostic. The user specific protocol is implemented in FPGA circuitry residing at the control room electronics. The SPI channel can be powered down to conserve power.

1 JTAG serial bus master channel. The JTAG channel can perform bus transactions of up to 128-bit length. Longer transactions are also possible by segmenting them and having them executed on consecutive channel commands. The interface implements an asynchronous reset line of configurable pulse width. The bus frequency spans from 156KHz up to 20MHz in 128 user programmable steps. The JTAG channel is implemented around two 128-bit shift register that serializes and deserializes the bit-streams between the TMS, TDO and TDI lines and the internal parallel bus. The JTAG channel in the SCA does not implement a JTAG.

Figure 10.1: GBT-SCA block diagram.

Figure 10.2: Connection diagram for the elements in the proposed ELMB++ architecture.
considered. The Hub-ELMB++ optical links can potentially be routed together with the power cables, or could be routed together with the front-end readout fibres.

Finally, there exists a different proposal to use so-called “mobile receivers” instead of the combination of the Hub-ELMB++ and ELMB++ FPGA, which avoids the intermediate optical GBT connection. This scheme could potentially be more economical but may not be a viable option if the maximum possible length of the E-link between the satellites and the receiver is not sufficient.

In order to reuse as much as possible the existing back-end infrastructure and WinCC OA projects, it is desirable to have as much as possible one-to-one correspondence between the supervised data points of the current and future Phase-II DCS systems. The current baseline option foresees the use of Hub- and Satellite-ELMB++ devices, minimally replacing the ELMBs that are currently installed.

For the LAr DCS subsystems, the baseline option considered for the Phase-II upgrade is to exchange the current ELMBs with Satellite-ELMB++ devices on a one-to-one basis. If “Option A” for the FEC power distribution scheme is adopted, which calls for a relocation of the LVPS to more accessible locations (See Section 9.1, additional Satellite-ELMB++ devices will have to be added to monitor and control the new LVPS. The star point topology scheme and the exact number of Hub-ELMB++ devices can only be precisely determined when the new locations of the FEC and HEC LV PS is defined. An initial estimate can be obtained by a scheme that reduces the cable lengths between the satellite ELMBs and FEC sensors. The projected total number of devices, under this approach, and its breakdown into the different LAr DCS subsystems is shown in Table 10.1. The projections include a number of devices that will be needed for development and test systems deployed in the laboratory.

Table 10.1: The projected number of ELMB++ components needed for the Phase-II upgrade of the LAr DCS system in the current baseline, assuming “Option A” for the FEC power distribution.

<table>
<thead>
<tr>
<th>Component</th>
<th>LAr DCS subsystem</th>
<th>Development systems</th>
<th>Total</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Temp. HEC LV FEC</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Hub-ELMB++</td>
<td>3 9 10</td>
<td>9</td>
<td>31</td>
</tr>
<tr>
<td>Satellite-ELMB++</td>
<td>29 73 74</td>
<td>98</td>
<td>274</td>
</tr>
</tbody>
</table>

An additional stream of DCS monitoring data, for example, temperatures and voltages of the on-detector and trigger electronics, will be delivered via the Phase-II upgraded DAQ system based on FELIX. The transfer and configuration of this data within FELIX should be independent of the data provided via the ELMB++ path. This goal could be reached by using DCS middleware interfaces (such as OPC Unified Architecture) [128, 129]. A preliminary scheme of the DCS data flow via the DAQ system is presented in Figure 10.3.
For the Phase-II upgrade, the hardware implementation of the LAr off-detector readout electronics will be based on the ATCA platform which will be the replacement of the VME system currently in use within ATLAS. As a consequence, a new WinCC OA project for the monitoring and control of the ATCA shelves will have to be created in replacement of the project currently controlling the LAr VME-based ROD system. The ATCA shelf monitoring system hardware implementation is expected to be very similar to the one planned for the LAr Phase-I upgrade [2] which will employ the functionality provided by and adhere to the specifications of the ATCA standard. In the ATCA standard, a “Shelf Manager” board controls the different ATCA elements inside a shelf. The DCS system and the WinCC OA monitoring project will connect to and subscribe to information provided by the ATCA shelf manager via the CERN network. The shelf manager is connected to the external CERN network and, via the Intelligent Platform Management Bus (IPMB), to an IPM controller (IPMC) mounted on each ATCA blade housed in the shelf. The IPMC is connected to an optional AMC through a Module Management Controller (MMC) mounted on the AMC, which is connected to a local IPM bus (IPML). A first prototype for the Phase-I system is under development.

### 10.3 R&D milestones

Most of the development of the proposed Phase-II LAr DCS system, in the current baseline, is contingent on the availability of the new ELMB++ devices, which will be produced by ATLAS. The ELMB++ is currently expected to be available in the beginning of 2020.

For the LAr temperature monitoring system, a first test will start when the new ELMB++ devices and the relevant OPC UA server are ready during LS2. In addition, as discussed in Section 9.3, during the development of the FEC and HEC LVPS, the associated DCS systems are also planned to be developed. Dedicated FEC LVPS WinCC OA test projects will be created while the prototype is being finalized. Furthermore, an exact mirror of the HEC LV system is planned to be constructed and a full test to be performed at MPI Munich. Finally, as discussed previously, a first prototype of the ATCA shelf monitoring for the Phase-I upgrade
is under development, with an architecture very similar to the one proposed for the Phase-II DCS system.
11 Installation and Commissioning

The installation of the upgraded ATLAS detector, and its commissioning for eventual use in physics production in Phase-II, will be the culmination of several years of effort. As discussed in Section 11.1, for the LAr calorimeter, the installation plans include the installation of the off-detector electronics, the mounting of the front-end electronics and their power supplies, and the routing of new cables. Finally, while it is too early to develop a precise plan, Section 11.2 discusses basic considerations in commissioning the system.

11.1 Installation

The installation of the LAr Phase-II Electronics will have to be planned within the boundary conditions of a very tight LS3 schedule for UX15. Whereas the installation and commissioning of the LAr signal processors and the fibre plant in USA15 will be rather independent from the work going on in UX15, the installation of the optical fibres, the HEC low-voltage power supplies, the front-end boards, the calibration boards, and the low-voltage power supplies for the front-end electronics will be driven by the accessibility of the front-end crates, the TileCal finger region and the cable chains. In the current LS3 schedule (V4), the access to the LAr front-end crates is foreseen between Oct. 1, 2024 and Oct. 17, 2025. Each of the four detector faces will be accessible for at least three months in a row, exact details about the access and scaffoldings needed will be worked out in the coming years. It is expected that a lot of experience will be gained during the Phase-I installation (baseplane exchange, FEB removal and re-installation, fibre connection, LTDB installation and LDPS installation). We estimate that three teams of two people (one engineer and one technician each) can perform the installation work within the allocated three months per detector face. Before installation each component will be tested thoroughly and reception tests at CERN will be performed.

The installation for each group of deliverables is briefly discussed below:

- Off-detector electronics in USA15: ATLAS Technical Coordination is planning refurbishment work inside USA15 and the installation of ATCA racks. Once this is finished access is basically always available. The installation of the off-detector electronics is rather simple and covers the placing of crates, boards, patch panels, fibres, fibre plant, etc. The necessary rack space is discussed in Chapter 8. Consultation with Technical
Coordination has started to determine which racks need preferred locations closer to UX15 for latency reasons.

- Front-end electronics: this is clearly the most constrained installation since about 1800 front-end and other boards in 58 FECs must be removed, new front-end and calibration boards installed and all services connected to allow for the final commissioning and sign-off on each complete crate before access is lost\(^1\). Given the amount of effort and the limited time frame available, it will be imperative to operate with several teams on several FECs simultaneously.

- Low-voltage power supplies: The baseline option for the low-voltage power supplies of the barrel calorimeter foresees the installation of new DC/DC converters in the region between the inner and middle MDT chamber layers in several azimuthal positions. These DC/DC converters will replace the current low-voltage power supplies mounted between the TileCal fingers with existing water cooling, however it is likely not possible to extend these cooling branches to the new locations. Under-pressure water cooling will need to be made available at these new locations (most likely a new dedicated small cooling station will be necessary). The low-voltage power supplies will be needed for the commissioning of the new front-end electronics and therefore need to be installed prior or in parallel to the board installation. The endcap low-voltage power supplies will be installed at locations close to the TileCal fingers, preferably in accessible positions (see Chapter 9) and will be connected to the existing cooling loops.

- Long fibre cables: the laying and routing of the cables will be performed by the ATLAS TC team. The routing has to be understood beforehand to determine the exact fibre lengths and probably will differ slightly from the routing of the legacy installation since some areas (e.g. Tile Barrel) are not accessible. All readout fibre cables from the endcaps will be routed through the existing cable chain in sector 9, where space will be freed by removing the legacy analog trigger cables (diameter of 12.5 mm). Together with the readout fibre cables from the barrel they will be routed through the so-called “trigger holes” in the USA15-UX15 wall. The dimensions of the trigger holes were measured during the 2016/2017 technical stop and it was established that there is enough space to be able to accommodate all new LAr readout cables. All these fibres will also be needed for the commissioning of the new front-end electronics and should as well therefore be laid for each detector face before the board installation.

11.2 Commissioning

The commissioning of the system must take place in parallel with the installation operation. Depending on the overall LS3 installation schedule, access to some front-end locations will be possible after the three-month period of initial installation.

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\(^1\) Additional access for repair or exchange of some boards will be possible after the three-month period of initial installation.
be limited during certain periods of the shutdown. After installation, there is an 8-week commissioning period with full access foreseen from October 2025 until January 2026. It is planned to commission each front-end crate immediately after installation and test the full functionality, even though final sign-off can wait until the end of 2025. In order to do this final sign-off, the full infrastructure must be available, power (including the new power supplies), DCS, and online software. Beyond this infrastructure, which will be installed by the LAr group, other important prerequisites for the commissioning will be taken care of by technical coordination. The optical fibres will need to be installed before the commissioning can start, the front-end cooling system must be operational and be extended to also serve the LVPSs at their new locations. To achieve that, we are in close coordination with the technical coordination teams.

The commissioning of each front-end crate will then consist in taking calibration runs to measure and analyse quantities like noise, coherent noise, crosstalk, electronics gain, pedestals, pulse-shapes and auto-correlation. It is also crucial to detect any dead readout channels or calibration lines and compare them to the dead-channel lists of the legacy system to determine whether a detected dead channel might be broken inside the detector.
Part III

Project
12 Project Organization

This chapter describes the planning, organization, and management of the LAr Phase-II upgrade project. Section 12.1 discusses the organization of upgrade projects in ATLAS in general and the management of the LAr Phase-II upgrade project more specifically. The foreseen available resources are briefly discussed in Section 12.2. Section 12.3 discusses the upgrade schedule and timeline, including a detailed breakdown for each element of the project of the milestones towards its completion. The risks involved with the project and the strategies to mitigate them are discussed in Section 12.4. Finally, in Section 12.5, the cost estimates are presented.

12.1 Project plan and management

12.1.1 Upgrade organization in ATLAS

The highest-level executive body in ATLAS is the Executive Board (EB), chaired by the Spokesperson with the Technical Coordinator (TC) as deputy chair. The overall steering and monitoring of the upgrade activities is delegated to the Upgrade Steering Committee (USC), which is a sub-committee of the EB, with an extended membership [130]. The USC is chaired by the Upgrade Coordinator (UC). The review and approval of Upgrade Projects is steered by the UC and the USC, with approval of such projects by the EB, subject to endorsement by the Collaboration Board (CB). The UC also oversees and monitors the overall upgrade planning and schedules. The management of approved Upgrade Projects rests with the Upgrade Project Leader (UPL) of that Upgrade Project, acting together with the parent system’s Project Leader and Institute Board chair. The Upgrade Coordinator should be well informed of the activities in the Upgrade Projects, and interacts regularly with the Upgrade Project Leaders to anticipate technical, schedule, resource, or other problems.

The TC, supported by the Technical Coordination organization (TCn), is responsible for ensuring that all the upgrades can be successfully integrated in the ATLAS detector, that their installation schedules are compatible with shutdown schedules, and that there are adequate resources allocated for the installation and commissioning of the upgrade detectors. To this end the TC has organized an Upgrade Project Office (UPO) that provides technical support for the Upgrade Projects and the Upgrade Coordinator. Moreover the TC is responsible for the upgrade of all the common infrastructure needed for the upgrade program.
The Review Office is an independent body embedded in Technical Coordination. In close collaboration with the UC, the TC, and the UPLs, the Review Office develops and organizes technical reviews for the components of the upgrades following the ATLAS review strategy, comprising specifications, preliminary design, final design, and production readiness reviews.

12.1.2 LAr Phase-II Upgrade Project Leaders

The LAr Phase-II Upgrade will be performed by a group of ATLAS institutions that commit to developing, designing, constructing and installing the new components, and to commissioning the upgraded system. The group includes both institutions which were already involved in the construction and/or operation of the current LAr system as well as new institutions. All institutions participating in the LAr Phase-II Upgrade are, or will become, members of the LAr Institute Board (IB), which is usually referred to as LAr Group Representatives.

The LAr Phase-II Electronics Upgrade is a necessary step to comply with HL-LHC radiation requirements and the ATLAS Phase-II readout architecture [5, 6]. After the Initial Design Review (IDR), the approval by the Upgrade Steering Committee and the endorsement by the ATLAS CB, this project has become an ATLAS Upgrade Project as outlined in [131]. Two (interim) co-Upgrade Project Leaders (co-UPLs) have been chosen by the LAr management and have been endorsed by the LAr IB. These (interim) co-UPLs are part of the LAr Steering Group and represent the LAr Phase-II Electronics Upgrade Project in the ATLAS Upgrade Steering Committee. The co-Upgrade Project Leaders report to the LAr Project Leader and chair the LAr Phase-II Electronics Upgrade Steering Group. Once the TDR is accepted, a search committee will be formed to identify the best candidates for UPL election. The LAr IB will elect the UPLs.

12.1.3 LAr Phase-II organization

As described above this project is led by two (interim) co-Upgrade Project Leaders. The project’s Work Breakdown Structure (WBS) is shown in Table 12.1. At Level-2, the project is divided into on-detector front-end electronics, and off-detector electronics. Each of these is further broken down into its main components, etc. At the time of writing of the TDR, Level-3 managers have been appointed for the front-end electronics, where R&D is well underway, whereas for the off-detector electronics only Level-2 managers have been appointed. Indeed, the off-detector electronics R&D work will only start in late 2017, when the Phase-1 system, on which it is modelled, enters its production phase. In addition to the contents of the WBS, there is a simulation effort that investigates low-level aspects (e.g. signal shaping) as well as reconstruction performance and physics.
Dedicated working groups have been created, led by one or two coordinators each. These coordinators are all members of the LAr Phase-II Electronics Steering Group which is organized and chaired by the (interim) co-Upgrade Project Leaders. The LAr Project Leader is an ex-officio member of this steering group. The current structure consists of six working groups, one covering the work on physics and performance simulation whereas the other five cover the different deliverables:

- Front-end board
- Calibration board
- Front-end powering (LVPS, HEC LVPS)
- Off-detector electronics
- Services and DCS (not active yet)
- Physics, performance & hardware simulation

In addition, a resource coordinator and a risk manager have been appointed. The resource coordinator maintains a database of required and pledged resources, both financial and human. The risk manager develops and maintains the risk register in coordination with the Level-1, 2 and 3 managers. The project’s approach to risk management is described in more detail in Section 12.4. The organization chart is displayed in Figure 12.1. Compared to the WBS, both front-end power supply Level-3 items are merged into one working group (coordinated by both Level-3 managers), the simulation group is added, and no working groups exist for deliverables consisting exclusively of commercially available components.

The LAr Phase-II Electronics Upgrade Steering Group meets typically monthly, including at every LAr Week. The subgroups currently meet at similar frequency, but Phase-I experience indicates bi-weekly meetings will be necessary as the prototyping phase sets in.

### 12.1.4 Technical Milestones

All of the custom components used in the LAr upgrade have to pass through a series of reviews before orders can be placed for procurement of parts and production of the deliverables, and before they can be used in the upgrade of the detector. These reviews are used to ascertain the quality and reliability of the components at various steps in the development and production process. They can also help to shorten the design phase, by enforcing in-depth presentations of the status at various stages. Reviews are conducted as (usually) half-day or full-day meetings of the group of people in charge of design and construction of the component with a team of reviewers. The review team is designated by the UC or by the Upgrade Review Office, and includes experts in the relevant technology, and, if applicable, users of the object to be reviewed or those interfacing other objects to it. This procedure is the ATLAS standard.
There are four main reviews for each custom component:

- **Specifications Review** This review is used to validate the specifications document, which describes the required functionality and performance of the device, its interfaces to other devices, tolerance to radiation, and reliability. The specified interfaces must be cross-checked for consistency with the corresponding component’s specifications.

- **Preliminary Design Review (PDR)** The PDR determines whether the design is sound and meets all requirements, including all interfaces to other components.

- **Final Design Review (FDR)** The FDR is used to establish that the final prototype meets all requirements. Integrated tests with prototypes for the components the item interfaces directly to are required at this stage. A successful FDR gives the green light for a small pre-production.

- **Production Readiness Review (PRR)** The results from pre-production are used to verify that larger scale production can be done with the acceptable yields, and that the quality control process is sufficiently thorough to filter out devices that will not meet
the performance specification over the lifetime of ATLAS. After successful PRR, full production is launched.

These reviews mark the transitions between different phases in each component’s development and production schedule, and are thus used as key technical milestones in the overall project schedule.

12.1.5 Interface with the Trigger and Data Acquisition Upgrade Project

The LAr Phase-II upgrade concerns the trigger and readout electronics chain. From the LASP, data flows to both the trigger and DAQ systems. To ensure the LAr, Tile and TDAQ requirements and specifications match, regular, typically monthly, calorimeter–TDAQ meetings are organized. These meetings have led to the specifications described in this TDR. Evolutions and/or refinements of these specifications will require sign-off from all stakeholders and corresponding specifications documents will be stored in EDMS.

12.2 Human and financial resources

Many Institutions have already stated their intentions of contributing to the LAr Phase-II electronics upgrade project, and many of them have already been working on R&D and design of the various components of the system. The details of responsibility and sharing will be defined in the Memorandum of Understanding (MoU) for the LAr Phase-II electronics upgrade, after the TDR.

Surveys of the interests of Institutions and of the available manpower have been performed in the framework of the Scoping Document (SD) in 2015, and have been updated after the Initial Design Review (IDR) and the Kick-Off meeting in March 2017. These surveys indicate that the human resources required for the LAr Phase-II electronics upgrade are available. Many of the interested Institutions have long-term experience in the LAr calorimeter system. The ongoing Phase-I upgrade project is in the last R&D stages and in preparation for component production and installation, so that system and hardware designers and engineers that have been involved in Phase-I were already able to contribute significantly to the Phase-II R&D. Further iterations are ongoing to match capabilities with requirements, in preparation for the MoU. The cost of the project is expected to be covered by the Institutions participating in the LAr Phase-II electronics upgrade project, with their respective Funding Agencies. Discussions among the Institutions and the Funding Agencies are ongoing in order to define the detailed list of deliverables, responsibilities, and the sharing of the project cost.
12.3 Schedule and milestones

12.3.1 ATLAS schedule for the Long Shutdown

The LAr Phase-II Electronics Upgrade development and production schedule is in large part driven by the ATLAS installation schedule for LS3, as it defines when the different components will need to be ready.

The current version of the LS3 installation schedule during LS3 is shown in Figure 12.2. The installation of the new LAr readout electronics is expected to begin in October 2024. The preliminary order of installation is to start with endcaps A and C and continue with barrel sides C and A. This sequence optimizes the access to different parts of the detector for the different subdetectors. (The ITk will be inserted through the C side.) Based on experience from the “refurbishment” campaign from 2007, where all FEBs had to be removed and reinstalled, we expect each of these four installation campaigns to last between 8 and 12 weeks: 12 weeks for the first one, gradually going down to 8 weeks as procedures are optimized. For now, four 12-week periods are scheduled, so that the electronics installation is completed by October 2025. This is followed by a commissioning period during which the front-end crates are still accessible for short interventions. The closing of the calorimeter barrels is scheduled for January 2026. This schedule is subject to modification if required by the installation procedure of other detector components. The next sections give high-level descriptions of the development and production schedule for the different upgrade components.

The project schedule relies heavily on experience from the original construction and Phase-I upgrades, and reflects both the number of test chips and prototype iterations needed in those projects, as well as the actual durations of the various phases of development and production observed. For both the front-end and off-detector electronics, approximately one year of schedule float is available to absorb delays.

12.3.2 Front-end electronics

To meet the radiation tolerance criteria, the complex functionalities in the front-end electronics will be implemented using 6 ASICs (Preamp/shaper, HEC preshaper, ADC, IpGBT, VL+ and calibration pulser). Experience from the ATLAS construction and Phase-I upgrade shows that for the more complex of these, three submissions are needed before production: two for R&D and first integration steps, then a prototype to be used for large scale integration tests with other components. This is then followed by pre-production and production. Transitions between these phases are marked by the Preliminary Design Review, Final Design Review, and Production Readiness Review milestones. The preamp/shaper and ADC schedules are shown in Figure 12.3, and the optical link and FEB2 schedules in Figure 12.4.
Figure 12.2: Schedule of the detector installation activities of ATLAS during LS3. The installation of the LAr front-end electronics is foreseen to start in October 2024 and to take about 1 year in total.

For the preamp/shaper, the first test chips in 65 nm (HLC1) and 130 nm (LAUROC) CMOS have been fabricated. Tests of both devices will continue and lead to choices of technology and architecture ahead of the second test chip. This next iteration (in a single technology) will be focused on the improvements needed to meet the noise requirements for the final chip. That version will be used in the first FEB2 development board, the analog test board. In parallel, the additions needed to have a single chip for both the electromagnetic and hadronic endcap calorimeters will be designed. The prototype will have the full functionality and will be used in the FEB2 slice test board, a (probably) 32-channel version of FEB2. The first ADC test chip, a single-channel device that includes both a DRE and SAR, which can be used together or separately, is now being tested. The next version will contain two channels, and most of the “logistics” necessary for operation: a PLL to synchronize the high speed clocks, voltage reference drivers, etc. Performance of this test chip will be reviewed at the PDR to evaluate if the fully custom ADC or a semi-custom ADC (using a commercial core ADC IP block) should be the baseline, or if fall-back to a COTS ADC solution is warranted. Assuming a (semi-)custom ADC is selected, the ADC prototype, with 8 channels, will be developed and used in the slice test board for integration tests with the preamp/shaper. lpGBT prototypes are expected on the same timescale and will be integrated on the slice test board as well. Pre-production ASICs will be used for the prototype FEB2s. Enough will be
made for testing at multiple institutions as well as to populate a crate for larger scale testing, and integration with the LASP prototype.

Given the large number of items to be produced, the production and QA/QC phases are expected to take more than one year in all cases, as for the original ATLAS construction. Therefore, FEB2 production starts after a subset of the production quantity ASICs have been tested/qualified, and similarly installation can start before all FEB2s have been tested/qualified. The calibration electronics schedule, seen in Figure 12.5, follows a very similar timeline. The durations of all phases are based on experience acquired during ATLAS construction and the Phase-I upgrade. This schedule has approximately twelve months of float with respect to the planned installation periods.

The front-end crate low voltage power supply schedule, shown in Figure 12.6, starts with the work needed to establish that a solution with the main converters located in an accessible location will work. A test power board will be exposed to the expected radiation level and magnetic field, and the positioning constraints will be established. At the conclusion of these studies, option A will be selected if all results are positive, otherwise work will turn to implementing option B. The next step will be fabrication of a pre-prototype, and then a prototype to be used in integrated tests with the front-end boards. The LTDB power mezzanine will need to be replaced given the different incoming voltages. This development will start when the pre-prototype power supply work is sufficiently advanced.

For the HEC low voltage power supplies, the required DC/DC converters have been identified. Work will soon start on identifying a controller FPGA and designing the mechanics and cooling. When the ELMB++ becomes available, a prototype will be built.

12.3.3 Off-detector electronics

For the off-detector electronics, the custom hardware consists of the LASP main board, data processing unit and RTM, and this requires development of corresponding firmware. Development is starting now on a LASP test board, which will have both main board and data processing FPGAs, but will include many more test points than a production board would. Once debugged, a mini-series will be produced so that all contributing institutions have a board to work with for both hardware and firmware development. Hardware and firmware development are expected to progress in parallel, with integration of the different elements occurring at each stage. Prototypes will be used for integration with prototype front-end boards. Also here, transitions between the phases are marked by the Preliminary Design Review, Final Design Review, and Production Readiness Review milestones. These reviews will consider both hardware and firmware performance. Figure 12.7 shows the off-detector hardware electronics development and production schedule for the “main board” and data processing units. The RTM and firmware schedules are identical.
Figure 12.3: Front-end readout electronics development and production schedule: preamp/shaper and ADC ASICs.
Figure 12.4: Front-end readout electronics development and production schedule: optical links and front-end boards.
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<th>Expected End</th>
<th>Predecessors</th>
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</table>
### 3.1 LAr Front-End Electronics

#### 3.1.1 Front-end cooling

- **LVPS**

#### 3.1.2 Calibration System

- **HILO**

#### 3.1.3 Front-end signal processing

- **Pre-prototype**
  - May 24, 2015
  - May 27, 2015

- **Preliminary Design Review**
  - May 5, 2016

- **Final Design Review**
  - Feb 10, 2017

- **Production Complete**
  - May 1, 2018

#### 3.1.4 Front-end power

- **LVPS**

#### 3.1.5 Mechanics

- **Housing Design**
  - Nov 8, 2019

#### 3.1.6 Front-end electronics

- **Pre-production**
  - Apr 4, 2019

#### 3.1.7 LAr power supplies

- **Pre-production**
  - Apr 4, 2019

#### 3.1.8 TEPC power supplies

- **Pre-production**
  - Apr 4, 2019

#### 3.1.9 LAr power supplies

- **Pre-production**
  - Apr 4, 2019

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### Figure 12.6: Low voltage power supply development and production schedule.
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Figure 12.7: Off-detector electronics development and production schedule.
12.4 Risk management

The LAr Phase-II upgrade is a complex undertaking on the part of multiple institutions, which prone to internal and external uncertainties, the consequences of which are known as risk. This risk cannot be avoided but it must be managed. The overall purpose of risk management is to maximize the chances of success through formal procedures for the identification and analysis of risk, and for further treatment if warranted. The overall risk management strategy for the LAr Phase-II upgrade follows the ISO-31000 standard, *Risk management – Principles and guidelines*. The risk management process is an integral part of the LAr Phase-II project management, as it informs decision making at every stage.

The risk assessment process is organized by the risk manager. It begins with risk identification: a survey is conducted in which a comprehensive list of all sources of risk is assembled together with their possible impact upon the cost, schedule, scope, or performance. Information from the survey is held in a database called the risk register, which contains not only threats to the success of the project but also opportunities for lower cost, faster completion, or improved performance. The register is assembled by the risk manager in collaboration with the risk owners; i.e. those with the competence and authority to manage a particular risk. Generally these are the subproject managers.

The next step of risk assessment is risk analysis, in which an understanding of the risk is developed. The risk owner in consultation with the risk manager evaluates both the likelihood of a risk event occurring and the impact. Factors which affect both impact and likelihood are taken into account. The cost, schedule, scope, and performance risks are categorized as high, medium, low, or negligible according to well-defined criteria for cost and schedule, and somewhat more subjective criteria for scope and performance. Based on both the probability and the impact, an overall risk level is assigned to each risk.

Risk evaluation occurs once the level of each risk has been established. If existing controls are insufficient to treat the risks, further measures may be decided upon.

Risk treatment is the process by which risks are mitigated, responses to the risk are formulated and their effectiveness studied, and, if required, the best response to a risk event is selected and executed. This is a cyclical process. Mitigation consists of measures taken to reduce the probability that the risk materializes. These measures may consist, for example, of locating numerous vendors for a product to fulfil a specific need, undertaking multiple cycles of prototyping, or simultaneously considering alternate technologies. These steps are documented in the risk register.

A response to a risk actually occurring may consist of a fallback solution, but in some cases it may be necessary to accept the risk and its consequences to the scope, performance, and/or schedule. For example, a low rate of power supply failure could lead to dead regions in the detector and a need for more frequent interventions during LHC operations, which would be categorized as performance risk. When no effective response to a risk can be formulated, the risk register provides a transparent estimate of the impact. The risk may be accepted by
informed decision of management. When risks materialize, they are dealt with according to the anticipated response. If they fail to materialize, they are retired. The risk register is a living document, kept up to date as the project advances.

The risk management process is an iterative process involving continuous monitoring by the risk manager, periodic reporting to higher levels of management, re-evaluation of known risks and identification of emerging risks through communication and consultation with risk owners and other stakeholders.

The version of the risk register that is current with this document makes assumptions about the baseline design and treats alternate solutions as possible responses. It is foreseen to review this at regular intervals, i.e. during the quarterly ATLAS LAr weeks.

The LAr electronics upgrade replaces existing electronics, and builds on both the original ATLAS construction and the LAr Phase-I upgrades. The experience acquired leads to a significant reduction in risk. Nevertheless, many custom items need to be developed, making risks inevitable. In many cases, the occurrence of risks will lead to delays w.r.t. the baseline schedule. There is approximately one year of schedule float to absorb such delays.

The main risks, mitigation strategies and responses are:

- **Preamp/shaper**: the performance benchmarks may be very difficult to achieve with the architecture and technology options under consideration. To mitigate this risk, the work was already started, and two architectures and technologies are being evaluated. If needed, it is possible to fall back to a bipolar technology, for which proof of principle exists. There is also time for an additional prototyping round should the prototype not meet the specifications.

- **ADC**: also here the performance requirements are stringent, and may be difficult to achieve. Use of a commercial IP block for the ADC core is under investigation, and a COTS device has been identified as a potential fall-back solution.

- **Optical links**: the lpGBT and VL+ solutions may not be available when planned. Prototype front-end boards can be made with commercial devices as placeholders, and there is float in the schedule to absorb an additional year of delay.

- **FEB2**: aside from delayed availability of the ASICs, there may be system-level performance issues on FEB2, e.g. high coherent noise. To mitigate this, integration of the different ASICs will start as early as possible exploiting test chips. Late modifications may nevertheless be needed, using some of the available schedule float.

- **Calibration system**: the pulser ASIC may not meet the specifications, requiring a design change and an additional iteration to achieve the required performance. Similarly to FEB2, the calibration board may have system-level performance issues which require an additional iteration.
• **ELMB++**: if the ELMB++ is delayed, prototypes will be built without this functionality and it will need to be integrated at pre-production.

• **Front-end crate power system**: option A may not be feasible for multiple reasons; this is a new approach for LAr. Work with a test power board and interactions with technical coordination will establish option A’s feasibility early, leaving enough time to fall back on option B, which is very similar to the current devices.

• **HEC LVPS**: if the negative voltage regulators become unavailable, an alternative solution will need to be identified. To mitigate this, these regulators will be procured as soon as possible.

• **LASP integration**: LASP test board evaluation and integration tests may reveal the need for additional hardware changes, in particular a change of the selected processing FPGA model, and/or significantly more firmware development needs. To mitigate this, a mini-series of the test board will be produced to ensure all collaborating institutions have hardware available for development and testing. An additional prototyping round and/or additional firmware effort can be added, absorbing schedule float.

### 12.5 Deliverables and cost estimates

Table 12.1 shows the current core cost estimate broken down to level 4 in the WBS. The estimates are based on existing contracts (ASICs), quotes (ASIC packaging, FPGAs, fibres, etc.), and extrapolation from past costs (optical links, FEB2, ...). The firmware core cost is 0 CHF as this relies on labour only. There is no core cost included for the HV system since it is not planned to replace the existing HV system. The costs for maintenance and rolling replacement of hardware components are foreseen as part of the yearly LAr maintenance and operation budget.
Table 12.1: LAr Phase-II electronics upgrade core cost estimate.

<table>
<thead>
<tr>
<th>WBS Number</th>
<th>WBS Title</th>
<th>Core Cost Estimate [kCHF]</th>
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<td>LAr Front-End Electronics</td>
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<td>HEC Preshaper</td>
<td>0</td>
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<td>3.1.1.3</td>
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<td>Calibration System</td>
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<tr>
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<td>Pulser ASIC</td>
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<td>Calibration Board</td>
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<td>Optical Fibres</td>
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<td>Front-End Power Distribution System</td>
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<td>Front-End Cooling</td>
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<td>LAr Off-Detector Electronics</td>
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<td>Data Processing Unit</td>
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<td>3.2.3.2</td>
<td>ATCA Switches</td>
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<td>3.2.3.3</td>
<td>Server PCs</td>
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<td>3.2.3.4</td>
<td>Controller PCs</td>
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<td>3.2.4</td>
<td>Optical Fibres</td>
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<td></td>
<td><strong>Total</strong></td>
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</tr>
</tbody>
</table>
Acknowledgements

We thank CERN for the very successful operation of the LHC, as well as the support staff from our institutions without whom ATLAS could not be operated efficiently.

We acknowledge the support of ANPCyT, Argentina; YerPhI, Armenia; ARC, Australia; BMWFW and FWF, Austria; ANAS, Azerbaijan; STFC, Belarus; CNPq and FAPESP, Brazil; NSERC, NRC and CFI, Canada; CERN; CONICYT, Chile; CAS, MOST and NSFC, China; COLCIENCIAS, Colombia; MSMT CR, MPO CR and VSC CR, Czech Republic; DAE and DNSRC, Denmark; IN2P3-CNRS, CEA-DSM/IRFU, France; SRNSF, Georgia; BMBF, HGF, and MPG, Germany; GSRT, Greece; RGC, Hong Kong SAR, China; ISF, I-CORE and Benoziyo Center, Israel; INFN, Italy; MEXT and JSPS, Japan; CNRST, Morocco; NWO, Netherlands; RCN, Norway; MNSW and NCN, Poland; FCT, Portugal; MNE/IFA, Romania; MES of Russia and NRC KI, Russian Federation; JINR; MESTD, Serbia; MSSR, Slovakia; ARRS and MIZŠ, Slovenia; DST/NRF, South Africa; MINECO, Spain; SRC and Wallenberg Foundation, Sweden; SERI, SNSF and Cantons of Bern and Geneva, Switzerland; MOST, Taiwan; TAEK, Turkey; STFC, United Kingdom; DOE and NSF, United States of America. In addition, individual groups and members have received support from BCKDF, the Canada Council, CANARIE, CRC, Compute Canada, FQRNT, and the Ontario Innovation Trust, Canada; EPLANET, ERC, ERDF, FP7, Horizon 2020 and Marie Sklodowska-Curie Actions, European Union; Investissements d’Avenir Labex and Idex, ANR, Région Auvergne and Fondation Partager le Savoir, France; DFG and AvH Foundation, Germany; Herakleitos, Thales and Aristeia programmes co-financed by EU-ESF and the Greek NSRF; BRF, GIF and Minerva, Israel; BRF, Norway; CERCA Programme Generalitat de Catalunya, Generalitat Valenciana, Spain; the Royal Society and Leverhulme Trust, United Kingdom.

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A Mapping of FEB2 boards to LASP units

The baseline mapping of the FEB2 boards to the LASP is assuming that each processing FPGA will receive digitized signals from 512 LAr cells with two gains, which corresponds to four FEB2 modules. Tables A.1, A.2, A.3, A.4, and A.5 show a possible readout scheme of the EMB, EMEC, HEC and FCal regions.

The option of a digital Super Cell readout for the HEC requires a concentration of HEC data in the range $|\eta| > 2.7$ and EMEC data in $|\eta| > 2.4$ into one data stream to the gFEX trigger modules. If four FEB2 boards can be handled by one FPGA, this stream can be prepared with data from two LASP FPGAs (LASP ID 1 in HEC/EMEC half-crate and LASP ID 1 in EMEC-special half-crate).

Table A.1: Tentative mapping of FEB2 boards to LASP units in the EMB for one detector side. The FEB2 slots of the front-end half-crates are listed together with the detector layer and pseudorapidity region (PS = presampler, F = front layer, M = middle layer, B = back layer). The LASP FPGAs cover up to four FEB2 boards, each with the number of cells as given in the table.

<table>
<thead>
<tr>
<th>Slot</th>
<th>A</th>
<th>B</th>
<th>Cells</th>
<th>LASP ID</th>
<th>LASPs per HFEC</th>
<th>No. of LASPs</th>
<th>Cells per LASP</th>
<th>Cell Sum</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>PS 0.8-1.5</td>
<td>PS 0.0-0.8</td>
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<td>0.5</td>
<td>16</td>
<td>496</td>
<td>7 936</td>
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<td>F 0.0-0.2</td>
<td>126</td>
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<td>512</td>
<td>16 384</td>
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</tr>
<tr>
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Table A.2: Tentative mapping of FEB2 boards to LASP units in the EMEC for one detector side. The FEB2 slots of the front-end half-crates are listed together with the detector layer and pseudorapidity region (PS = presampler, F = front layer, M = middle layer, B = back layer). The LASP FPGAs cover up to four FEB2 boards, each with the number of cells as given in the table.

<table>
<thead>
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<tr>
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</tbody>
</table>
Table A.3: Tentative mapping of FEB2 boards to LASP units in the EMEC-special and HEC regions for one detector side. The FEB2 slots of the front-end half-crates are listed together with the detector layer and pseudorapidity region (PS = presampler, F = front layer, M = middle layer, B = back layer). The LASP FPGAs cover up to four FEB2 boards, each with the number of cells as given in the table.

<table>
<thead>
<tr>
<th>Slot</th>
<th>A</th>
<th>B</th>
<th>Cells</th>
<th>LASP ID</th>
<th>LASPs per HFEC</th>
<th>No. of LASPs</th>
<th>Cells per LASP</th>
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Table A.4: Tentative mapping of FEB2 boards to LASP units in the EMEC-special/HEC region for one detector side. The FEB2 slots of the front-end half-crates are listed together with the detector layer and pseudorapidity region (PS = presampler, F = front layer, M = middle layer, B = back layer). The LASP FPGAs cover up to four FEB2 boards, each with the number of cells as given in the table.

<table>
<thead>
<tr>
<th>Slot</th>
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<th>Cells</th>
<th>LASP ID</th>
<th>Laspers per HFEC</th>
<th>No. of Laspers</th>
<th>Cells per LASP</th>
<th>Cell Sum</th>
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<td>EMEC 2.5-3.2</td>
<td>EMEC 2.5-3.2</td>
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<td>4</td>
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<td>1920</td>
</tr>
<tr>
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<td>HEC 1</td>
<td>HEC 1</td>
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<tr>
<td>6</td>
<td>HEC 2</td>
<td>HEC 2</td>
<td>128</td>
<td>2</td>
<td>1</td>
<td>4</td>
<td>512</td>
<td>2048</td>
</tr>
<tr>
<td>7</td>
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<td>HEC 3</td>
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<td>4</td>
<td>512</td>
<td>2048</td>
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</tbody>
</table>

Table A.5: Tentative mapping of FEB2 boards to LASP units in the FCal region for one detector side. The FEB2 slots of the front-end half-crates are listed together with the detector layer and region identifier (F1-F3 = FCal module 1-3). The LASP FPGAs cover up to four FEB2 boards, each with the number of cells as given in the table.

<table>
<thead>
<tr>
<th>Slot</th>
<th>A</th>
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<th>Cells</th>
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Appendix A: Mapping of FEB2 boards to LASP units
The low voltage in each of the three supply voltages for the HEC PSB is supplied through 2 m of warm copper cable and 11 to 17 m long cold copper cable plus feed-through and other connectors. The total resistance is of the order of 1 Ω. The supply voltages need therefore to account for these losses:

- **in cold:**
  - 7.2 V: loss in cabling $\sim$ 0.20 to 0.40 V
  - 3.1 V: loss in cabling $\sim$ 0.16 to 0.22 V
  - −1.5 V: loss in cabling $\sim$ 0.04 to 0.07 V

- **in warm:**
  - 7.2 V: loss in cabling $\sim$ 0.35 to 0.70 V
  - 3.1 V: loss in cabling $\sim$ 0.14 to 0.20 V
  - −1.5 V: loss in cabling $\sim$ 0.07 to 0.12 V

the voltages should be settable to 5% accuracy. Once fixed the voltage line regulation should stay accurate to 1%, the over-current protection per channel should be set to:

- 7.2 V: 1.0 A
- 3.1 V: 0.6 A
- −1.5 V: 0.4 A

the 3 voltages are supplied each to 5 different types of PSBs in 8 wedges. Each wedge has exactly one PSB board of each type. The summed maximal currents for all 40 PSB boards for one LVPS are:

- **in cold:**
  - 7.2 V: 13.3 A
  - 3.1 V: 7.9 A
  - −1.5 V: 2.4 A

- **in warm:**
Taking the larger of the warm/cold in each voltage and adding 10% for irradiation induced increased currents in the PSB and 10% for irradiation induced currents in the LVPS and 1 A in the 7.2 V channel for digital electronics the following maximal currents are expected:

- 7.2 V: 29.8 A
- 3.1 V: 9.5 A
- −1.5 V: 5.2 A
C Radiation maps

This appendix contains radiation maps obtained with simulation for an integrated luminosity of 4 000 fb$^{-1}$. The plots show the displacement damage in silicon (Figure C.1), the total ionizing dose (Figure C.2), and the total fluence of hadrons (Figure C.3). The minimum-bias $pp$ events are simulated with Pythia8 at 14 TeV centre of mass energy assuming an inelastic cross section of 80 mb. Particle tracking and interactions with material are simulated with the GEANT3/GCALOR code using the latest geometry description of the Phase-II ATLAS detector. The geometry model is symmetric in azimuth and about $z = 0$. 
Figure C.1: Displacement damage in silicon for an integrated luminosity of 4000 fb$^{-1}$, expressed as the equivalent fluence of 1 MeV neutrons.
Figure C.2: Total ionizing dose in Gy/400 fb\(^{-1}\) in the tracking and calorimeter regions of the Phase-II ATLAS detector.
Figure C.3: Total fluence of hadrons with $E > 20$ MeV per cm$^2$ for an integrated luminosity of 4,000 fb$^{-1}$. The integrated fluence can be converted to the flux per second at a peak luminosity of $5 \times 10^3$ cm$^{-2}$s$^{-1}$ by dividing by a factor of $8 \times 10^7$. 

Appendix C: Radiation maps
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