Upgrade of the ATLAS Monitored Drift Tube (MDT) Electronics for the HL-LHC

**Background**

- The ATLAS muon spectrometer is composed of precision tracking and trigger chambers.
- Precision measurements of the muon track coordinates are provided by three stations of Monitored Drift Tube (MDT) chambers up to ||z|<2.5.
- Cathode strip chambers (CSC) with higher granularity are used in the innermost station covering 2.0<||z|<2.7.
- Resistive plate chambers (RPC) located in the barrel region (||z|<1.05) and thin gap chambers (TGC) in the endcap region (1.55<||z|<2.4) are used to provide trigger information.

**MDT detector**

- The ATLAS muon spectrometer is mainly used for muon triggering, identification and momentum measurement.
- Provides a standalone momentum measurement (10% at 1 TeV), mainly by the monitored drift tube (MDT) chambers.
- 1150 chambers with 35k tubes covering an area of 5500 m².
- Each tube has an inside diameter of 29.97 mm and is filled with a mixture of Ar/CO₂ (53/47) at 3 bar.
- A 50 µm gold-plated tungsten wire is positioned at the center of each tube.
- A high voltage of 3.08 kV is imposed across the tube wall and the central wire.
- Ionization created by the passage of a muon track can take up to 750 ns to reach the anode wire.

**New MDT Frontend**

- One ASG has 8 channel covering 8 raw drift signals.
- One TDC has 24 channels covering 3 ASD chips.
- One front-end (mezzanine) board has one TDC three ASGs on it to cover 24 raw drift signals.
- One Chamber Service Module (CSM) can cover up to 18 mezzanine boards.
- CSM broadcasts the Timing, Trigger and Control (TTC) signals to the TDCs.
- In CSM, the data are formatted, stored in a large de-randomizing buffer, and sent via an optical link to the MDT readout driver modules (MRD).

**Consideration of MDT Frontend Electronics in Phase II**

- MDTE FE electronics needs to cope with new proposed ATLAS DAQ scheme (1 MHz L0 trigger rate with a latency of 15 ns).
- The max rate current MDT readout electronics can handle: 46 kHz tube.
- 160 buffers in the current TDC chips are too small to store all hits for such a long latency time.
- MDT will be used at L0 to further sharpen the L0 trigger turn-on curve.
- Radiation tolerant.
- Proposed MDT electronics system:
  - Triggerless at FE and trigger matching performed at USA 15.

**Amplifier Shaper-Discriminator (ASD)**

- Similar schematic as the present ASD (550 nm Agilent technology) but using the GF 130 nm CMOS process.
- Charge Sensing Preamplifier (CSP): DA1→DA2→DA3 (three shaping stages) → discriminator
- The silicon area is 2.26 x 3.36 x 7.6 mm²

**New ASD**

- Drift time spectrum measured with the new ASD vs. strips in excellent agreement with drift time spectrum measured with ATLAS ASD chip.

**A New TDC Design**

- 3 is a demonstration prototype, with only triggerless mode.
- TDC architecture w.o. i.e. the timing resolution:
  - Multiple clock phases, interpolation: 0.320 MHz
  - 4 phases of 320 MHz ⇒ 0.125 ns to 0.78 ns, LSB
- Main components:
  - Generation of multiple clock phases: PLL (CERN)
  - Time Digitization: TDC channels (42 MHz, dual edges)
  - Time processing/calibration, output serial interface (TDC logic part)

**Chamber Service Module (CSM)**

- One Chamber Service Module (CSM) must cover up to 18 new mezzanine boards.
- Each new mezzanine board has two 320 MHz data line.
- 2 CSM sends out data to USA 15 using 3 X 4 Gbps fibers.
- CSM gets clock, configuration information using a fiber.
- CSM sends out the mezzanine boards status like temperature, power supply using a fiber.

**Motivation for a new TDC:**

- Previous AMT is no longer available for production.
- Out data band with not enough for high rate.
- Issues found with the AMT chip.
- Develop the TDC ASIC for the MDT phase II upgrade.
- Comparable timing performance (Tubes unchanged).
- Additional features: Triggerless mode + Trigger mode.

**FPGA-based CSM (a)**

- FPGA-based Advantages
  - Flexibility
  - Uniform hardware design
  - Can easily handle migration from Phase I triggerless to Phase II triggerless
  - Ticks with old CERN or can be replaced in Phase II

- FPGA-based Design Complications
  - Uncertainty about FPGA SEU performance in Phase II
  - Maintenance needed for firmware

**FPGA-based CSM (b)**

- GBT-based Advantages
  - Low cost, low power
  - Radiation hard ASIC’s from CERN
  - No firmware design maintenance

- Design Complications
  - Functionality fixed by GBT chip
  - Small additional chip needed for JTAG distribution

**Custom Layout Part**

- TDC Logic Part

- 0 ns delay: RAMS ~36 ps

- 4 ns delay: RAMS ~119 ps