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Final Design Review of Deliverable D4.3 (TSV in 65 nm)

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Abstract:
The compatibility of the large-scale 65 nm CMOS integrated circuit RD53A with the process of fabricating Through-Silicon Vias was reviewed with the two TSV technology vendors that were selected in the first stage of the project (MS23). CMOS wafers from the RD53A engineering run in 65 nm will be available by the end of 2017, and the implementation of TSVs and of the relevant process steps in selected wafers will be discussed in WP4 after a brief testing phase.
AIDA-2020 Consortium, 2017
For more information on AIDA-2020, its partners and contributors please see www.cern.ch/AIDA2020

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Executive summary

Through-Silicon Vias are a key ingredient of 3D integration of silicon pixel sensors with CMOS readout integrated circuits. In the first stage of the project, two technologies have been selected for the fabrication of TSV in 65 nm pixel readout integrated circuits based on promising results with the previous generation of front-end chips in 130 nm CMOS. The possibility of fabricating TSVs in the large scale 65 nm CMOS pixel chip called RD53A was evaluated with two technology vendors. It was verified that the chip was implemented according to design rules compatible with TSV processing from the backside of the CMOS substrate. After chip delivery and testing, the implementation of the TSV processing steps in selected 65 nm CMOS wafers will be discussed in WP4.

1. INTRODUCTION

The main goal of Task 4.4 is to accomplish the interconnection of the 65 nm CMOS readout chips developed in Task 4.2 with the silicon pixel sensors that will be provided by WP6 and WP7. Moreover, this task plans to accomplish a connection to the backside of the 65 nm CMOS chips by using through-silicon vias (TSVs) across the substrate. The goal is to qualify a technology that makes it possible to achieve a connection of the chip periphery to the backside, where a metal redistribution layer can be used to fabricate bump bonding pads. The possibility of performing TSV processing steps on the large-scale pixel readout chip RD53A was reviewed with the two technology vendors selected in a previous stage of the project (MS23).

2. TSV COMPATIBILITY OF THE 65 NM CMOS PIXEL READOUT CHIP RD53A

An important goal of WP4 is to demonstrate the feasibility of TSV processing in 65 nm CMOS pixel readout chips. The adoption of 3D integration technologies in the design of pixel detector systems, will bring important advantages in terms of pixel form factor, readout speed, reduction of dead areas and material. In WP4, it is planned to test TSV processing on the RD53A 65 nm CMOS chip developed in Task 4.2. Two technologies for TSV fabrication, developed at CEA-LETI and Fraunhofer IZM, were previously selected after extensive testing with 130 nm chips. The tests were performed as part of previous AIDA WP3 activities.

The RD53 readout chip was submitted at the end of August 2017 in a 65 nm CMOS engineering run, together with several other integrated circuits. Wafers from this run are expected to be delivered at the end of November 2017. The RD53A chip was designed to demonstrate in a large format integrated circuit the suitability of the 65 nm CMOS technology for the ATLAS and CMS pixel upgrades at the High Luminosity LHC. This chip was developed following the design rules for TSVs in its peripheral regions. More specifically, the bonding pads in RD53A are compatible with a backside etching process available in TSV fabrication, such as the one already successfully tested with 130 nm FE-I4 CMOS wafers, as shown in Fig. 1. In a CMOS process such as the 65 nm one, these pads have all metal layers from the first one, M1, to the actual aluminium pad, as shown in Fig. 2. In RD53A, M1 and M2 were removed to reduce parasitic capacitance and optimize the performance of high-speed drivers.

The RD53A bond pad structure was submitted to IZM and CEA-LETI for an internal review. According to non-disclosure policies, it was not possible to discuss technology details of the 65 nm and the TSV processes in an open session. The result of these internal reviews is that no...
problems are foreseen for both processes, as far as the adopted design rules are concerned. As a result of the review, and according to WP4 plans, it is possible to proceed with TSV fabrication on the 65 nm CMOS wafers once they are available and the chips are successfully tested.

There are still important challenges that remain to be tackled, such as handling large wafers, thinning them down to about 100 µm, and flip-chipping them for the interconnection to sensors. Further support to solve these issues is expected from the PoC project (funded by WP2), *Advanced Through Silicon Vias for Pixel Detectors* (led by the University of Bonn), which is planning to study various implementation aspects related to TSV processing in 65 nm CMOS wafers.

It is also important to mention that other projects (such as PIXFEL, funded by INFN) are also planning to have TSVs etched in smaller chips in the same run. This will help in sharing experience and results once chips with TSVs are tested.

![Fig. 1: TSV etched from the backside of the substrate in FE-I4 chip (IZM process).](image)

**Fig. 1:** TSV etched from the backside of the substrate in FE-I4 chip (IZM process).

![Fig. 2: Structure of bump bonding pads and of relevant metal levels in an advanced CMOS process.](image)

**Fig. 2:** Structure of bump bonding pads and of relevant metal levels in an advanced CMOS process.

### 3. CONCLUSION

Following the results of a closed review with the two selected technology vendors, the RD53A chip was validated with respect to its compatibility with TSV processing in the periphery of the chip. The 65 nm CMOS wafers are expected to be delivered by the foundry in November 2017. After extensive testing, WP4 partners will discuss how to proceed with TSV fabrication in selected wafers.