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Prototyping of petalets for the Phase-II upgrade of the silicon strip tracking detector of the ATLAS experiment

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Prototyping of petalets for the Phase-II upgrade of the silicon strip tracking detector of the ATLAS experiment


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Abstract: In the high luminosity era of the Large Hadron Collider, the instantaneous luminosity is expected to reach unprecedented values, resulting in about 200 proton-proton interactions in a typical bunch crossing. To cope with the resultant increase in occupancy, bandwidth and radiation damage, the ATLAS Inner Detector will be replaced by an all-silicon system, the Inner Tracker (ITk). The ITk consists of a silicon pixel and a strip detector and exploits the concept of modularity. Prototyping and testing of various strip detector components has been carried out. This paper presents the developments and results obtained with reduced-size structures equivalent to those foreseen to be used in the forward region of the silicon strip detector. Referred to as petalets, these structures are built around a composite sandwich with embedded cooling pipes and electrical tapes for routing the signals and power. Detector modules built using electronic flex boards and silicon strip sensors are glued on both the front and back side surfaces of the carbon structure. Details are given on the assembly, testing and evaluation of several petalets. Measurement results of both mechanical and electrical quantities are shown. Moreover, an outlook is given for improved prototyping plans for large structures.

Keywords: Particle tracking detectors (Solid-state detectors); Si microstrip and pad detectors; Solid state detectors; Performance of High Energy Physics Detectors

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1 Introduction

For the ATLAS experiment, a new, all-silicon tracker is foreseen at the High-Luminosity LHC (HL-LHC). It will consist of a pixel and strip detector [1] and is expected to be installed in 2024. The strip tracking detector will feature five silicon sensor layers in the central region and six in the forward region. An important concept of the upgrade tracker is modularity, allowing for faster final assembly and staged pre-assembly and pre-testing. For the central region so-called staves will be built and details of the prototyping can be found in ref. [2]. The basic building block used in the forward region is referred to as petal. Petals are double-sided objects in trapezoid-shape built from a carbon-fibre sandwich structure, the core, with six ring sectors of silicon sensor modules glued onto both sides of the core. Figure 1 illustrates the geometry of a petal, including modules, silicon sensors (in blue) with readout electronics (in green and brown) glued on top. The end-cap modules are designed to cover the whole petal region in R-φ with two layers of castellated, slightly overlapping petals. The petal design is optimized for silicon sensors coming from 6” wafers. At higher R, in the regions in which a single silicon crystal coming from a 6” wafer cannot cover the
whole area in φ, sensors are split in two and placed next to each other. In contrast, a single module provides coverage in the azimuthal direction for lower values of R. In this region the modules employ the shortest strip sections to cope with the highest occupancy regions of the strip end-caps, thus requiring two readout boards per sensor. In addition, power boards (in orange in figure 1) and the readout board of the modules and petal (in light green) are sketched. Titanium cooling pipes run inside the core and petal locators can be seen next to the outer ring of the petal, which compose the interface between the petals and the global end-cap structure. A multi-layer flexible circuit is assembled at the core surfaces (the so-called bus tape, in yellow), for the routing of power lines and electrical signals along the petal.

In total 384 petals with 6,912 modules will be produced. One disk of an end-cap will be assembled out of 32 petals. A reduced-size version of petals, called petalets have been developed to kick-off the prototyping of large structures with multiple silicon detector modules. A detailed R&D programme covering design, assembly and evaluation of these prototypes has been conducted. Two different readout architectures have been investigated to optimize the assembly and readout of full-size petals [3–5]. The main results of this study, the assembly and evaluation of fully assembled petalets are reviewed in this paper, including a comprehensive comparison between the two readout options investigated.

Figure 1. Schematic representation of a petal consisting of a carbon-fibre core with cooling pipes inside. One side is visible with silicon-detector modules glued on top. The modules house the silicon sensor, readout-board and a powering board. Cooling pipe connectors and the readout board are visible at the side of the petal. The layout is for silicon sensors manufactured in 6” wafer technology and ASICs produced in a 130 nm CMOS process.
2 Layout and components of petalets

2.1 Petalet layout

The petalets are smaller-size prototypes and consist of similar components to the ones which are used in petals. Their overall size is $17 \times 19 \text{cm}^2$ and they are about 6 mm thick. Instead of nine sensors like on a petal, three silicon sensors are glued on each side of a petalet core with their respective readout electronics, constituting fully functional silicon microstrip modules. A schematic sketch with core dimensions in millimeters is given in figure 2. It sketches the top surface of the carbon-fibre core attached with a bigger lower sensor and two smaller upper sensors having flex printed-circuit-boards, called hybrids, glued on top. The hybrids have readout chips designed in 250 nm CMOS process glued on top which were the version available at the time of the protoyping phase. The ASICs have 128 analogue channels with binary output allowing to process signals from the silicon strip sensors in a binary read-out architecture. The readout channels and silicon strips are connected by wire-bonds. Titanium cooling pipes are placed inside the carbon-fibre core and a thin (150 $\mu$m) multi-layer flexible circuit tape for electrical routing is glued on top of the core surfaces. The connectors of the pipes can be seen sticking out the core. Additional boards required for the electrical readout of the modules are glued on the tape. With these double-sided support structures the routing between front and back side as well as the handling and assembly can be prototyped.

![Diagram of petalet layout](figure2.png)

**Figure 2.** Schematic drawing of a petalet consisting of a carbon-fibre core with cooling pipes inside. One side is visible with two upper sensors and a lower sensor glued on top. For the upper module the hybrid is not shown but lines indicate the placement and wire-bond area. For the lower module the hybrid is drawn on top. Dimensions are shown in millimeters. Reproduced from [4]. CC BY 3.0.

During the prototyping of the petalets, two different readout architectures have been under investigation. They are compared aiming for low complexity and high performance. One readout scheme deploys connections and routing of data, clock, trigger, timing, and control signals at the right-hand side of the module, while powering is routed on the left-hand side. This scheme is called
split readout scheme, and a sketch of it, indicating the routing, can be seen in figure 3. The second scheme routes data, trigger, control, and powering to one side of the module. This one is called common readout scheme and is sketched in figure 4. A single piece of bus tape covers both the front and back side of the petalet, providing power and data lines for both sides. The bus on the left-hand side connects one front side and two back side modules, while the one on the right-hand side connects one back side and two front side modules. Six hybrids are used to read out six sensors. Specific tooling has been developed for all dedicated construction and assembly steps for both layouts.

Figure 3. Sketch of one side of the split readout scheme layout. Two modules, each consisting of one hybrid mounted on one (lower module) or two (upper module) sensors, respectively, are placed and read out on one bus tape on each side of a petalet. Each hybrid hosts 12 chips. The power is routed on the left-hand side whereas data, clock, timing, trigger, and control (TTC) signals are routed on the right-hand side. Reproduced from [4]. CC BY 3.0.

2.2 Modules

Silicon sensor modules have been developed within the petalet project. The modules consist of a flex printed circuit board with ASICs, the hybrids glued on top of one or two silicon sensors. A detailed description is given in refs. [4, 6]. The ASICs are produced in 250 nm CMOS process and specifications are given in refs. [7, 8]. In the future, they will be produced in a 130 nm CMOS process, with 256 readout channels per ASIC, which leads to a reduced number of ASICs per silicon module for petals as opposed to the petalets [9]. The sensors are made of p-type bulk material with p-stop insulation [3, 10]. Three sensor geometries have been designed for placement at the lower, upper left and upper right position on the petalet. In addition, two sensor types are available, a set with embedded pitch adapters to reduce the wire-bonding angle and a set with standard pitch adapters on each strip. The second metal layer of the embedded pad sensors leads to increased noise values depending on the length and geometry of the second metal layer traces [11, 12]. This effect has to be taken into account when comparing the performance of petalets with modules built either from standard sensors or from embedded ones.

Both readout schemes require different hybrid layouts. They vary in both the direction of data and power readout as described before and the amount of chips per hybrid, either six or twelve. In addition, the upper modules of the split readout scheme have one hybrid glued onto two silicon
Figure 4. Sketch of the two sides of the common readout scheme layout. Six hybrids are used to read out six sensors. They host either six or twelve chips. A single piece of bus tape covers both the front and back side of the petalet, providing power and data lines for both sides. The bus on the left-hand side connects one front side and two back side modules, while the bus on the right-hand side connects one back side and two front side modules. Reproduced from [4]. CC BY 3.0.

sensors. For the common readout scheme, individual hybrids are glued on the upper left and upper right sensors, resulting in total in three modules per petalet side. Details on the hybrids for the forward region are given in ref. [4, 6]. In these papers also the assembly and testing of modules in test frames is described. In total about 40 modules have been built and thoroughly tested. The test results show a good performance and low average input noise values corresponding to an equivalent noise charge of $380 \pm 20$ electrons for hybrids and $520–750$ electrons for modules depending on the sensor quality.

2.3 Petalet cores

The petalet core structure mimics the envisioned design for the full-length support structures, the petals. It consists of a flat, lightweight carbon-fiber based structure with embedded titanium cooling pipes. The choices of materials and adhesives aimed for the best compromise between thermal and mechanical performances, also after irradiation, and a minimum material budget. The surfaces of the structure are constituted by three layers of carbon fiber reinforced polymer (CFRP), co-cured together with a certain fiber orientation among them (0-90-0 degrees, from top to bottom). This fiber orientation was found to provide the optimal thermal and mechanical properties of the petal structures. The titanium cooling pipe is bent to an U-shape and has an outer diameter of 2.275 mm, with 140 $\mu$m wall thickness. Stainless steel fittings are brazed into the pipe inlet and outlet. Inside
the core structure, the pipe is surrounded by thermally conductive, carbon fiber-based foam of very low density (0.23 g/cm$^3$), from Allcomp Inc. [13]. The pipe-foam structure is glued on the back side of the CFRP face-sheets with Boron Nitride-loaded Hysol EA9396 epoxy from Henkel Inc. [14]. The rest of the structural material consists of Kevlar N636 Para-Aramid fiber honeycomb from DuPont Inc. [15]. The honeycomb is also glued down to the top and bottom CFRP face-sheets with EA9363 epoxy. The core structure is closed sideways with closeout elements of different shapes, machined in thermoplastic polymer (PEEK) and glued to the face-sheets with EA9363. An electrical break, required to isolate electrically the petals from noise sources from the surrounding environment, will be included in petal pipes but is not yet in the petalet cores. Custom mechanical tools were developed for the precise assembly of the petalet cores. Figure 5 shows a photo of the internal structure and figure 6 a complete core with the top face-sheet attached. The total thickness of the petalet cores, including the bus tape (described in section 2.4) on top, is 5.4 mm. Its mass is about 77 g. Nine petalet cores have been manufactured for the petalet project.

Figure 5. Petalet core on a mounting jig without the top CFRP skin.

Figure 6. Complete core structure of the petalets.
2.4 Bus tape

The bus tape is a printed circuit on a flexible substrate. Its main purpose is to route power, command and data lines between the front-end electronics and the outer data acquisition system. The bus tape is aimed for low material budget while giving good thermal path between the hottest elements (front-end electronics and sensors when irradiated) and the cooling pipes that run inside the carbon fibre core. Bus tapes are designed to be manufactured in thin polyimide at ELGOLINE d.o.o. [16]. Furthermore, bus tape designs for the petalet minimise the number of polyimide layers to one in the region under the sensors and a maximum of two metal layers (copper traces under a metal shield) is used. For simplicity and ease of manufacturing, vias are avoided. Connection to the bottom metal layer is done with openings and wirebonding. A sketch of the stack-up of the bus tapes can be seen in figure 7. In the first prototypes, aluminium was used as a conductor in the ground-shield layer to minimize the scattering material. However it was abandoned due to the mismatch of the coefficient of thermal expansion with the copper layers, leading to deformations in the tape during manufacture. Later versions employ 12 $\mu$m copper, 25 $\mu$m polyimide laminate, and 25 $\mu$m glue joining layers. Openings in polyimide and glue are done with a laser cutter. Wire-bondable electrodeposited gold (ENIG) is covering the exposed areas of copper traces. A 12.5 $\mu$m polyimide coverlayer with 25 $\mu$m glue protects the upper surface of the tape. Power lines to the front-end electronics and sensors consist of two power supply lines (about 10 V), two control lines for power supply of the DC-DC converter (more in section 2.5) and one pair of high voltage line (HV) and its return (HVret) per sensor. Widths of power lines and separation of HV lines are designed following IPC-2221 standards [17]. Command and control lines require three differential pairs (COM, BCO, L1R). A DATA differential pair and two lines to read a temperature sensor are connected to each hybrid. As the carbon-fibre core has low resistivity, an opening is designed in the bus tape in order to ground the core. The bus tape plays an important role in the evaluation of the two readout options for the forward region, not only electrically but also mechanically. Thus, two bus tape designs are implemented and photographs of both are shown in figure 8. On the left photograph, the bus tape for the common readout scheme is displayed. In this option, each sensor has its own hybrid. The design covers both petalet sides and is folded around the upper part of a core. The photograph on the right presents the bus tape for the split readout scheme. Two equal bus tapes, one on each side of the petalet core, are needed for this readout scheme. Soldering pads for connectors are visible on both tapes.

Figure 7. Sketch of the stack-up of the bus tapes.
2.5 Electrical boards

For powering and data readout, the petalets are connected to the so-called End-of-petalet boards. Two types of these boards have been developed for the two readout architectures. The boards filter and multiply data to the HSIO readout board [18] which is connected to a computer with data acquisition software. In addition, two more types of boards are glued onto the petalet. One buffer control chip (BCC) per module, mounted on a printed circuit board, is used as an interface board to the ASICs on the hybrid and fosters signal distribution. By this the hybrids are addressed and the number of required signal lines is reduced. It also handles trigger, timing, and command signals. The second type of boards, made of low noise and low mass DC-DC converters, allows powering of the hybrids. The converters provide 2.5 V to the front-end chips from the 10 V supply voltage. Each converter uses a toroidal coil inductor, which needs to be shielded to reduce the emitted electromagnetic noise. DC-DC powering is the baseline for strip modules in the upgrade tracker. Both boards can be seen assembled on a petalet in figure 14.

3 Assembly of petalets

3.1 Assembly and testing of bus tape and core

Once the cores are assembled, the bus tape with 150 $\mu$m thickness is glued onto the top side of both CFRP face-sheets with a thin layer of EA9363 epoxy. Figure 9 shows a core with bus tape for the common readout scheme. In the baseline petal layout, the bus tapes are co-cured together with the CFRP face-sheets and no additional glue layer is required. The planarity of cores including bus tapes is measured after curing and figure 10 shows the result of a planarity measurement of a representative core structure performed with a contact probe mounted on a coordinate measuring.
machine (CMM). The measurements were divided in sectors, since the bus tapes have different thicknesses over the core surface. In the region below the silicon sensors, the average measured thickness is 5.39±0.05 mm. The finished cores exhibit a flatness tolerance equal to 37±12 µm. In total six cores were successfully assembled with bus tapes. In a next step, connectors are soldered on bus tapes and fully functional modules are mounted after cleaning the surface with alcohol.

**Figure 9.** Test assembly of a dummy core with bus tape for the common readout scheme, glued and bent over the upper part of the core. On the right-hand side a top view of the bent area is visible.

**Figure 10.** Results of a planarity measurement of a representative petalet core. Surface is divided in five different sectors, according to the different thicknesses of the bus tape: silicon area (center), top area, lateral areas, and bottom area. Values are given in mm.
3.2 Loading of modules onto cores

A custom set of tools was developed for the precise placement of the petalet modules onto the petalet cores. A set of vacuum plates and vacuum-holding pick-up tools is used to pick up the silicon modules once they have been disconnected from their test frames. The modules are located on a vacuum plate integrated with an X-Y-stage driven by micrometer screws. Pick-up occurs on the ASICs surface, preserving enough clearance to the wire-bonds. Fiducials located on the silicon sensors allow for precise pick-up of the modules onto the petalet core. The petalet core is placed on a custom precision frame, to which the pick-up tools holding the modules are then mechanically locked. The modules are glued down onto the petalet cores with SE4445 thermally conductive and electrically insulating silicone gel from Dow Corning Inc. [19]. The high voltage (HV) contact of the sensor backplane to the traces on the bus tapes is attained with electrically conductive TRA-DUCT 2902 epoxy from Henkel Inc. [14]. The glue is dispensed on the core surface by means of a custom glue stencil template. The stencil is designed to maximize the SE4445 glue spread and hence the thermal contact between the petalet core and the strips modules. The glue pattern on the core surface can be seen in figure 11. The thickness of the glue is determined by 150 $\mu$m diameter nylon wires and with adjusted micrometer screws on the pick-up tools. Once the modules are glued, the DC-DC converters and BCC boards are also assembled onto the petalet core with thermally conductive glue. Figures 11, 12 and 13 show different stages of a petalet undergoing the gluing of the silicon modules with the custom mechanical tools. Figure 12 shows the module pick-up and figure 13 the final placement onto the core with custom pick-up tools. Both upper and lower modules are placed on the core for curing. The clearances between sensors are 500 $\mu$m. Figure 14 shows one side of a fully assembled petalet in the split readout scheme. Before electrical testing of the petalets, hybrid and bus tape pads need to be connected via wire-bonds. All cores with bus tapes are assembled to five petalets in the split readout scheme and one petalet in the common readout scheme.

Figure 11. Glue pattern on core surface with a split readout scheme bus tape before module assembly.
4 Testing of petalets

A variety of tests were conducted with the petalets. Both petalets with standard and with embedded modules and petalets of both readout schemes were evaluated as presented in the following sections. The results are compared between different types of petalets. Moreover, electrical test results of modules are compared before and after gluing on the core as well as measurements were performed at different operating temperatures.
Figure 14. Complete petalet including DC-DC converter and BCC boards. Two upper and one lower module of the split readout scheme are glued onto the bus tape.

4.1 Procedure for electrical tests

The petalet under test is connected using custom-designed adapter boards and cables to low voltage and high voltage power supplies. The connection of data lines is made with a flat-ribbon cable to an HSIO readout board [18] that provides the interface to the computer. For petalets in the split readout scheme both sides are connected individually to the adapter boards, while for petalets in the common readout scheme the bus tape connects both sides to one adapter board and cabling.

A first test is the verification of the connectivity of all ASICs of the modules by requesting their addresses. Afterwards, the important quantities like noise behavior and signal readout of the modules are tested with the HSIO test board and specific data acquisition software. At the beginning, the delays are correctly set. Then every channel of the ASICs is evaluated using threshold scans in the binary readout architecture. In a threshold scan a number of hits at a fixed injected charge versus the discriminator threshold voltage is recorded. By varying the threshold and repeating the measurements 200 times, the occupancy curve can be obtained, plotting the number of hits above threshold versus threshold value. Due to noise contributions this curve is widened by a Gaussian distribution, resulting in the s-curve. The output noise is the standard deviation extracted from the width of the s-curve. The 50% occupancy point of the s-curve for various values of injected charges leads to the response curve distribution. Its derivative corresponds to the gain of the channel. By dividing output noise and gain, the input noise at the discriminator can be calculated. It is given in the measurement results for an injected charge of 1 fC and corresponds to the equivalent noise charge in electrons. To reduce the spread of the gain in the individual channels, a trim circuitry in the chips can be used. The mean of the input noise per chip is the most important quantity in following comparisons of modules before and after assembly on petalets. It is obtained from a
Gaussian fit of the input noise values from each individual channel of the ASIC. Its uncertainty is the standard deviation of the fit over the 128 channels [4].

4.2 Testing of split readout scheme petalets

Five split readout scheme petalets were evaluated. The input noise was measured under different conditions and its behaviour was evaluated. The thermal behavior of a split readout scheme petalet was also investigated.

4.2.1 Electrical tests

All modules of each petalet were operational showing a successful assembly. The leakage currents were measured after assembly, showing a similar behavior compared to previous measurements of the modules on test frames. A representative input noise figure obtained from four modules of one petalet is presented in figure 15. It shows the average input noise from ten measurements for twelve ASICs of each module at a bias voltage of 150 V and cooling liquid temperature of 0°C [20]. BCC address 59 corresponds to the upper module on the front side and BCC address 60 to the lower one. BCC address 61 (upper module) and address 62 (lower module) correspond to the modules of the back side. Individual variations between modules are caused by different sensor qualities and different interstrip capacitances due to longer strip lengths for lower modules. The uncertainties are in the order of 0.1%, and not shown in the histogram.

![Figure 15](image.png)

**Figure 15.** Average input noise over ten measurements for twelve ASICs from four modules of a common readout scheme petalet read out simultaneously (petalet common 1). The uncertainties are in the order 0.1%.

The comparison between the behavior of modules tested in test frames and on the core, read out individually and simultaneously, is given in figures 16 and 17. Figure 16 shows the input noise distribution for an upper standard module and figure 17 shows the distribution for a lower module. Distributions of the average input noise on twelve ASICs are presented as a function of bias voltage.
The green curves correspond to operation in the test frame, the red curves to one side of the petalet operating and the blue curves to both sides powered and read out. The similarity of the red and blue data points shows that there is no cross-talk leading to changes in noise due to operation of one side or both sides of the petalet. In all modules the noise is slightly increased after assembly on the cores compared to test results in the test frame. After reaching full depletion, input noise values at 1 fC are about 550 electrons for the upper and 650 electrons for the lower module. Similarly full depletion of all sensors could be obtained for the other petalets and the measurements show a stable operation by having variations in repeated runs of less than 5 electrons.

**Figure 16.** Input noise distributions for a standard upper module on a split readout scheme petalet as a function of bias voltage. The values are averaged over all chips on the hybrid of the module. Curves are given for operation in the test frame (green) and after assembly on the core, operating one side (red) and two sides (blue) (petalet common 4).

A stable operation of the modules is possible and the long-term behavior was tested over 12 hours. Representative values for one petalet are given in table 1.

**Table 1.** Average input noise values for all modules on a petalet (common 5) in a long-term measurement of 12 hours.

<table>
<thead>
<tr>
<th>Module ID</th>
<th>Input Noise at 1 fC [electrons]</th>
</tr>
</thead>
<tbody>
<tr>
<td>upper module front</td>
<td>763±2</td>
</tr>
<tr>
<td>lower module front</td>
<td>789±3</td>
</tr>
<tr>
<td>upper module back</td>
<td>647±1</td>
</tr>
<tr>
<td>lower module back</td>
<td>753±3</td>
</tr>
</tbody>
</table>

The input noise values can be reduced by optimizing sensors but also by improving the grounding and shielding. This has been pursued using shields on power lines of the bus tapes and around the coils of the DC-DC converters.
4.2.2 Thermal tests

Two types of thermal tests were performed. First, the temperature of the petalet under operation was measured with NTCs at different positions of the core surface. The warmest area is found at the DC-DC converters. Second, the input noise behavior was tested at different operation temperatures in an insulated box. The result can be seen in figure 18 in the temperature range from 7°C to 28°C. An increase with temperature of about 20 electrons was measured in this temperature range. The uncertainty on the temperature was caused by the non-optimal cooling method with dry ice in an insulated box.

4.3 Testing of common readout scheme petalet

The petalet in common readout scheme is shown in figure 19 and was evaluated using the same electrical tests. Three DC-DC converters and BCC boards, one for each module are placed next to each other on both core surfaces. All six modules were operational, however not all BCC boards were fully functional and two were replaced. The input noise distributions for individual chips of all six modules at a bias voltage of 150 V, which is above the full depletion voltage, are shown in figure 20. The values are averaged over the 128 channels of each chip. Variations between chips of one module are small. The upper right back module had problems during gluing, which resulted in an increased noise compared to the other upper modules. A summary of the electrical performance is given in table 2.

4.4 Comparison of readout schemes

Petalets of both readout schemes were successfully assembled and tested. Table 3 summarizes the electrical performance, including the averaged input noise values for each petalet, and indicating

Figure 17. Input noise distributions for a standard lower module on a split readout scheme petalet as a function of bias voltage. The values are averaged over all chips on the hybrid of the module. Curves are given for operation in the test frame (green) and after assembly on the core, operating one side (red) and two sides (blue) (petalet common 4).
the operation conditions (sensor type and grade, maximum bias voltage, temperature). The measurements show that both schemes deliver adequate signals and are feasible to operate. The input noise values at 1 fC vary between 590 electrons and 730 electrons. The variations are caused by different sensor grades. In line with the results obtained with single modules, no large differences in the input noise performance are observed between the two readout schemes during multi-module tests. The behavior after irradiation was not the main scope of the petalet programme and will be studied in detail once the final detector components are available (e.g. new ASICs).

Figure 18. Average input noise of one module for different operation temperatures of the petalet.

Figure 19. Photo of common readout scheme petalet.
Figure 20. Input noise distributions for standard modules on the common readout scheme petalet for individual chips of all six modules at a bias voltage of 150 V. The values are averaged over channels on each chip.

Table 2. Average input noise values of chips for six modules of the common readout scheme petalet.

<table>
<thead>
<tr>
<th>Module ID</th>
<th>Input noise at 1 fC [electrons]</th>
</tr>
</thead>
<tbody>
<tr>
<td>upper left front</td>
<td>572.0±0.7</td>
</tr>
<tr>
<td>upper right front</td>
<td>559.4±0.6</td>
</tr>
<tr>
<td>lower front</td>
<td>675.3±0.7</td>
</tr>
<tr>
<td>upper left back</td>
<td>563.0±0.8</td>
</tr>
<tr>
<td>upper right back</td>
<td>694±1.4</td>
</tr>
<tr>
<td>lower back</td>
<td>665.1±0.7</td>
</tr>
</tbody>
</table>

The common readout scheme has an electrical topology which covers both sides of a petalet. This implies that the bus tape is folded on top of the core but only one end-of-petalet board is required. The later is also challenging, causing electrical routing constraints. It has the advantage using only one bus tape flavour and allows a reduced amount of tape since not all the area of the petalet requires coverage. The bus tapes of the split readout scheme are single-sided and required two different types to connect the modules on the front and back sides to separate end-of-structure boards. Whilst this concept results in a larger tape surface, it requires a smaller amount of DC-DC converters and offers advantages in terms of HV insulation and ease of routing.
Table 3. Overview of input noise values for all petalets and various operation conditions. Std refers to standard sensors, emb to embedded sensors. Similarly in ref. [20].

<table>
<thead>
<tr>
<th>Petalet common</th>
<th>common 1</th>
<th>common 2</th>
<th>common 3</th>
<th>common 4</th>
<th>common 5</th>
<th>split 1</th>
</tr>
</thead>
<tbody>
<tr>
<td>sensor type</td>
<td>std</td>
<td>std</td>
<td>emb</td>
<td>std</td>
<td>emb</td>
<td>std</td>
</tr>
<tr>
<td>sensor grade</td>
<td>A</td>
<td>B</td>
<td>A</td>
<td>A/B</td>
<td>A/B</td>
<td>A</td>
</tr>
<tr>
<td>temperature [°C]</td>
<td>0</td>
<td>15</td>
<td>5</td>
<td>-20</td>
<td>-20</td>
<td>-15</td>
</tr>
<tr>
<td>bias voltage [V]</td>
<td>150</td>
<td>150</td>
<td>140/130</td>
<td>200</td>
<td>100/250</td>
<td>150</td>
</tr>
<tr>
<td>Input noise [electrons]</td>
<td>601</td>
<td>674</td>
<td>728</td>
<td>597</td>
<td>727</td>
<td>621</td>
</tr>
</tbody>
</table>

A comparison of the mechanical implications of the two readout schemes shows that for assembly, and particularly the gluing procedure, the bus tape of the common readout scheme was slightly more difficult due to its wrapping around the top of the carbon core. In addition, its long shape could enhance CTE mismatches. Similar difficulties are expected when co-curing bus tapes on face sheets. The split readout scheme bus tapes have slightly more material because they have also kapton below the sensor area which can be avoided in future for bus tapes in common readout scheme. It is estimated to have an increase of 3.5% of the bus tape radiation length per bus tape for full-size petals. In terms of module loading, no differences are observed between both readout schemes, as an equal number of mounting steps per module is required. Moreover, the assembly of the split readout scheme hybrids is easier in the module assembly step. For both schemes, a higher accuracy in module placement is expected making use of the sensor fiducials. Modules are single entities in both concepts and it is suggested to reduce the width of the hybrids to match the sensor widths [4].

In summary, despite slightly additional material and the need of different bus tape flavours per side, after an ITk internal review, the ITk strips community agreed to use the split readout scheme for future prototyping of large structures, i.e. petals. This choice will also allow more direct synergies with the developments of the central part of the future ATLAS strip tracker.

5 Summary and conclusions

In the petalet project, fully equipped structures for the upgrade of the forward region of the silicon strip tracker of the ATLAS experiment were developed, prototyped and evaluated. In addition, the project aimed at demonstrating the feasibility of the components and a selection of the readout scheme. Six fully integrated petalets were successfully built deploying two different readout schemes, the feasibility of which has been demonstrated.

Carbon-fibre sandwich structures with embedded titanium cooling pipes were built, including the development of bent pipes. Two bus tape designs were laid out and the gluing process of the bus tapes onto the cores was developed. In the future, co-curing of the bus tapes and carbon fibre facesheets is expected to improve the planarity of the assembly. Preliminary prototyping of this process shows very encouraging results. The silicon sensor modules were mounted on the cores by custom-designed tooling, maintaining a precision to keep clearances between modules. The introduction of fiducials in both the silicon sensors and the petal cores is expected to enhance the
positioning accuracy of the modules. The thermal behavior of the petals is acceptable, as shown for the measured range. The modules of the various petals were found to be fully functional after loading and the development of adapter boards was successful. Both sides of the petals can be read out simultaneously and do not influence each other significantly. The direct comparison of input noise values of different petals is misleading due to different sensor grades which dominate the noise behaviour. In summary, the mean input noise values at 1 fC, averaged over all modules of one petal, show variations for different petals between 590 electrons and 730 electrons. The minimum input noise for a lower module is 650 electrons and for an upper module 550 electrons in both layouts. Comparing these values with results from single modules measured in test frames (lower modules about 650 electrons, upper modules about 520 electrons) [4], the noise values are slightly higher for petals. The grounding was optimized for all petals. General problems in the operation were the initial start of the modules and the operation of BCC boards, which partially failed and needed to be replaced. For modules on petals they will be replaced with new ASICs and implemented in the hybrids. The connectors soldered on the bus tapes proved to be fragile, and thus their use is envisioned to be avoided in future bus tapes.

The experience and knowledge gained in this work is directly transferred to the prototyping of full-size petals. They will employ the split readout scheme due to easier module assembly and bus tape routing. In future studies, irradiation, systematic temperature cycling and high rate tests are foreseen.

Acknowledgments

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