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Abstract:
Deliverable D4.2 is the fabrication of the readout chip for imaging calorimeters of WP14 and timing detector of WP13. After the choice of TSMC130 nm as preferred technology for performance and radiation hardness in Milestone MS22 and the design review of milestone MS63, the chip ASIC HGCROC1 has been fabricated in summer 2017 and delivered in October 2017. It is now being tested and will soon be delivered to WP13 and WP14 for tests with detector.
AIDA-2020 Consortium, 2018
For more information on AIDA-2020, its partners and contributors please see [www.cern.ch/AIDA2020](http://www.cern.ch/AIDA2020)

The Advanced European Infrastructures for Detectors at Accelerators (AIDA-2020) project has received funding from the European Union’s Horizon 2020 Research and Innovation programme under Grant Agreement no. 654168. AIDA-2020 began in May 2015 and will run for 4 years.

### Delivery Slip

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Executive summary

HGCROC is a high performance readout ASIC designed for new imaging/timing calorimeters. The chip has been fabricated in TSMC 130 nm during summer 2017 and is now under test before being delivered to WP13 and WP14 for tests with detector.

1. INTRODUCTION

Readout ASICs are a crucial element of modern “imaging” calorimeters, where the number of channels has increased tremendously to allow particle flow algorithms. More recently, picosecond timing capability has been developed to provide useful additional information and pileup rejection.

The deliverable of WP4.3 consists of the readout ASICs for the imaging calorimeters of WP14 and timing detectors of WP13. The technology chosen in Milestone MS36 was TSMC130 nm. The chip developed is called HGCROC1 for High Granularity Calorimeter Read Out Chip. It includes blocks designed by several AIDA2020 partners: CERN, Imperial and IRFU.

2. HGCROC ASIC

2.1. ASIC DESCRIPTION

HGCROC is a 32-channels ASIC for charge and time readout. It has been designed originally for the CMS HGCAL calorimeter [1] and can be used with SiPMs and RPCs for accurate charge and time measurements. The specifications are the following:

- **low noise** (2500 e\(^-\)) and **large dynamic range**, from 0.2f C to 10 pC
- **linearity** better than 1% over the full range
- ability to provide **timing information** with a precision better than 50ps for pulses above ~12 fC (corresponding to about 3MIPs in the 300 um silicon)
- **fast shaping time** (peaking-time <20ns) to minimize the out-of-time pileup
- **compensation of the leakage current** which will develop in the silicon devices after irradiation (DC coupled sensors)
- **compatibility with negative and positive inputs** sensors, to be able to read both p-on-n and n-on p
- on detector digitization and **data processing for zero suppression, for linearization and summing of the trigger data**
- **maximum latency** of 36 bunch crossings for the trigger primitives at the output of the detector
- **buffering** of the data to accommodate the 12.5 \(\mu\)s latency of the L1 trigger;
- high speed readout links to interface with the 10Gb/s low power GBT serialiser
- **low power budget** <20 mW
- **high radiation resistance** (> 1.5 MGy and \(10^{16}\) neq) and SEU compliance

The schematic diagram is shown in Figure 1 below:
The chip has been reviewed before fabrication in April 2017, which constituted AIDA2020 milestone MS63.

It covers an area of 35 mm² and the layout is shown in Figure 2. The 32 channels are split 16/16 with the bias and clock distribution in the middle. The analog inputs are on the left side and the digital outputs on the right side.

It has been sent to TSMC in July 2017 and received back in October.
2.2. ASIC SIMULATED PERFORMANCE

The performance has been evaluated from simulations and from measurements on a previous test vehicle for the analog part [2]. The analog waveform shown in Figure 3 (left) exhibits a peaking time of 20 ns in good agreement with simulations and the noise (Figure 3 right) is also below 2000 e- for \( C_d = 47 \) pF, which fulfills the specifications.

![Figure 3: Measured pulse shape and Equivalent Noise Charge of Test Vehicle TV2 [2].](image)

The large signals are readout with Time over Threshold technique (ToT), measuring the preamplifier output width when it enters saturation. This width is proportional to the input charge up to 10 pC as shown in Figure 4 (left). Finally the timing performance is shown in Figure 4 (right), exhibiting a jitter of 50 ps for signals larger than 100 fC.

![Figure 4: Time over Threshold (ns) as a function of input charge (pC) (left) and jitter (ps) as a function of input charge (pC) (right). Measured on Test Vehicle TV2 [2].](image)
3. HGCROC FABRICATION AND TEST

The chips were received in October 2017 and a test-board has been prepared in collaboration with CEA-IRFU and Imperial College London. Six PCBs were manufactured in October and assembled in November. The ASICs were then bonded directly on the PCB, but the company hired for this job run into internal difficulties that delayed the operation by one month and a half and resulted in very poor quality bonding (see Fig. 5). Indeed, out of the six boards, none got all the connections made and we could only perform tests on partial areas. New boards are being refabricated and will be bonded at CERN in order to have fully working test stands to distribute to WP13 and WP14.

![Fig. 5: Zoom on the bonding issues found on the test board. Several missing connections are visible.](image)

![Fig. 6: Test board for HGCROC with the chip bonded directly on the PCB. High-speed data are read by a Xilinx Kintek KCU5 digital board. First signals can be seen on the oscilloscope.](image)
4. CONCLUSION AND RELATION TO OTHER AIDA-2020 WORK

The ASIC for imaging/timing calorimeters has been fabricated according to AIDA2020 schedule and constitutes deliverable D4.2. It is now being successfully tested and will rapidly be delivered to WP13 and WP14 for tests with detectors.

REFERENCES


https://indico.cern.ch/event/608587/contributions/2614093/contribution.pdf