ATLAS Tile Calorimeter Upgrades for HL-LHC

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Abstract

The High-Luminosity phase of the Large Hadron Collider (LHC) at CERN is expected to begin in 2026, delivering a luminosity of $5 \times 10^{34} \text{cm}^{-2}\text{s}^{-1}$, with up to 200 interactions per 25 ns bunch crossing. In order to cope with the expected high trigger rates and intense radiation environment, the ATLAS Tile Calorimeter will be upgraded with re-designed electronic systems that will maintain its optimal performance in its future operation.

Keywords: Calorimetry
PACS: 29.40.Vj

1. Introduction

The Large Hadron Collider (LHC) \cite{1} at CERN is scheduled to undergo a decisive upgrade program \cite{2}, that will extend its physics potential well beyond the initial design goals \cite{3, 4}. The final, High-Luminosity LHC (HL-LHC) is expected to begin operation in the year 2026, delivering an instantaneous luminosity of about $5 \times 10^{34} \text{cm}^{-2}\text{s}^{-1}$ and aiming to collect an integrated luminosity of at least 3000 fb\textsuperscript{−1} by the year 2035.

In order to perform in the harsh radiation environment of the HL-LHC, with up to approximately 200 proton-proton collisions per 25 ns bunch crossing, the ATLAS detector \cite{5} is also scheduled for important upgrades, targeting for an all-new inner tracker, upgraded calorimeters and muon spectrometer, as well as an improved trigger and data acquisition system \cite{6}.

2. The ATLAS Tile Calorimeter

The Tile Calorimeter (TileCal) \cite{7} is the central hadronic calorimeter of ATLAS, constructed of steel plates as absorber and scintillating tiles as active medium. It is divided into two central long-barrel and two extended-barrel partitions, covering the pseudorapidity\textsuperscript{1} range $|\eta| < 1.7$. Each barrel is comprised of 64 wedge modules, tightly aligned along the azimuthal coordinate. The scintillation light is collected from both sides of the tiles by wavelength-shifting (WLS) fibres, which are bundled, to define readout cells, and coupled to a pair of photomultiplier tubes (PMTs). This arrangement of the Tile readout employs a total of 9852 PMTs.

3. Mechanics

The PMTs and Front-End (FE) electronics are inserted at the outer radius of each Tile module, currently housed by a pair of mechanical structures, called “drawers”. The upgrade plan foresees the replacement of the 1.4 m long drawers with mini-drawers of half their size to improve the reliability of the cooling circuits and grant easier access to the electronics. Each mini-drawer is designed to host up to 12 PMTs, along with dedicated FE readout and High Voltage (HV) distribution cards. Another benefit of the mini-drawers is the reduced demand for a wide detector opening in order to service the Tile electronics.

4. Front-End electronics

The PMTs are currently read by FE cards, which shape and amplify the signal in two channels, with a gain ratio of 64. The analog output is then digitised by 10-bit 40 MSps Analog-to-Digital Converters (ADCs), located on dedicated boards, serialised and transmitted to the back-end electronics upon trigger decision. The upgraded readout system is adapted to the trigger policy of ATLAS for the HL-LHC, which requires delivery of the data from each mini-drawer to the off-detector electronics, upon each bunch-crossing. As in the current system, the analog processing of detector signals is performed in two channels, but with a gain ratio of 32, while digitisation is carried out at the Mainboard by 12-bit ADCs, establishing an effective 17-bit dynamic range. The digitised data are finally received by the Daughterboard, that handles all communication with the back-end electronics, to be deserialised and propagated to the off-detector Pre-Processor (PPr) through high-speed optical links.

5. Pre-Processor (PPr)

The PPr serves as the off-detector interface to the FE electronics, sending Detector Control System (DCS) commands...
and run-control data to the Daughterboards, using the GigaBit Transceiver (GBT) protocol (4.8 Gbps). Each PPr unit receives and deserialises the data from 32 mini-drawers, at the 40 MHz LHC clock cycle, and stores them in pipeline buffers. At the same rate, reconstructed data are transmitted to the trigger system. The stored samples are then forwarded to the ATLAS data acquisition system upon trigger decision. Finally, the PPr is designed as a full ATCA (Advanced Telecommunications Computing Architecture) blade to fit the new data communication protocol adopted by ATLAS for the HL-LHC.

6. Low Voltage Power Supply

The Low Voltage Power Supply (LVPS) system controls and monitors the operating voltage of the FE electronics. Each Tile module is supplied by one water-cooled LVPS box, installed at the “finger” of each Tile module (right in front of the two drawers), consisting of eight individual power supply boards, called “bricks”, a fuse board and a monitoring/control board. Currently, each brick converts a 200 V input to the output low voltage required by the sub-circuit it is powering. The new brick design, however, uses identical bricks with 10 V output, while the supply for the individual loads will be created by means of point-of-load regulators located at the loads. This allows redundancy to the system by grouping the bricks into four sets of two and using a diode-OR on the point-of-load regulators.

7. High Voltage Power Supply

The High Voltage Power Supply (HVPS) system controls and monitors the voltage applied to each PMT. In the current system a primary HV feeds the HV regulation boards (HVopto) installed on each drawer. In the new system, the HV regulation boards (HVremote) will be located in the ATLAS counting room, out of the radiation environment of the detector, granting permanent access for maintenance, while the monitoring and control system will be implemented by means of Ethernet links. Furthermore, the current, passive HV dividers, attached to the base of each PMT, will be upgraded into active dividers with one transistor and one diode in parallel, in the last three stages. The new design has demonstrated improved linearity for a large range of DC currents, pulse shape stability and radiation hardness.

8. Calibration Systems

The TileCal incorporates three calibration systems to ensure accurate and stable measurements. First, the Charge Injection System (CIS), implemented on each FE card, injects the readout electronics with known charge, allowing constant monitoring but also mapping of the FE response (ADC counts) to the input charge (pC). For the HL-LHC, the CIS will be updated to cover the input range of the new FE electronics. Next, the Cesium (Cs) system allows calibration of the full optical chains (scintillating tiles, WLS fibres, PMTs, FEs) by means of a movable $^{137}$Cs $\gamma$-source, hydraulically circulated through a system of tubes that traverses every tile-row. The upgrade plan foresees integration of the control data flow into the standard data readout electronics (GBT slow control stream), optimization of the operation mode and revision of the principle of the source movement. Finally, the laser system monitors the PMT gains between subsequent Cs scans. The current, reliable architecture will be preserved, with substitution of aged components and adaptation of the interfacing card, called LASCAR (LAser Calibration Rod), to comply with the ATCA format of the PPr.

9. Conclusion

As described in the above sections, the TileCal strategy for the HL-LHC relies on the current design, which has demonstrated excellent performance during the preceding data-taking periods [8]. The scheduled upgrades, focused on the optimisation of the readout system, will allow the TileCal to cope with the harsh radiation environment of the HL-LHC in order to fully exploit the unprecedented delivered luminosity.

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References