The ATLAS Tile Calorimeter Phase II Upgrade

A major upgrade of the LHC is planned by 2024 with the aim of increasing the instantaneous luminosity up to $7.5 \times 10^{34} \text{ cm}^{-2}\text{s}^{-1}$, leading to the High-Luminosity LHC (HL-LHC). A new readout architecture with a full-digital trigger system will be implemented in TileCal, the ATLAS central hadronic calorimeter. The upgrade of the TileCal readout electronics is required to cope with the new requirements. In the HL-LHC era, the on-detector electronics will transmit readout data for every bunch crossing to the PreProcessors (TilePPr) in the off-detector electronics, which will provide data to the trigger and DAQ systems.

![Diagram of the TileCal readout architecture for the HL-LHC.](image)

**Clock and Dataflow at the Test Beam Setup**

The TileCal Demonstrator Upgrade project aims to evaluate and qualify the proposed readout architecture before its full replacement during the Long Shutdown 3 (2024-2026). As part of the Demonstrator project, prototypes of the new electronics are being validated in several test beam campaigns at the CERN SPS facilities between 2015 and 2018. The Demonstrator module includes all the upgraded on-detector electronics needed for the digitization of PMT signals, high-speed communication with the off-detector electronics, the calibration circuitry, and the high voltage distribution system.

![Eye diagram at 4.8 Gbps with a RI of 2.74 ps and DJ of 2.44 ps.](image)

The TilePPr Demonstrator is responsible for the reception and processing of the digital data coming from the Demonstrator module, and for the distribution LHC clock to the on-detector electronics. This prototype can operate one TileCal module representing 1/8 of the final TilePPr module for the HL-LHC.

The TilePPr Demonstrator has a double mid-size Advanced Mezzanine Card (AMC) form factor with 4 QSFP modules, one Virtex 7 FPGA (Readout) and one Kintex 7 FPGA (Trigger). The Readout FPGA reads out and operates the Demonstrator module through the QSFP modules using the GigaBit Transceiver (GBT) protocol. A total of 16 GBT links are used to encode Detector Control System (DCS) commands and Timing, Trigger and Control (TTC) information at 4.8 Gbps, while detector data is received and decoded at 9.6 Gbps.

![Eye diagram at 9.6 Gbps with a RI of 2.97 ps and DJ of 5.97 ps.](image)

Digitized data from the on-detector electronics are stored in pipeline memories at the LHC frequency upon the reception of a trigger acceptance signal, when selected data is transmitted to the Phase II Upgrade FELIX system and to the legacy DAQ system keeping backward compatibility with the current readout architecture.

The GBT links were configured for fixed and deterministic latency operation providing to the on-detector electronics a clock synchronous with the LHC. The stability of the clock distributed towards the on-detector electronics was studied using digital phase monitoring tools based on subsampling techniques. These tools permitted the detection of non-deterministic latency variations in the high speed path produced after a power cycle or due to temperature drifts. Time variations observed between the distributed and received clock from the on-detector electronics have a maximum value of 100 ps full pk-pk.

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