The Phase-1 Trigger Readout Electronics Upgrade of the ATLAS Liquid Argon Calorimeter

Yuji Enari, on behalf of the ATLAS Collaboration
ICEPP, the University of Tokyo, 7-3-1 Hongo, Bunkyo-ku, Tokyo 113-0033, Japan
E-mail: yenari@icepp.s.u-tokyo.ac.jp

Abstract. Electronics developments are pursued for the trigger readout of the ATLAS Liquid-Argon Calorimeter towards the Phase-I upgrade scheduled in the LHC shut-down period of 2019-2020. The LAr Trigger Digitizer system will digitize 34,000 channels at a 40 MHz sampling with 12 bit precision after the bipolar shaper at the front-end system, and transmit to the LAr Digital Processing system in the back-end to extract the transverse energies. Results of ASIC developments including quality assurance and radiation hardness evaluations, performances of the final prototypes and results of the system integration tests will be presented along with the overall system design.

1. Introduction
ATLAS Liquid-Argon Calorimeter (LAr) is a sampling calorimeter designed for providing precise measurements of the electromagnetic (EM) object pseudo rapidity up to 2.5 and hadronic object in the forward region. Precise measurement and triggering EM object are very important for the physics at LHC, as one can recognize it from the fact that the Higgs discovery has been established with two photons and four leptons final states.

To explore physics beyond the Standard Model, the LHC upgrade to increase instantaneous luminosity is scheduled as described in Fig. 1. With current instantaneous luminosity of $L \sim 1.7 \times 10^{34}$ cm$^{-2}$s$^{-1}$, average number of interaction for each bunch crossing, $\mu$, is about 50. In the Run-3 starting from 2021 after the second Long-Shutdown (LS2), the luminosity will be increased by about 1.5, the expected $\mu$ is 80. For the high luminosity LHC (HL-LHC) run from 2026, the luminosity will be enhanced by a factor two, the expected $\mu$ is up to $\sim 200$.

Increase of instantaneous luminosity degrades detector resolution and increases background rate due to pileup effect, which is originated from the multi-jet processes and the inelastic $pp$ collision. There is a limitation for data taking capability, we need to reduce the trigger rate by raising threshold on the transverse energy ($E_T$) of the object if we use current system. The ATLAS LAr Calorimeter readout electronics will be upgraded in two stages, Phase-1 and Phase-2. The Phase-1 upgrade is for trigger electronics scheduled in the LS2 from 2019 to 2020. And the Phase-2 upgrade is for main readout system in the third Long-Shutdown (LS3) from 2023 to 2025 before entering the HL-LHC era.

2. ATLAS LAr Phase-1 upgrade project
In order to reduce the backgrounds for EM trigger, the granularity of the trigger readout needs to be finer. As shown in Fig. 2, the current trigger readout, so-called Trigger Tower (TT), is
based on an analog sum of signal from the calorimeter cell in the range of $\Delta \eta \times \Delta \phi = 0.1 \times 0.1$ for all four layers of the ATLAS EM calorimeter. This size is larger than the size of “Moliere” radius, which is 0.08 in $\eta$, and the TT is insensitive for shower development. In new system, we are going to introduce new readout, so-called Super Cell (SC), which is layer by layer, with increased readout granularity by four times with respect to the TT in the middle layer and the front layer. With the SC readout, the EM shower development can be measured as shown in Fig. 2 (the color shows energy deposit in each TT or SC of the calorimeter in case of 70 GeV electron). The current readout sends the summed analog signal from on-detector (frontend, FE) electronics to the off-detector electronics (backend, BE) system with 70 m copper cable. This can not be realized for the SC readout which has 10 times more channels with respect to the TT readout. Therefore, the new FE electronics needs to digitize the analog signals, and send them via optical fibers. And the BE system performs a real-time digital signal processing.

Thanks to the finer readout in the front and the middle layer, we can reconstruct shower shape variable, i.e. $R_\eta = E_{T3x2}/E_{TTx2}$ as shown in Fig. 3(left). In addition, we can use width of the shower, and energy fraction of the third layer, and so on. By applying additional selection on these shower shape variables, we can improve the performance of the background reduction, which reduces the jet background significantly and makes the trigger rate low. In the ATLAS experiment, the maximum event rate at the first trigger level (hardware based trigger system) is 100 kHz, and allocated budget for EM triggers is limited to 20 kHz. If the trigger rate would exceed the budget, we would need to increase the threshold on the $E_T$ of the EM object. Figure 3(right) shows the trigger rate as a function of the threshold. With the upgraded system, we can apply lower threshold of $\sim 25$ GeV, which is very important to trigger electrons from $W$ and $Z$ boson decay, also photons from Higgs boson, which is the key channels on the physics program in the ATLAS experiment.

Figure 1. LHC upgrade schedule and ATLAS LAr calorimeter upgrade plan

Figure 2. Composition of the Trigger Tower and the Super Cell. Colors indicate energy deposit in case of 70 GeV electron [1].

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3. New Hardware

In order to minimize potential risk and to make smooth transition, we are going to install new trigger readout path with keeping current main and trigger readout. An overall schematic of new system is shown in Fig. 4. After the Phase-1 upgrade, the current trigger path will be used until the validation of the new trigger readout is finished. The components to be replaced are the baseplane and the layer sum board (LSB) as described below.

- Baseplane of the FE crate on detector
  In order to digitize the analog signal of the SC at the FE, we need to insert new electronics board into the FE crate, which is the LAr Trigger Digitizer Board (LTDB). This means we need to replace the baseplane of the FE crate which is a custom-made PCB board to pass the signal from the calorimeter cell to the front end readout board (FEB), and routing from the FEB to the trigger readout board.

- LSB in the FEB
  The SC has finer granularity, therefore electronics circuits summing the analog signal need to be modified. This is done by the LSBs, a small mezzanine board in the FEB. To replace the LSB, we need to extract all FEBs from the FE crate and bring them to surface during the LS2. The production of new LSBs have been done and now the quality assurance (QA) is going.

New electronics board in the FE is LTDB described in next section. And the new BE system, LAr Digital Processing System (LDPS), is described in Section 5. During LS, we will also install optical fibers (70 m, ~ 7,000 fibers) from the LTDB to the LDPS.

4. LAr Trigger Digitizer Board

There are three main functionalities for the LTDB as shown in Fig. 5. The first is analog signal treatment, which includes the analog sum for the front and the middle layers to build the TT signal, and ADC driver. The second is the analog-to-digital conversion, which is processed by an ASIC, so-called Nevis-15 [2]. The third functionality is serializing the ADC data for several SCs and transmitting to the backend system, which are performed by LOCx2 chip and LOCld chip [3]. The control signal transmission of the LTDB is performed via the GBT link, which is running with 4.8 Gbps. The GBT link includes the Timing, Trigger and Control (TTC) signal,
which provides the common system clock synchronized with LHC clock. A LTDB can handle up to 320 SCs, its key components are radiation hard ASICs.

4.1. Custom-made ASICs
These custom-made ASICs are designed for the LAr Phase-1 upgrade. The chip design are finalized about two years ago, and now, these packaging are being finalized. Because the LTDB is one of the FE electronics, it needs to be radiation-tolerant. The requirement for the ATLAS LAr FE electronics is that any electronics component needs to be stably functional after receiving 100 kRad of total dose, and passes the single event effects (SEE) tests with total fluency of $3.8 \times 10^{12}$ hour/cm$^2$. Performance and each production status are summarized below.

- Nevis-15 Quad Channel ADC
  Nevis-15 is a quad channel ADC, 40 MS 12 bits pipeline ADC fabricated with IBM8RF 130 nm CMOS technology. Effective number of bits should be larger than 11 bits, measured dynamic range is 11.7 bits on the chip of the engineering production. It should be low
Figure 6. Photograph of LTDB[1] (a), and schematic of Nevis-15 ADC chip[2] (b) and LOCx2 serializer chip[3] (c).

power consumption, established chip has 50 mW per channel. The chip must have a fixed latency of less than 100 ns (and measured latency of 100 ns). The radiation tolerance has been verified up to 10 MRad, and observed SEE cross section is $10^{12}$ cm$^2$ per channel [2].

Towards the production (13,000 chips), the wafer production, the dicing and packaging processes have been established with an yield of 80%. This is based on a result of Quality Control (QC) for 186 chips with engineering production wafer. The QA procedure has been established, about 2,100 chips can be checked every week, and all chips are expected to be available in August 2018.

- LOCx2 Serializer and LOCld laser driver

LOCx2 is the serializer for LTDB, which is a dual channel 8×14 bits for 5.12 Gbps transmission. Both LOCx2 and LOCld chips are fabricated with a 250 nm Silicon-on-Sapphire technology. The LOCld laser driver is a dual channel VCSEL driver. The latency of the serializer must be less than 75 ns.

The radiation tolerance has been verified up to 200 kRad TID and has been confirmed no issue on the output eye diagram in the optical data transmission test with LOCld with the serialized digital data through LOCx2 chip.

The wafer production has been finished without any issue. However, we have encountered issues on the packaging. We are trying out several companies to produce stable and reliable chips with reasonable yield (60%-70%).

Figure 6 shows a pre-production version of the LTDB. In this version, the final design of ASICs are used, and the board design of the circuit are also close to the final version. Two boards have been assembled and been replaced the demonstrator in the ATLAS detector after an extensive test. Currently, the last modifications are being done, and final verification process is underway before mass production (~ 150 boards including spare boards.).

5. LAr Digital Processing System

Main functionalities for the LDPS are (i) receive ADC data and align timing, (ii) compute the $E_T$ for each SC with identifying bunch crossing timing, (iii) sum the $E_T$ in the defined area, (iv) send computed result to the ATLAS Level-1 Trigger (Level-1) system. Because the 12 bits ADC is used for each SC, the data transfer rate from the LTDB to LDPS become 25.2 Tbps in total. After converting into the $E_T$, same information needs to be sent at least two destination including the summed $E_T$, the output data transferring rate becomes 41.1 Tbps to the Level-
1 system. The dense and high speed optical links, and a real time digital signal processing performed in a high performance FPGA, are crucial items for this system.

The system is designed with the Advanced-TCA (ATCA) architecture. In this system, the core hardware is the Advanced Mezzanine Card, so called LATOME, and the ATCA carrier blade (LArC) with the RTM card. Photographs of the final version are shown in Fig. 7. In total, the LDPS consists of 124 LATOMEs, 31 LArCs with three ATCA shelves.

5.1. LArC
The LArC carries four LATOMEs. It provides LATOMEs power, system clock, control signals and monitoring data transfer. The power consumption for each LATOME is close to maximum 80 W, which is ATCA regulation limit, therefore the LArC has capability to supply power up to 400 W per board. In addition the LArC has a role of high speed network switch. There are a GBT link and a 10 Gbps link for monitoring data transfer from each LATOME. These functionalities are realized with Xilinx Vertex-7 FPGA. In order to establish these requirements, the number of layer of PCB becomes 22, which is fit in the thickness of 2.4 mm.

5.2. LATOME
The LATOME has 48 links with 5.12 Gbps per link from the LTDB, and 48 links with 11.2 Gbps to the Level-1 system. These data flows are the main data streams for the LDPS. This is realized with the microPOD. It is a commercial chip, having 12 RX links or 12 TX links. All high speed links are connected to Intel Arria-10 FPGA. In addition, a system clock with trigger information, a control link of 1 Gbps, and two monitoring links (10 Gbps and GBT links) are connected to the LArC. The PCB of the LATOME has 16 layers with the thickness of 1.6 mm.

5.3. LATOME firmware
The Arria-10 FPGA on the LATOME performs digital processing for the main data stream. There are four logic blocks. Each block has specific task with different base clock frequency in order to fulfill the system requirements.

- Input Stage: Receive 48 data streams, and align the bunch crossing timing for all links (all LATOMEs in the system, by setting proper length of FIFO). This block is running with 320 MHz clock.
- Re-Map: Remap SCs across serialized data stream in order to minimize the latency for the $E_T$ summing among the TT of the SC. The remapping is performed with 320 MHz clock, and switch to 240 MHz clock with increasing the number of stream from 48 to 62.

Figure 7. Photograph of LAr Carrier blade (left) and LATOME (right) [1].
• User Code: Compute $E_T$ with assigning of the bunch crossing timing for each SC. A optimal filtering algorithm, which is one of finite impulse response (FIR) filter is used. The FIR calculation is based on combination of multiplication and summing, i.e. $E_T = \sum_{i=1}^{4} a_i S_i$. Here $S_i$ is ADC data and $a_i$ is the filtering co-efficient which are set by the algorithm with minimizing noise [4]. The multiplication is performed with DSP block integrated in the Arria-10 FPGA. In order to find the peak of the pulse, we implement 4-stage FIR filter. The latency of this block is realized with 4.5 bunch crossing.

• Output Summing: Perform $E_T$ summing in the range of $\Delta \eta \times \Delta \phi = 0.1 \times 0.1$ (the TT), and $0.2 \times 0.2$ with 240 MHz clock. Then the base clock is switched with 280 MHz in order to serialize each stream for transmitting data to the Level-1 trigger system.

5.4 Backend system test

In order to verify hardware capabilities, we have built a test stand with ATCA based system. We have verified first the power consumption as a function of the number of links and the number of DSP. This is the most basic and important test. We have confirmed the LArC can provide full load of power to LATOMEs up to 80 W, and there is no voltage drop on supplied voltage at LATOME as shown in Fig. 8. Also we have performed data transmission test from LATOMEs to Level-1 system, and verified all 48 RX and 48 TX have the bit error rate less than $10^{-14}$ with the data transfer speed of 11.2 Gbps.

As an integrated system test, two LArCs with four LATOMEs are used for a loop back test, two of LATOMEs sending a set of pseudo LTDB data as generators and the other two LATOMEs performing the original data processing as described in last section. The latter two LATOMEs send back the processed data to the generator LATOMEs in order to verify the data contents as expected. With this system, we confirmed long run stability (several hours). Also, an overall latency has been measured as 15.38 bunch crossings while its requirement is 15 bunch crossings. The stability of the latency against various resets is also verified.

6. LAr Phase-1 Demonstrators

Even after verifying all functionalities at the test stand, operating under real beam condition provides a lot of valuable experiences. We have installed and operated two kind of LTDB demonstrators and two LDPS demonstrators since 2014. The demonstrator system has collected data from the beginning of the LHC Run-2 with 13 TeV $pp$ collision. In 2018, we have replaced the LTDB demonstrators with the pre-production version, which are built with the production version ASICs with semi-final version of LTDB circuit. We can verify hardware
Figure 9. (a) Measured pulse shapes (red) of SCs in the LAr Phase I demonstrator are compared with predicted pulse shapes (black) for the middle layer. 3D box plots (size of each box is proportional to the $E_T$ in each SC) show the reconstructed transverse energy in the SC readout (b) and the main readout(c), and those relation (d). All results on demonstrator are described in [5].

stabilities including fixed latency of full upgraded system. Figure 9(a) shows reconstructed pulse shape from data taken with the demonstrator system [5]. The understanding of pulse shape is crucial item to have precise $E_T$ measurement with the optimal filtering. The black line shows an expected pulse shape which is extracted from calibration system, and the red points are collision data. There are good agreements especially in the peak region. Disagreement in the overshoot part is known feature of mismodeling of the liquid argon gap (distance between the electrodes). The reconstructed $E_T$ is compared with reconstructed $E_T$ based on the main readout. Figures 9(b) and 9(c) show observed $E_T$ in each SC for an EM cluster which has $E_T$ of 124.4 GeV, for the demonstrator system and the main readout system, respectively. Those relation have a good linearity as shown Fig. 9(d).

7. Summary
In this presentation, overview and status on the ATLAS LAr Calorimeter Phase-1 upgrade project, which is scheduled coming long shutdown (from 2019 to 2020) are summarized. The upgraded trigger readout system will be used including the HL-LHC up to ~2035.

In the frontend electronics, three custom-made ASICs are in production. The design of new digitizer board are being finalized for mass production. The QA and QC procedure are also being finalized. The pre-production boards are installed into the ATLAS detector as demonstrator in 2018. In the backend electronics, after intensive system tests to verify hardware capabilties and firmware functionalities, the production have been started. Currently assembling and the QA test scheme are developed.

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References