An updated design of the read out link and control board for the Phase-2 upgrade of the ATLAS Tile Calorimeter.

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The ATLAS hadronic Tile Calorimeter (TileCal) is being upgraded for the High Luminosity Large Hadron Collider (HL-LHC). We present a redesign of the TileCal Phase II read out link and control Daughterboard (DB). The DB has a double redundant radiation tolerant design that will provide continuous high-speed readout of digitized data samples of two gains of 12 photomultiplier channels each, while handling the timing, control and communication between the front-end and off-detector electronics, all over multi-gigabit optical links. Four SFP+ modules serve $4 \times 9.6$ Gbps uplinks and $2 \times 4.8$ Gbps downlinks, handled respectively by two re-programmable Kintex Ultrascale+ FPGAs and two CERN developed gigabit link ASICs (GBTx). Better high-speed uplink timing and improved radiation tolerance have been achieved by migrating the previous design from the Xilinx Kintex-7 FPGAs to the Kintex Ultrascale+ architecture. Preliminary TID radiation tests were performed on a Daughterboard revision 5 following the TOTAL DOSE STEADY-STATE IRRADIATION TEST METHOD ESCC22900 and the ATLAS protocol and safety factors.

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1. The ATLAS Tile Calorimeter Phase-II read-out system.

The Tile Calorimeter (TileCal) design for the Phase-II Upgrade of the ATLAS detector for the High-Luminosity Large Hadron Collider (HL-LHC)[1] will assure better timing and energy resolution while decreasing the sensitivity to out-of-time pileup. Approximately 1024 radiation tolerant link and control boards (Daughterboards) will interface the Front-End (FE) with the off-detector systems providing continuous read-out of the entire TileCal at 40 MHz. The off-detector system will provide full-granularity digital data to the first level of trigger.

The Phase-II read-out system is modularized in Minidrawers (MD) (Figure 1a) each serving up to 12 channels. On each channel, each photomultiplier (PMT) signal is shaped, conditioned and amplified by a FE Board (FEB). Each FEB provides two different gain values that are digitized in a Mainboard (MB). A DB provides LHC synchronized timing, control and configuration to the FE, and continuous readout of the MB channels to the Tile PreProcessor (TilePPr) located at the off-detector systems. A TilePPr receives and stores two gains of PMT data in pipelines until a trigger decision event is received, while supplying reconstructed data to the trigger.

![Figure 1](image)

Figure 1: (a) TileCal Phase-II Upgrade Minidrawer, (b) Daughterboard revision 5 picture and (c) block diagram.

2. The Daughterboard Revision 5 design.

The DB Revision 5 (DB5) (Figure 1b) has a double redundant design, allowing nominal running with either one or two working links powered by $4 \times$ SFPs+. Migration from the GTX powered Kintex-7 in previous designs to the GTY powered Kintex Ultrascale+ FPGAs allowed to reach a 9.6 Gbps communication with full compatibility with the LHC timing in addition to improved radiation tolerance[2]. The design included backwards compatibility with legacy interfaces such as high voltage (HV-OPTO), the MB FMC connector and the Cs calibration system[3]. The DB5 includes two xADC panels for extra sensor monitoring and new digital unique ID serial chips for identifying each of the MD halves on-detector. By means of two 4.8 Gbps input links, each of the two GBTx ASICS recovers $2 \times 160$ MHz good quality LHC synchronized clocks from the downlinks in order to drive the transceivers of both FPGAs, and $6 \times 40$ MHz phase configurable clocks, two of them driving the FPGAs relevant logic and four driving the digitizing blocks of each MD quadrant (Figure 1c). Furthermore, each GBTx propagates configuration and control commands to both FPGAs via a configuration bus while providing remote control of the FPGA resets and JTAG chains for
remote reconfiguration of the FPGAs and their attached PROMs. Each FPGA powered with Triple Modular Redundancy enabled firmware transmits continuous GBT-CRC protected words with two gains of digitized PMT data and detector control information to the back-end by means of a pair of redundant readout uplinks.

3. TID tests.

Preliminary TID tests were performed with a DB5 powered by a functional firmware connected to a TilePPr. The DB was exposed to a total of 20 kRad delivered by a 9 MeV $e^-$ beam in six doses over $\approx 1$ h, following the ESCC-22900 standard[4] Level E of TID (20 kRad/200 Gy) "Standard Rate - Window 1": $365 \text{ Rad(Si)}/\text{min} @ 9 \text{ MeV}$ and $381 \text{ Rad(Si)}/\text{min} @ 12 \text{ MeV}$. Between doses, the system was power cycled and FPGAs reconfigured from the PROMs. Monitored currents were constant over the full irradiation process, apart from the GBTx which had a small but measurable current decrease after the 20 kRad exposure (Figure 2a). Temperature and current monitoring showed no evidence of latch-up (Figure 2a and 2b). Core FPGA voltages (VCCint) were extremely stable over the entire irradiation period (Figure 2c). The test finished successfully with no component failure on either the board or the two types of SFP+ tested: the CORETEK CT-000NPP-SB1L-D and the AVAGO AFBR-709SMZ.

![Figure 2: TID Test Results for the DB5 exposed to a total dose of 20 kRad.](image)

4. Conclusions

The DB revision 5 was designed to meet all the requirements for the Phase-II Upgrade. Firmware development and improvement is taking place so that it is fully integrated to the MDs. TID radiation tests showed good preliminary results. However, the doses might need to be adjusted to new ATLAS simulation values according to the ATLAS protocol and safety factors. Near future plans include a testbeam iteration at the SPS at CERN and SEE and NIEL tests.

References


