The JEFX prototype was produced in November 2017 and extensively tested during the last 12 months. The tests were mainly focused on the power consumption, ripple measurement on the MGTS power pins, thermal dissipation, Multi-Gigabit Transceivers reference clock quality and validation of the optical inputs and parallel IOs.

### Validation of all optical inputs

- **Setup used for testing at 240 Gbps simultaneously**:
  - Open Area of Eye Scans @ 11.2 Gbps
  - Xilinx PSM 4.5
  - FPGA PWR Mezzanine

### Hardware Characterization

- **Power consumption and thermal dissipation**
  - Current consumption measured is consistent with Vivado estimations
  - Current consumption and dissipation are with the MGX specs!

- **Phase Noise values for the MGX reference clock are within the Xilinx specs!!**

### Conclusion

The JEFX prototype board has been delivered in November 2017. The board has been extensively and successfully tested over the last 12 months. A pre-production module, with no hardware changes with respect to the prototype, is currently being manufactured and is expected to be delivered before the end of 2018. The final JEFX modules are expected to be installed on the ATLAS detector before the end of 2019.