Updated Readout System

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Abstract:
Detector Interface cards, DIF, respecting the space and power constraints for operation in a Linear Collider Detector, have been developed. For two hadron calorimeter prototypes, the SDHCAL and the AHCAL, DIF cards have been designed and produced. For the SiW ECAL a new DIF system, consisting of four cards has been developed.
AIDA-2020 Consortium, 2019

For more information on AIDA-2020, its partners and contributors please see [www.cern.ch/AIDA2020](http://www.cern.ch/AIDA2020)

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Executive summary

Highly granular calorimeters designed for Linear Collider detectors require readout electronics integrated into the detector. The large channel count of the detectors means that the individual readout devices like the Detector Interface cards, DIF, need to handle a large number of detector channels and many readout ASICs and have to respect the space and power constraints due to their location within the detector volume. DIF cards for two hadron calorimeter prototypes for Linear Collider detectors, the SDHCAL and the AHCAL have been developed. For the SiW ECAL a new DIF system, consisting of four cards has been designed and produced. The boards will be tested using the developments of a data acquisition system done in WP5.

1. INTRODUCTION

Calorimeters for Linear Collider detectors can have up to 100M readout cells. The number of digital readout devices has to be small to be able to fulfil space and hermiticity constraints in collider detectors, requiring that the individual components such as Detector InterFace cards, DIF, have to serve up to 10,000 calorimeter cells. DIF cards, optimised in size and power consumption, are developed. The first step was the definition of the interfaces and the DIF design, documented in milestone report M58 [1]. In this report the design and production of prototype boards of the DIF for the Analog Hadron Calorimeter, AHCAL, and the Semi-Digital Hadron Calorimeter, SDHCAL are discussed. The DIF system development for the SiW ECAL has led to the development of three boards which have been produced. These boards were particularly challenging to develop because of the tight space constraints in the SiW ECAL.

While the detector technology is different for AHCAL, SDHCAL and SiW ECAL, the front end electronics for all detectors come from the ROC family tailored to the individual needs (SPIROC [2], HARDROC [3] and SKIROC [4]). The developments of Aida WP5 (DAQ), such as the Trigger-Logical-Unit (TLU) and EUDAQ2 are important ingredients for the tests and combined running of the detectors.

2. AHCAL DIF

The AHCAL is a hadronic sampling calorimeter concept based on 3*3 cm$^2$ scintillator tiles individually read out by Silicon Photomultipliers (SiPMs). The absorber consists of steel or tungsten, with a thickness of about 0.1 nuclear interaction length, corresponding to 1.7 cm for steel or 1 cm for tungsten.

2.1. DESIGN OF THE AHCAL DIF

The AHCAL DIF is one of three interface boards that connect an active layer of the AHCAL to the DAQ and external power supply: the DIF providing the DAQ interface, the POWER board providing the interface to the power supply, and the CALIB board providing the functionalities for the LED calibration system. A set of mostly passive interface boards (Central Interface Board CIB and Side Interface Board SIB) hosts the DIF, POWER and CALIB boards and provides the connection to the front-end boards, the HBUs (Hcal Base Unit).

The AHCAL DIF can handle up to 18 HBUs, arranged in 3 slabs of 6 HBUs connected in series. The DIF controls up to 72 SPIROC2 [2] readout ASICs with up to 2592 readout channels. The
communication is split into 6 parallel open collector lines (2 per slab), handling a maximum of 12 ASICs each.

The AHCAL DIF connects to the DAQ system via an intermediate board, the Link Data Aggregator (LDA). The communication between the LDA and the connected DIFs is handled on HDMI cables with a custom communication protocol. The DIF receives the ASIC configuration data and local DAQ commands from the LDA, and sends the data collected from the ASICs to the LDA. For debugging purposes a USB2 interface is provided. The USB connector is located on the DIF, while the HDMI connector is housed on the CIB. The AHCAL DIF receives a common 40 MHz clock from the LDA by a dedicated line pair on the HDMI connection, and derives the 5 MHz slow clock that is needed for the SPIROC2 ASICs. For debugging purposes, it can also generate these clocks. The AHCAL DIF houses a Xilinx Zynq XC7Z020-1CLG484I that includes an FPGA and an ARM9 microcontroller. More details about the architecture and operation of the AHCAL DIF can be found in [5].

To meet the compactness requirements of the ILD detector, the AHCAL DIF is limited in size to 9.4 x 8.1cm². The total height of CIB, DIF and external cooling plate is limited by a layer spacing pitch of 1.8 cm (see figure 1 left). This pitch is compatible with an absorber thickness of 1 cm, the preferred thickness for an AHCAL with tungsten absorber. For steel, the absorber plates are about 7-9 mm thicker, leading to less stringent space restrictions.

A series of 50 AHCAL DIFs has been produced and successfully used in tests in particle beams and in the lab (see Fig. 1 right).

2.2. BEAM AND LABORATORY TESTS OF THE AHCAL DIF

For a large prototype of the AHCAL, 38 modules consisting 2*2 HBUs, an SIB and a CIB hosting DIF, POWER and CALIB board have been built. They have been installed in a steel absorber structure, together with a cooling system (see Fig. 2 left). The DIFs were all connected to the same LDA, and the central 40 MHz clock was provided by a Clock and Control Card (CCC). Each of the DIFs had to handle the data of 16 SPIROC2E ASICs with 576 readout channels. In total the
AHCAL prototype had ~22000 channels. The prototype was exposed to muon, electron and pion beams at the CERN SPS for several weeks in 2018, and collected several $10^7$ events. The prototype was tested in a mode were the ASICs are powered continuously and also in power pulsing mode, in which the parts of the ASICs are switched off during the times when they are not needed. Both operation modes were stable, and no problems with the DIFs were observed. The readout speed was fulfilling the requirements. During data taking of beam events, no limitations due to the data throughput of DIF or LDA were observed. During LED calibrations, where the maximum data volume and rate is reached, the readout was limited by the LDA, not the DIFs. The limitation of a maximum bandwidth of about 6 MB/s for the TCP data transfer was due to a non-optimised handling of the direct memory access (DMA) in firmware and software of the LDA. This DMA handling is being improved now, and a factor of 10 in LDA bandwidth looks achievable.

The beam tests of the AHCAL prototype included two weeks of combined running with a prototype of the silicon part of the CMS HGCAL. In this configuration, the handling of the central signals is done by the HGCAL SYNC board. The common data taking was operated with EUDAQ2.0. Also during this time the operation was stable and reliable. Due to limitations of the HGCAL prototype, the readout speed was lower than in the AHCAL stand-alone runs, and the operation was less challenging for the DIFs.

![Fig. 2 View of 38 AHCAL layers installed in a steel absorber stack for beam tests (left). The interface boards including the DIFs extend beyond the absorber structure and are covered from view by copper cooling plates. Test of a large AHCAL layer with 2 slabs of 6 HBUs each, connected to one set of interface boards (right)](image)

A test of a large AHCAL layer up to the maximum size of 3*6 HBUs has started in the lab. So far, 2 slabs of 6 HBUs, corresponding to 48 ASICs with 1728 channels, have been operated (see Fig. 2 right). Such a large configuration can only be operated safely in power pulsing mode, otherwise the power consumption would be too high and heat up the electronics too much. The DIF firmware has
been modified to enforce the constraints needed to limit the power consumption to a sustainable level. The operation was stable, and no limitations from the DIF were observed. In the coming months, the setup will be enlarged to one layer of 3 slabs with 6 HBUs each. As next step, the operation of 3 or 4 large layers with 3 slabs each is planned.

3. **SDHCAL DIF**

The SDHCAL is a calorimeter using Glass Resistive Plate Chamber (GRPC) as active medium. The front-end chip used to read out the GRPC is called HARDROC [3]. It provides a semi-digital readout. Its DIF is designed to be the interface board between the ASU board (Active Sensors Unit) that embeds all required HARDROC3 ASICs and the DAQ software.

The SDHCAL DIF controls the ASIC configuration through redundant I2C, performs the ASIC readout and sends data to the DAQ software according to the global detector finite state machine.

The SDHCAL DIF can handle 432 HARDROC3 ASICs (for a 1m x 3m detector). For speed and reliability reasons, communication with the ASICs has been split into 12 parallel lines each serving a maximum of 36 ASICs. For each line, ASIC configuration and ASIC readout are on separated dedicated lines (both doubled for reliability purpose, two I2C busses for configuration and two open collector serial links for data readout).

A block diagram representing all functionalities of the SDHCAL DIF is shown in Figure 3a.

![Figure 3a: The block diagram of the SDHCAL DIF is shown](image)

The SDHCAL DIF is developed with both a FPGA and a microcontroller unit (MCU) to ensure communication with both ASICs and DAQ software (Ethernet link).
The SDHCAL DIF receives clock and synchronous commands from the central detector system through a TTC (CERN standard Time, Trigger and Control used at the LHC) optical link. This ensures that all ASICs are in phase and take data at the same time. The hardware of the TLU developed in WP5 can output a TTC signal for which the firmware would have to be written.

The SDHCAL DIF receives all ASIC configuration data and local DAQ commands from a local Ethernet interface. In the same way, data coming from the ASICs are sent to the DAQ software through the Ethernet interface.

A USB2 interface is integrated for debugging purposes.

The SDHCAL DIF has to take into account several constraints: To meet the compactness requirements of the ILD detector, the SDHCAL DIF has to occupy the narrowest possible space and be as close as possible to each ASIC line. Therefore, it has been designed to measure 70 cm x 6 cm.

All connectors to ASICs have to be on the same side of the detector. The DIF provides low voltage to all ASICs with which it communicates. The peak power consumption of all ASICs has been estimated to 93W. As the ASICs can be power pulsed (to limit power consumption, ASICs are partially powered down between spills), the DIF embeds a super-capacitor to be able to provide the peak power when needed with a limited global power budget.

A picture of the SDHCAL DIF board is shown in Figure 3b.

A picture of the SDHCAL DIF board is shown in Figure 3b.

All the functionalities of the SDHCAL DIF board have been tested, except power pulsing that will be tested in a near future.

The next step is to develop the definitive firmware, which is an advanced state.
Tests of ASICs configuration (using both I2C busses, primary and redundant) have been run with two ASU boards.

4. **SIW ECAL System**

The concept of the SiW ECAL calls for up to 13 ASUs to be configured, supplied with low voltage and read out via the DIF system. Each of the ASUs is equipped with SKIROC [4] chips for a total of 1024 channels. The DIF system consists of three boards:

1. The SLab digital interface board (SL-Board) which is connected to the last ASU of the serially connected ASUs.
2. The Control & Readout Kapton (CORE Kapton) which connects the SL-boards of slabs to the Control and Readout (CORE) module.
3. The CORE Module which consists of the detector specific CORE daughter board mounted on the generic CORE mother board.

In e.g. the ILD Detector the SL-Board is to be installed between the ECAL and the HCAL, which are separated by only 67 mm including 25 mm of mechanical tolerance. In the other dimension, the DIF has to be less than 70 mm in size, as the cooling of the detector electronics takes up the remaining space. The CORE Kapton connects the SL-boards to the CORE Module from the smallest to the largest radii with respect to the beam axis.

A conceptual diagram of the system describing the links between the different boards is shown in Figure 4a.

![Diagram of the DIF system for the SiW ECAL](image)

*Fig. 4a: The DIF system for the SiW ECAL is shown with the SL-board, CORE Kapton and the CORE Module consisting of the CORE mother board with the CORE daughter board is shown.*

4.1. **SL-BOARD**

The SL-Board is the digital interface board situated at the extremity of a slab consisting of up to 13 ASUs.
The SL-board respects the daunting space constraints for operation e.g. in ILD. It is designed for low power consumption and good signal integrity. High versatility for testing and debugging of the board and the detector was taken into account in the definition of its functions.

The SL-Board handles:

1. Control & readout of the chained ASUs, thus communicating with the SKIROC chips on the ASU.
2. Interface to the CORE acquisition module through a kapton cable. It is a rigid PCB on the slab side with a flex part on the CORE side.

The SL-board is designed around an Altera MAX10 mixed CPLD/FPGA low power technology. It is equipped with a 40 MHz oscillator and a remote USB interface. This allows standalone control of the slab. Testing of the slab interface and the communication through the CORE Kapton is possible without running the central DAQ.

The printed circuit board (PCB) routing of the SL-Board is shown in Figure 4b.

![Figure 4b: The PCB routing of the SL Board is shown.](image)

The PCB is 180 mm wide. The central part is only 10 mm in depth to leave place for the cooling of the ASUs (WP14.5). The main part at the left of Figure 4b is 42 mm in depth and 70 mm in width. Its thickness is 1.6 mm with 10 layers, including 2 layers of flex. The fully equipped SL-Board is shown in Figure 4c.
The SL-Board is connected to the ASU via a 35-pin 1 mm pitch GradConn connector (reference BB02-YN351-KB3-150000) of height 1.5 mm.

The CORE Kapton is at an angle of 45° with respect to the SL-Board. As standard connectors provide a board to board connection of either 90° or 180°, the SL-Board provides a flex extension of 40 mm in length for the connection. The connector located on the flex is of type BERGSTAK 2x20 pins, 61082 series, 0.8 mm pitch. Its 40 pins transmit 7 differential pairs for sensitive signals, including two pairs for data readout and flow control, 11 unipolar signal lines, a few spare lines (both differential and unipolar) and 8 pins of ground (GND).

4.2. **CONTROL & READOUT KAPTON AND CORE-MODULE**

The CORE Kapton connects the SL-Board to the CORE-Module. As described in the introduction, it is a rigid board on the SL-Board side and has a flex part on the other side to reach the CORE-Module on the top of the detector which is at an angle of 45°.

The connection to the SL-Board is a 40-pin BERGSTAK connector of the opposite sex (type 61083) of that described in Section 4.1. On the CORE-Module side a 100-pin connector of type HIROSE FX18-100P-0.8SH is used. The rigid part can connect up to 15 SL-boards, each of which has its individual flow control and readout differential lines in addition to the common lines.

The PCB layout of the board is shown in Figure 4d.
The board has been produced and assembled. A picture is shown in Figure 4e.

Fig. 4d: The PCB layout of the CORE Kapton is shown.

Fig. 4e: The CORE Kapton is shown.

The CORE-Module is based on a mother board which was developed at LAL for fast waveform digitizers. The CORE-Mother provides the following functionalities: interface to the DAQ (USB and Gbit UDP, both copper and optical), reception and transmission of the DAQ clock, delivery of adequate power supplies.

The CORE daughter board was developed specifically for this project. It is connected to the CORE Kapton flex via a connector of type HIROSE FX18-100S-0.8SH. Its PCB routing is shown in Figure 4f. Its role is mainly the transmission of clock and fast signals to the SL-Boards, the collection of event data, and the control of detector electronics. Event data travels in parallel on individual differential lines on the CORE Kapton and is grouped on an event-by-event basis on the CORE daughter board, before being transmitted to DAQ.

Fig. 4f: The layout of the CORE daughter board is shown.
The CORE daughter board has been built, assembled and mounted on the CORE-Mother as shown in Figure 4g top slot of the motherboard. The bottom slot is empty and one can see the board-to-board 100-pin connector.

![CORE daughter board](image)

**Fig. 4g: The CORE module is shown**

### 4.3. Tests

The following tests have been performed on the SL-Board:

- Power supplies
- JTAG programming
- USB communication
- Interconnection with the ASU
- ADC internal to Altera MAX10
- Test of interconnection ok

None of the tests have revealed a problem.

The firmware development is ongoing. The first step is the interface with the ASU for controlling and reading out the SKIROC ASICs. The second step will be the interface with the CORE Module via the CORE Kapton. The corresponding test bench software is also being developed in parallel. The C access functions will be integrated in the DAQ software environment (PYRAME) used for the detector characterization.
5. FUTURE PLANS / CONCLUSION / RELATION TO OTHER AIDA-2020 WORK

Extensive work has been performed on the DIF systems of the AHCAL, SDHCAL and SiW ECAL. The systems have been built with an emphasis on respecting the challenging spatial constraints of usage in a detector such as ILD.

The firmware of the systems is being developed. In the future beam tests and combined beam tests with these system can be performed using the developments of WP5, the AIDA2020-TLU and EUDAQ2 in particular, to further validate the systems.
6. REFERENCES


## ANNEX: GLOSSARY

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<tr>
<td>ASU</td>
<td>Active Sensor Unit: basic detector unit</td>
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<td>DIF</td>
<td>Detector InterFace between the active detector layers and the DAQ</td>
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<tr>
<td>HBU</td>
<td>HCAL Base Unit: basic detector unit in the AHCAL</td>
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<tr>
<td>SL-board</td>
<td>Slab digital interface board for control and readout of the ASUs</td>
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<td>CORE Kapton</td>
<td>Control and Readout Kapton connecting the SL-board to the Core module</td>
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<tr>
<td>CORE-Module</td>
<td>Motherboard plus detector specific daughter board handling control and readout connected</td>
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<td>to the Control and Readout Kapton</td>
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<td>PYRAME</td>
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