Development of a Power Quality Conditioning System for Particle Accelerators

A Voltage Dip Mitigation System based on Back-to-Back HVDC Converter Topology

Tony Endré Slettbakk

Bachelor in Electrical Engineering
Submitted: 28.12.2018
Supervisor: Ian Norheim, IEL
Co-supervisor: Thomas Höhn, CERN

Norwegian University of Science and Technology - IEL
The European Organization for Nuclear Research - CERN
Title of thesis: Development of a Power Quality Conditioning System for Particle Accelerators

Subtitle: A Voltage Dip Mitigation System Based on Back-to-Back HVDC Converter Topology

Date: 28.12.18
Number of pages: 110
Number of appendices: 6

Master’s thesis X Bachelor’s thesis

Name: Tony Endré Slettbakk
Supervisor: Ian Norheim, NTNU
External contacts/ supervisors: Thomas Hohn, CERN. Karsten Kahle, CERN.

Keywords:
- Power Quality Conditioning
- Modular Multilevel Converter
- Transient Voltage Dips
- HVDC Technology
- Particle Accelerators
- CERN

Tony Endré Slettbakk
Abstract

CERN is frequently experiencing power quality problems caused by transient voltage dips originating from the outside grid, causing issues with electrical equipment and, in the worst case, tripping the particle accelerators. This thesis will prove the feasibility and develop a power quality conditioning system to mitigate these voltage dips to ensure satisfactory power quality for CERN today, and in the future for even larger particle accelerators. The mitigation system is based on the back-to-back HVDC converter concept and, as the nature of the electrical network of CERN is entirely passive, the converter is operating as a remote-end converter. The purpose of this converter is to supply constant power during voltage dips occurring in the upstream network, and thus, completely decouple CERN from the grid. The topology of choice is concluded to be the HVDC modular multilevel converter, which has the added benefits of being able to connect to weak AC networks. In addition, it possesses reactive power support, low harmonic distortion as well as high modularity and reliability. This thesis has further categorised two mitigation strategies with the back-to-back converter: Increased line-current control and energy storage support, with the latter one being the primary focus. This is based on incorporating the energy storage in the converter topology by proper dimensioning of submodule capacitors. A statistical analysis of voltage dips is performed, optimising the energy storage for reduced investment costs. Furthermore, the system is designed for the electrical network of CERN, identifying optimal location and operational parameters. The converter is designed down to component-level and important aspects in the design are highlighted. The system is simulated with MATLAB & SIMULINK and the feasibility of the control system, dip mitigation and extra features is proven. The reliability of the designed submodule is reviewed, and the footprint of the converter is investigated. The total cost of the converter is estimated and cross-referenced with literature, and a net-present value analysis is performed based on the economic gain for CERN to employ such a system for the Large Hadron Collider. The thesis is finalised by reviewing the possible applications for the power quality conditioning system in the industry outside of CERN.
Preface

This bachelor’s thesis was carried out during my time at CERN in Geneva, Switzerland as a technical student, working in the power converters group from February 2018 until January 2019. The thesis is part of the 30 credits course "Bachelor Thesis CERN" at the Norwegian University of Science and Technology. A technical seminar for the power converters group at CERN were held 6th of December 2018, presenting the main topics of the thesis. Throughout my thesis work I have learned so much about everything from power electronics and electrical engineering, to how particle accelerators work and the activities at CERN. My year at CERN has been an incredible experience, which I will treasure forever.

First of all I want to give my greatest gratitude to Thomas Höhn, my supervisor at CERN, for all the nice discussions we’ve had and for the support throughout the thesis work, you have simply been wonderful! I want to thank Karsten Kahle and Francisco Blanquez for giving me the opportunity to work with this incredibly interesting project, and for helping me throughout my time at CERN and with the thesis project. It has given me great challenge and I have learned so much. I also want to express my heartfelt gratitude to my girlfriend Birte, for encouraging me throughout my studies and for help in proof-reading my thesis. I want to thank Ian Norheim, my supervisor at NTNU, for the guidance during the writing process, and for reviewing of my thesis. Lastly I want to thank my colleagues at CERN for making my time abroad amazing, and to my friends and family for all the support throughout the year.
Contents

List of Figures xiii
List of Tables xv
Abbrevations xvi

1 Introduction 1
  1.1 CERN and the Accelerator Complex ........................................ 1
  1.2 Transient Voltage Dips .................................................... 2
  1.3 Objectives and Scope of Thesis ........................................... 4

2 HVDC Converter Topologies 7
  2.1 High Voltage Direct Current .............................................. 7
     2.1.1 HVDC Configurations ............................................... 8
     2.1.2 HVDC for Passive Network ......................................... 9
     2.1.3 HVDC Guidelines .................................................. 10
  2.2 Current Source Converters ................................................. 11
     2.2.1 The Thyristor ...................................................... 11
     2.2.2 Line-commutated Converter ....................................... 12
     2.2.3 Capacitor Commutated Converter .................................. 13
  2.3 Voltage Source Converters ................................................ 14
     2.3.1 The IGBT ........................................................... 15
     2.3.2 Two-level Converter ............................................... 15
     2.3.3 Cascaded H-bridge Converter ..................................... 16
  2.4 Discussion and Conclusion ............................................... 17

3 Modular Multilevel Converter 21
  3.1 Back-to-Back MMC ........................................................ 21
     3.1.1 Reference Projects .................................................. 22
  3.2 Mathematical Model of MMC .............................................. 23
     3.2.1 Fundamental Operation of the Submodule ......................... 24
     3.2.2 AC and DC Side Interactions ..................................... 25
3.2.3 Upper and Lower Arm Dynamics ........................................ 26
3.2.4 Circulating Dynamics Between Arms ................................. 29
3.3 Capacitor Balancing Strategy .............................................. 30
3.4 Modulation Strategy .......................................................... 32
3.5 Control System .............................................................. 35
  3.5.1 Control in Synchronous Reference Frame ......................... 35
  3.5.2 Outer Voltage Loops ................................................ 36
  3.5.3 Inner Current Loop ................................................ 38
  3.5.4 Circulating Current Suppression Control ......................... 39

4 System Design .................................................................. 41
  4.1 Energy Storage Considerations ......................................... 41
     4.1.1 Dip Mitigation Strategies ........................................... 42
     4.1.2 Analysis of Voltage Dips ............................................ 43
     4.1.3 Energy Storage Calculations ...................................... 46
  4.2 System Level Parameters .................................................. 49
     4.2.1 CERN Electrical Network .......................................... 49
     4.2.2 Voltage Level Considerations ..................................... 50
     4.2.3 Converter System Parameters ..................................... 52
  4.3 Converter Component Design ............................................. 54
     4.3.1 Submodule Switching Devices ..................................... 54
     4.3.2 Submodule Capacitor ............................................... 57
     4.3.3 Arm Inductance ..................................................... 58
     4.3.4 Gate Driver and Auxiliary Power .................................. 59
     4.3.5 Cooling and Mechanical Equipment .............................. 59
  4.4 Fault Operation and Handling ............................................ 60
     4.4.1 AC Grid Fault ....................................................... 61
     4.4.2 Load Network Fault ................................................ 61
     4.4.3 Active Bypass System .............................................. 62
     4.4.4 Submodule Bypass System ........................................ 63
     4.4.5 Submodule Fault .................................................... 64
     4.4.6 DC-bus Fault ......................................................... 64
  4.5 Transformer-independent Converter ................................... 65
     4.5.1 Transformer-less Connection ...................................... 65
5 Simulation Studies 67
  5.1 Simulation Model ................................................. 67
    5.1.1 Matlab & Simulink ........................................ 67
    5.1.2 Aggregate MMC Model ....................................... 67
    5.1.3 Simulation Parameters ...................................... 69
  5.2 Converter Start-up and Operation ................................. 70
    5.2.1 Steady State Operation ..................................... 72
    5.2.2 Controller Responses ........................................ 73
  5.3 Voltage Dip Mitigation Feasibility ............................... 74
    5.3.1 Three-Phase Dip Mitigation ................................. 75
    5.3.2 Single-Phase Dip Mitigation ................................. 79
  5.4 Power Quality Feasibility ........................................ 82
    5.4.1 Total Harmonic Distortion ................................. 82
    5.4.2 Reactive Power Support ...................................... 84
    5.4.3 Circulating Current Suppression ............................ 86

6 Techno-Economical Studies 89
  6.1 Reliability Analysis .............................................. 89
  6.2 Footprint Estimation .............................................. 92
  6.3 Converter Cost Estimation ....................................... 94
  6.4 Economic Evaluation .............................................. 99
  6.5 Further Applications ............................................. 102

7 Conclusion and Future Work 105
  7.1 Conclusion ..................................................... 105
  7.2 Future Work .................................................... 106

References 107

A dq0-Transformation Theory 111

B Voltage Dip Measurement Data 113

C Economical Analysis of LHC Availability 114

D MATLAB & SIMULINK Models and Scripts 118
  D.1 Matlab Scripts ................................................ 118
  D.2 Simulink Model ................................................. 121

E CERN Distribution Network 134

F Footprint Estimation 136
List of Figures

1.1 The CERN accelerator complex. ............................................ 2
1.2 Measured voltage dips during last 5 years resulting in loss of physics. ... 3
2.1 Commonly used HVDC system configurations. ............................... 9
2.2 Back-to-back HVDC connected as a remote-end converter. ................. 10
2.3 Fundamental operation of a single-phase half-wave thyristor rectifier. .... 12
2.4 The twelve-pulse thyristor converter. ......................................... 13
2.5 The capacitor-commutated converter concept. ................................ 14
2.6 The two-level Voltage source converter. ....................................... 15
2.7 Full-bridge and half-bridge configuration. ...................................... 16
3.1 The principle of the back-to-back MMC system for a passive load. .......... 22
3.2 Detailed look into the MMC in the back-to-back configuration. ............. 22
3.3 MMC converter arm and fundamental operation of submodule. .............. 24
3.4 MMC converter dynamics - Equivalent model. .................................. 27
3.5 Process for controlling the modular multilevel converter. .................... 30
3.6 Phase-shifted carrier waves in pulse width modulation. ...................... 33
3.7 Phase-dispositioned carrier waves in pulse width modulation. .............. 33
3.8 Nearest level modulation strategy for a 5-level MMC. ....................... 34
3.9 DC voltage controller for the rectifier. ....................................... 36
3.10 AC voltage controller for the inverter. ....................................... 37
3.11 AC voltage controller for the rectifier. ....................................... 38
3.12 Reactive power controller for inverter. ...................................... 38
3.13 Inner current loop control in synchronous reference frame. ................. 39
3.14 Circulating current suppression controller in dq0 frame. .................... 40
4.1 Statistical representation of voltage dip measurements. ...................... 45
4.2 Measured voltage dips and the dip severity visualised. ...................... 46
4.3 Energy of a capacitor as a function of voltage. ............................. 47
4.4 Voltage dip mitigation capability based on installed system energy. ......... 48
4.5 Electrical distribution network feeding the LHC machine. ................... 49
4.6 The LHC machine network with the BTB HVDC system to be studied. ....... 51
4.7 Overview of converter and network system parameters. 53
4.8 Detailed overview of the MMC submodule. 54
4.9 Fault scenarios in the BTB HVDC converter. 60
4.10 The static thyristor AC switch for bypassing the converter. 63
4.11 Zero sequence current controller - Using PR regulator. 66

5.1 Detailed control system model - Overview. 70
5.2 Converter start-up and energising. 71
5.3 Start-up resistors for charging of the converter. 72
5.4 Steady state operation of the submodule voltage and current. 73
5.5 Response of outer loop controllers. 74
5.6 Ideal voltage dips - Visualisation. 75
5.7 Consequence of voltage dip without a mitigation system. 75
5.8 Three-phase voltage dip - Voltage, power and energy dynamics. 77
5.9 Three-phase voltage dip - Inverter output AC voltage. 78
5.10 Three-phase voltage dip - dq0 measurements and modulating index. 78
5.11 Single-phase voltage dip - Voltage, power and energy dynamics. 80
5.12 Single-phase voltage dip - Inverter output AC voltage. 81
5.13 Single-phase voltage dip - dq0 measurements and modulating index. 81
5.14 Harmonics in inverter output voltage with nearest level modulation. 83
5.15 Enhanced reactive power support for load network. 84
5.16 Reactive power support from inverter - Simulation. 85
5.17 Circulating current suppression controller (CCSC) feasibility. 87

6.1 Fault tree analysis for the submodule. 90
6.2 The various MMC applications identified today. 103

A.1 dq0 transform showcased in stationary abc-frame. 112

C.1 LHC beam operation cycle and consequence of beam dump. 116

D.1 to D.21 - Simulink simulation models. 122

E.1 Electrical distribution network feeding the LHC machine. 134
E.2 Complete electrical distribution network of CERN. 135

F.1 Mackinac BTB HVDC converter station footprint. 136
F.2 Proposed MMC submodule rack configuration and dimensions. 137
List of Tables

2.1 Comparison of HVDC converter topologies. .......................... 19
3.1 Existing HVDC reference projects using VSC technology. .......... 23
3.2 Operation of SM based on switch states. .......................... 25
4.1 Parameters for the LHC machine network at CERN. ................ 50
4.2 Nominal and derated voltage rating of industrial IGBTs. .......... 55
4.3 Industrial ratings for wire-bond IGBT modules. .................. 57
4.4 Industrial capacitor standards for MMC application. ............ 58
4.5 Fault states of the submodule and detection method. ............ 64
5.1 Converter start-up process in simulation. .......................... 72
5.2 Total harmonic distortion (THD) simulation results. ............ 82
5.3 Reactive power support - Load demand in simulation. .......... 85
6.1 Failure rate for the critical components in the submodule. .......... 91
6.2 Failure rate calculation results based on maintenance period. .......... 92
6.3 Estimated costs of the individual submodule. .................. 96
6.4 Estimated total system cost for the converter station. ........... 98
6.5 Summary of cost estimation methods for the back-to-back system. ........ 99
6.6 Net Present Value analysis for the proposed system. ........... 101
B.1 Measured voltage dips at CERN. ................................. 113
C.1 Availability data of the LHC for 2016 and 2017. ................ 117
# Abbreviations

<table>
<thead>
<tr>
<th>Abbreviation</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>BTB</td>
<td>Back-to-back</td>
</tr>
<tr>
<td>CCC</td>
<td>Capacitor-commutated converter</td>
</tr>
<tr>
<td>CCSC</td>
<td>Circulating current suppression system</td>
</tr>
<tr>
<td>CERN</td>
<td>The European Organization for Nuclear Research</td>
</tr>
<tr>
<td>CSC</td>
<td>Current source converter</td>
</tr>
<tr>
<td>Dq0</td>
<td>Direct quadrature zero</td>
</tr>
<tr>
<td>DSRF</td>
<td>Dual synchronous reference frame</td>
</tr>
<tr>
<td>FCC</td>
<td>Future circular collider</td>
</tr>
<tr>
<td>FIT</td>
<td>Failure in time</td>
</tr>
<tr>
<td>HVDC</td>
<td>High voltage direct current</td>
</tr>
<tr>
<td>IGBT</td>
<td>Insulated gate bipolar transistor</td>
</tr>
<tr>
<td>LCC</td>
<td>Line-commutated converter</td>
</tr>
<tr>
<td>LHC</td>
<td>Large Hadron Collider</td>
</tr>
<tr>
<td>MMC</td>
<td>Modular multilevel converter</td>
</tr>
<tr>
<td>NLM</td>
<td>Nearest level modulation</td>
</tr>
<tr>
<td>NPV</td>
<td>Net present value</td>
</tr>
<tr>
<td>PCC</td>
<td>Point of common coupling</td>
</tr>
<tr>
<td>PLL</td>
<td>Phase locked loop</td>
</tr>
<tr>
<td>PQCS</td>
<td>Power quality conditioning system</td>
</tr>
<tr>
<td>p.u</td>
<td>Per unit</td>
</tr>
<tr>
<td>PWM</td>
<td>Pulse width modulation</td>
</tr>
<tr>
<td>SC</td>
<td>Short circuit</td>
</tr>
<tr>
<td>SCR</td>
<td>Short circuit ratio</td>
</tr>
<tr>
<td>SM</td>
<td>Submodule</td>
</tr>
<tr>
<td>SRF</td>
<td>Synchronous reference frame</td>
</tr>
<tr>
<td>THD</td>
<td>Total harmonic distortion</td>
</tr>
<tr>
<td>TSO</td>
<td>Transmission system operator</td>
</tr>
</tbody>
</table>
Chapter 1

Introduction

1.1 CERN and the Accelerator Complex

The European Organisation for Nuclear Research (CERN) is the largest organisation in the world focused on particle physics. It is located in Geneva, Switzerland and operates on the border between Switzerland and France. CERN has 22 member states who all contribute to the operation of the laboratory and the scientific research that is being conducted. The main objective of CERN is to study the properties of particles through high-energy physics experiments. To do this, CERN operates an accelerator complex consisting of several machines. The flagship of CERN, the Large Hadron Collider (LHC) is a circular collider with a circumference of 27 km located 100 meter underground. It is the largest particle accelerator ever built and it collides particles at an energy of 13 TeV. The construction of LHC started in 1998 and it was finished in 2008 through a huge global collaboration. It is connected to the accelerator complex through a succession of machines, each accelerating particles to a higher energy until they reach LHC and collide there, creating an explosion of particles of which scientific data is recorded and analysed.

The particles start in the linear accelerator, LINAC, where they are taken from a hydrogen source. The electrons are removed and only the proton is accelerated to an energy of 50 MeV before being fed to the next step in the chain, the Booster. Here the protons are accelerated to an energy of 1.4 GeV before they are injected into the Proton Synchrotron (PS). Its job is to accelerate the protons to an energy of 25 GeV. From here, the next step in the chain is the Super Proton Synchrotron (SPS), measuring 7 km, which accelerates the protons up to 450 GeV. After this, the protons are injected into the LHC in two groups, going clockwise and anti-clockwise, there they are accelerated to almost the speed of light. They gain an energy up to 6.5 TeV before being collided head-on with the other beam rotating in opposite direction, essentially creating a collision with twice the energy.
CERN operates several large detectors called ATLAS, CMS, ALICE, and LHCb. These are the machines that record and analyse the results of the collisions happening in the LHC. Each of the detectors is intersecting the beam pipe of the LHC in large underground cavities. Here they have access to their own particle collisions where they record data. ATLAS and CMS are the general purpose detectors, which was constructed to achieve the same goal using different strategies. This way, the real results will be mutual for both detectors and the real discoveries can be validated by both. The accelerator complex of CERN is presented in figure 1.1, showing the chain of accelerators, the detectors and the largest experiments at CERN [1].

Figure 1.1: The CERN accelerator complex [1].

1.2 Transient Voltage Dips

Transient voltage dips are a big topic for the industry today, as they can disturb sensitive electrical loads and in the worst case cause an interruption of production. Transient voltage dips are categorised mainly by two parameters: The magnitude of change in the voltage, and the duration of the dip. The official definition of a voltage dip defines it as the event when the magnitude is reduced under the threshold of 10% of nominal value over the duration ranging from one half-cycle to several minutes [2]. A typical voltage dip can affect several phases, and as such, the dip magnitude is defined as the most severe reduction in RMS amplitude in any of the phases, with respect to ground. The duration
is defined as the time the magnitude is below the magnitude threshold. After several minutes of duration, the event will be categorised as under voltage. The definition of a voltage dip must be separated from the definition of short interruption, which is the case when the magnitude of the voltage is zero, or relatively close to zero.

The origin of voltage dips is normally related to sudden switching of loads, line faults and lightning strikes, with the latter one being the most frequent cause in the industry. When the lightning strikes near or at overhead lines it can cause short-circuits between phase(s) and ground, reducing the voltage for a short duration. This reduced voltage will propagate through the lines downstream and reach load-centres, potentially causing issues. CERN is connected to the transmission network of France and Switzerland, operating at 400 kV and 220 kV. As CERN inhibits very sensitive electrical loads, such as power converters and cryogenics, voltage dips can from time to time cause operational interruptions. The accelerators at CERN operate under extreme requirements for precision, and once a disturbance related to the control and operation is detected, it will be forced into safe operation by dumping the particle-beam out of the accelerators. This causes downtime in production of science and decreases the availability of the accelerators.

Figure 1.2 shows all the voltage dips that have caused a major event at CERN during the last five years of operation. A major event is defined as when an accelerator in the accelerator-chain is tripped. The majority of voltage dips measured at CERN is in the range within -50% magnitude and 150 ms. This is classified as the design-range of the potential power quality conditioning system. The duration for these dips is mostly less than 100 ms; this is caused by the employed time selectivity of relays and protections in the overlying transmission network. Once a voltage dip has been sustained for the selected time selectivity, relays will disconnect the compromised line and the system will revert back to a healthy state.

Figure 1.2: Measured voltage dips during last 5 years resulting in loss of physics.
1.3 Objectives and Scope of Thesis

As transient voltage dips are of great concern for CERN, the study of a power quality conditioning system able to mitigate these voltage dips is of great importance. This system will increase the availability of today's particle accelerators, as well as future accelerators of even larger dimensions.

Today, power converters and other equipment of the machines are designed to function with a small variation of voltage that can appear in the distribution grid. Only some of the converters are designed with internal energy storage to be immune to voltage dips. This type of design is called dip mitigation at equipment level, and it increases the complexity, efficiency and economic aspects of the equipment itself. With the need for protecting all sensitive equipment from voltage dips, there are great potential in concepts that can be specifically designed to mitigate transient voltage dips for an entire electrical network. This is called dip mitigation at system level. CERN has identified three possible concepts for this purpose. What is common for every concept is the very fast response speed, which is required for precise mitigation of the transient voltage dips. The concepts are as follows: The back-to-back HVDC converter, the dynamic voltage restorer, and the DC distribution grid.

Objectives

The objectives of this thesis is to explore the concept and feasibility of the back-to-back HVDC converter as a power quality conditioning system, used for mitigating voltage dips and ensuring satisfactory power quality. This includes the following:

- Feasibility study and proof of concept for the back-to-back HVDC system for power quality conditioning applications. This includes literature review to identify the most promising topology for this application.

- Detailed system design and definition of main component ratings for application in the LHC network.

- Development of a simulation model with a high-performance control system, and performing a case study for such a system feeding the Large Hadron Collider.

- Techno-economical estimations for the proposed converter of the case study.

The feasibility of the system is to be proven through simulation studies, showing a high-performance control system and the functionality of dip mitigation and quick response of the system. The design-range for mitigation of dips is pre-defined as: All three-phase dips of up to -50% magnitude and up to a duration of 150 ms. This design-range is identified
by CERN based on Figure 1.2. Later in the studies, the design range is re-evaluated to be smaller based on statistical calculations.

**Chapter 2** will explore the concept of HVDC technology, including the different configurations such as back-to-back, and how such a system would be applied to an industrial distribution network. The converter topologies used for HVDC are reviewed based on their features and applications, and the chapter will finally conclude the most suited topology for further development of the power quality conditioning system.

**Chapter 3** is going to delve into the mathematical model and representation of modular multilevel converters. It will explain the operation of the MMC in a back-to-back configuration, as well as explain the consideration for capacitor voltage balancing, and the different modulation strategies available. The chapter will end by presenting the control objectives and how the control loops are designed based on synchronous reference frame.

**Chapter 4** will look into the practical aspects of the power quality conditioning system with focus on component design and selection, voltage dip mitigation strategies and energy storage dimensioning. The electrical network of CERN is presented, and after identifying the most suitable voltage level for the application, a design proposal of a 220 MVA back-to-back HVDC MMC system connected to 66 kV AC is discussed. Finally, the aspects of the submodule design is reviewed, and the different fault situations for the converter and how to handle them are explained.

**Chapter 5** will prove the feasibility of the power quality conditioning system through a case study with simulations in the MATLAB & SIMULINK environment. The development process of the simulation model is presented, together with the model itself. Voltage dip mitigation capabilities will be showcased for balanced and unbalanced conditions, and features of the system, such as harmonics, reactive power support and circulating current suppression is proven.

**Chapter 6** features first a reliability analysis including a fault tree analysis, showing how to design the system based on redundancy. Following up is the footprint estimation based on the dimensions of components found in the system design, together with a footprint review of an already existing project. Furthermore, an economic analysis is done based on own estimations, and cross referenced with literature and the costs of real projects already realised. Finally, a net-present-value (NPV) analysis of the investment cost of the proposed system is presented, together with the economic gain of increased availability of the LHC machine network of CERN. The chapter is concluded discussing the system developed in the thesis, and how it can be applied for applications beyond CERN.

**Chapter 7** will conclude this thesis and lay the ground for future work.
Ethics

CERN is a non-profit, peaceful organisation consisting of multiple nationalities and collaborations. All technology and development is open to the public with the ideology of sharing the advancements with society.

CERN states in its original convention for establishment of the organization [3], article 2, paragraph 1, that:

The Organization shall provide for collaboration among European States in nuclear research of a pure scientific and fundamental character, and in research essentially related thereto. The Organization shall have no concern with work for military requirements and the results of its experimental and theoretical work shall be published or otherwise made generally available.

The thesis project of developing a power quality conditioning system is applicable to several fields in the industry. Direct unethical and controversial applications of the to-be developed system are not identified as possible applications.
Chapter 2

HVDC Converter Topologies

2.1 High Voltage Direct Current

High voltage direct current (HVDC) is a technology that has been used in the industry for over half a century. It started out as a specialised product but it has gained a lot of momentum in the recent decades as the need for efficient and stable power transmission increased. This is especially thanks to the environmental focus on renewable energy where HVDC is widely used in transmission of offshore wind energy generation and other renewable sources. Beyond this, HVDC is used for a wide range of applications today [4], of which includes:

- Bulk power transmission over long distances on both land and subsea, connecting different grids together and creating a wider market for import and export.
- Stabilisation of power grids, reducing and mitigating effects of cascading AC instability [5].
- Power transmission to isolated locations such as islands, offshore platforms and remote locations in general.
- Connection of asynchronous grids allowing power to be exchanged despite different operating frequency or phase shifts, that otherwise would be incompatible with AC.
- Load centre in-feed, using underground HVDC cables and indoor converter stations for high power distribution with a small footprint. Examples of this are city centres, heavy industrial areas and urban areas in general.

HVDC is defined for converter stations operating at a DC voltage between 100 kV and 800 kV, and any voltages beyond are categorised as ultra-high DC. HVDC is based on two bidirectional electric power converters, where one is acting as a rectifier and the other
as an inverter. Connected together, these two converters form an AC-DC-AC conversion, utilising the properties of direct current and frequency in-variation combined with the ability to control power flow and other grid properties. In addition, HVDC is divided in two categories: The first is the point-to-point (PTP) connection that transmits power using cables or overhead lines with one converter station at each end, often called the HVDC link. The second is the back-to-back (BTB) connection, which is the configuration to be investigated in the thesis. The back-to-back connection is when the two converter stations are connected at the same site, and often in the same building using direct bus bars. This configuration is used mostly for the connection of asynchronous grids, but other specific uses exist as well.

HVDC converters are today based on two topologies, current source converter (CSC) and voltage source converter (VSC), each with their own advantages, disadvantages and operating principles. These topologies will be explained in the next chapters.

2.1.1 HVDC Configurations

HVDC technology comes in many different configurations, each with their own features and abilities. They are classified through the number of converters in parallel, as well as their earthing scheme and number of DC conductors. As presented in figure 2.1, the main configurations are:

- Symmetrical monopole.
- Asymmetrical monopole.
- Bipole, with and without metallic return.

A very common configuration for point-to-point connections are the bipole configuration. It allows for enhanced redundancy and operation, as it operates with two separate converter stations in parallel. It is a commonly chosen configuration using a converter topology called the current source converter (CSC). This configuration allows for the HVDC transmission to operate with only one pole active, in case of maintenance or faults of the other pole.

The monopole configuration is a more emerging type of configuration, often used by the so called voltage source converters (VSC). It relies on single converters with two lines connecting the rectifier and inverter. Some converters operate as a symmetrical monopole, meaning that both conductors operate at half of the DC voltage, respective to earth. This solution requires highly resistive earth connection at each converter station. Most back-to-back connections are realised with this configuration, where the two poles are direct bus bars. Another configuration is the monopole as an asymmetrical connection, meaning
that one conductor operate with the DC voltage, while the second one is the metallic return, or otherwise called the earth conductor.

For both the bipole and asymmetrical monopole, the choice of using the metallic return is optional for the function of the converter. If chosen not to use the metallic return, a highly resistive grounding must be implemented in both converter transformers. This way, the return current will flow to ground, requiring equipment and increased footprint leaving an environmental impact that might be unwanted. If metallic return is used, then one more conductor must be used, increasing costs and a potential impact on the subsea footprint.

![Figure 2.1: Commonly used HVDC system configurations.](image-url)

2.1.2 HVDC for Passive Network

The challenge with the back-to-back converter concept when it comes to industrial application, is that an industrial network is most of the time entirely passive, as seen in figure 2.2 which represents such a case. The definition of passive network means that there is no generation of energy, and hence no inertia. This means that the HVDC back-to-back must operate as a remote-end converter, or in what is sometimes called islanded operation mode. This case is found for HVDC links supplying islands without generation, offshore platforms and remote locations. The application is realised by giving the inverter the
task of creating an artificial inertia, by synthesizing the grid voltage for the passive network. This requirement is the most important factor when choosing topology and design of the converter, as the industrial load network would require excellent power quality and control over the synthesized AC voltage. Example of a remote-end HVDC converter is the offshore platform Valhalla [6], where the HVDC link supply all required power to the platform and the inverter creates and controls the AC voltage.

Studies have been conducted earlier in this field of using a back-to-back voltage source converter as a power quality conditioning system for industrial load applications [7]. This application and method did not break through to the industry, but this was over 10 years ago and the HVDC technology has advanced far since then.

![Diagram of back-to-back HVDC connected as a remote-end converter.](image)

Figure 2.2: Back-to-back HVDC connected as a remote-end converter.

### 2.1.3 HVDC Guidelines

Employing a HVDC converter scheme connected to the global energy distribution network in Europe, certain criteria must be fulfilled. From the official journal of the European Union, the "Commission Regulation (EU) 2016/1447 - establishing a network code on requirements for grid connection of high voltage direct current systems and direct current connected power park modules" [8], the regulation rules have to be followed for HVDC commissioning projects.

The regulations explicitly explains the roles of commissioner, transmission system operator (TSO) and owner of such projects, and defines necessary functions and requirements of the system. The most important paragraph from the regulatory is article 3, paragraph 7.a, which states:

> This regulation shall not apply to: HVDC systems whose connection point is below 110 kV unless a cross-border impact is demonstrated by the relevant TSO. The relevant TSO shall consider the long-term development of the network in this assessment;

This means that, by connecting a HVDC converter at 66 kV or below, following the reg-
ulatory to the letter is not necessary. Still, the regulatory provides useful information on commissioning of the HVDC scheme, which functions should be integrated and important aspects the TSO should be aware of.

Beyond regulations, there exists several design guidelines for HVDC projects. The many colloquiums and collaborations of CIGRE have created several guidelines in this field, by combining experience from academia, industry and transmission system operators across the globe. These guidelines are referred to as technical brochures, and some are used for this thesis project [9] [10] [11] [12]. Another useful guideline is from Det Norske Veritas (DNV GL) [13], explaining the role of HVDC converters and design process in the off-shore segment, which can be applied to all HVDC projects.

2.2 Current Source Converters

The current source converters (CSC) are a group of power electronic converters that are able to control and manipulate the current, essentially acting as a controllable current source. In the field of HVDC technology, CSC refers to thyristor converters, which again are often called line-commutated converters (LCC). The thyristor is a semiconductor switching device known for its high power capabilities and robustness, which is often used in HVDC converter stations for bulk power transmission. This type of converters can achieve power capabilities up to several gigawatt, and their power limits are constantly being pushed higher.

The thyristor converter used for HVDC comes in different configurations, being six-pulse, twelve-pulse and multi-pulse design. The operational principle of the thyristor switch is that it can be controlled to turn on to conduct current, and it is automatically turned off when the current reaches zero. This gives the thyristor converters the ability to shape and control the output current. Current source converters in the megawatt-range are usually designed as the twelve-pulse thyristor converter, because of the advantage of harmonics and power scalability. The multi-pulsed converter (18, 24, 36 pulses, etc.) are sometimes found in special applications ranging up to several gigawatt, where power-scalability is combined with the objective to reduce the harmonic distortion of the grid voltage.

2.2.1 The Thyristor

Going into the topic of this thesis, a fundamental understanding of power electronics is required. A key component to all power electronics is the semiconductor switching device that is used to develop active applications. These switches are divided into two families, the power thyristor and the bipolar switches, such as the insulated-gate bipolar transistor
(IGBT), the gate turn-off thyristor (GTO), as well as the integrated gate-commutated thyristor (IGCT).

The power thyristor is known for its high current and voltage ratings, while being very robust and economically feasible. Its major downside is that it can only be controlled to start conducting, and will turn off when the current passing through reaches its zero crossing. This creates several limitations that will be explained further in the next sections.

The thyristor is the fundamental component of the current source converter which is to be introduced. Utilising the fact that the thyristor stops conducting when the current is zero, adding an inductance in series, often called a "choke", the current can be phase shifted in such a way that the voltage will be negative when it is switched off. By this method, the thyristor is able to manipulate the output voltage, which is seen in figure 2.3.

![Figure 2.3: Fundamental operation of a single-phase half-wave thyristor rectifier.][14]

2.2.2 Line-commutated Converter

Figure 2.4 shows the twelve-pulse thyristor converter, which is commonly used in HVDC transmission. This converter works by utilising a three-winding transformer from wye-wye/delta creating a phase-shift of 30 degrees, effectively reducing harmonic distortion and DC ripple. The basic twelve-pulse converter is the line-commutated converter, while a special configuration with inserted line capacitors and switches is called the capacitor-commutated converter (CCC).

Whether the CSC can be connected to a particular network is determined by the short circuit ratio (SCR), as defined in (1). This is the short circuit power at the connection point of the converter, over the converter rating itself, which more precisely is defined as
the short circuit power of the AC network, over the short circuit power at the DC bus. This parameter determines if the converter will be susceptible to commutation failure if the connected grid is not strong enough to withstand certain transient events. A typical value from literature is that the twelve-pulsed thyristor converter must have an SCR of 3 or more [14]. In comparison, a passive AC network has a short circuit power of zero and thus to realise the CSC as an inverter, an external method to commutate must be employed, such as a generator-set or an active switching solution presented in [15].

$$SCR = \frac{S_{sc}}{S_{rating}}$$

(1)

![Figure 2.4: The twelve-pulse thyristor converter.](image)

### 2.2.3 Capacitor Commutated Converter

Another topology for the current source converter is the capacitor-commutated converter (CCC), which is based on the original thyristor converters with six or more pulses. The CCC operates by connecting capacitors in series with the high-voltage line, so that it compensates reactive power based on the active power supplied. This makes the converter independent from the grid connection strength and helps to control the active commutation process of the converter, making it less independent of line commutation and less sensitive to disturbances preventing commutation failure. The CCC still requires an SCR of around two to ensure safe operation, and it is not applicable to feeding a passive grid. The challenge of the CCC is the design of series capacitors that must withstand the
line current, increasing the complexity of the converter design in relation to the original twelve-pulse converter. The concept of the capacitor-commutated converter is seen in figure 2.5 for a 6-pulse thyristor bridge, where the line capacitors are placed between the converter transformer and the converter valves. This topology can be expanded to the 12-pulse converter, as well as multi-pulse applications.

![Figure 2.5: The capacitor-commutated converter concept.](image)

### 2.3 Voltage Source Converters

The voltage source converter is a group of converters that can control the applied DC voltage of its output terminals, essentially working as a controllable voltage source. With regard to HVDC technology, VSC is a popular group of topologies that is based on the modern IGBT and IGCT semiconductor switches that are capable of controlling both turn-on and turn-off. This ability gives the VSC a larger degree of freedom and allows forced commutation that is not depending on the zero crossing of the current, which the thyristor is. One of the main features for all VSC is that they can operate under weak network connections, and even with networks with an SCR of zero. In the family of VSC are several notable topologies. Among them are the neutral point clamped converter and flying capacitor converter, which are commonly used in industrial drives and other low-medium power applications. Their technology is limited, and often it is designed as a three-level converter. This means that the converter can generate an output voltage in three steps, being the positive DC voltage, zero, and negative DC voltage. Another topology within the VSC is the cascaded converter, using series-connection of either H-bridges or half-bridges. This is called the modular multilevel converter.
2.3.1 The IGBT

The IGBT and its family of switches can be switched both on and off, giving more freedom and controllability compared to the thyristor. With that being said, the IGBT is not as robust as the thyristor, and comes with smaller power ratings while being more expensive. What is common for both types of the semiconductor switches is that they are three-terminal devices, with two connectors as the conduction path, and the last as the control terminal. The switches are controlled by sending pulses to the control terminal, often called the gate. The thyristor requires a high current pulse to start conducting, while the IGBT requires two voltage pulses, one to switch on and one for off. Every switch needs its own gate controlling circuit, called the gate driver. When receiving logic signals, they generate the electrical pulses to operate the power electronic switches.

2.3.2 Two-level Converter

The two level voltage source converter works by adapting the voltage in two steps, this is $\pm V_{DC}/2$. The fundamental function is well presented in [16]. This type of converters normally operates with a high switching frequency to reduce harmonics, and while having a simpler construction compared to other solutions, it has increased switching-losses. This also means that the two-level VSC often needs harmonic filtering to satisfy the required power quality of the systems connected to it. The typical two-level voltage source converter is presented in figure 2.6. The "low"-level voltage source converters often requires series connection of semiconductor switching devices in medium and high power applications, to reach the rated DC voltage. This requires snubber circuits to guarantee equal voltage sharing between the switches, which increases the amount of components as well as the electrical losses.

![Figure 2.6: The two-level Voltage source converter.](image)
2.3.3 Cascaded H-bridge Converter

The cascaded H-bridge converter is a concept that can be realised in many ways, and is built on the technology of the VSC. It is based on using so-called "submodules", which are a two-terminal devices that allow for series connection. These submodules are mainly divided into two types, the full-bridge submodule or the half-bridge submodule, as seen in figure 2.7. The main difference between these two types is that the full-bridge has more output voltage stages, but at the same time it has more power electronic components and higher losses than the half-bridge. The half-bridge is the most common submodule in high power applications, as efficiency is of high importance. Connecting these submodules in series forming converter arms, the topology of modular multilevel converter (MMC) is realised.

The modular multilevel converter is often more expensive and more complex than a typical two or three-level converter, but it enhances and improves many aspects. Some of the benefits of the MMC is that it operates at unity power factor, needing no reactive power compensation. It also allows for high efficiency, reduced harmonic generation and very high reliability. The IGBT is the most commonly used semiconductor switch used for modular multilevel converter, but the topology can be realised with the GTO or IGCT as well.

![Figure 2.7: Full-bridge and half-bridge configuration - (a) Shows the half-bridge module and (b) the full-bridge module.](image-url)
2.4 Discussion and Conclusion

The design options for a remote-end back-to-back HVDC converter is many, and when the rectifier and inverter can be designed individually, it opens for several interesting combinations. The rectifier and inverter is not limited to the same topology, and a hybrid combination should be considered. Table 2.1 summarises all features of the CSC and VSC. Based on the previous chapters and this table, there are four different combinations possible from the different topologies:

1. VSR and VSI - Voltage source back-to-back topology.
2. CSR and CSI - Current source back-to-back topology.
3. CSR and VSI - Hybrid back-to-back topology.
4. VSR and CSI - Hybrid back-to-back topology.

Based on the needs presented in the objectives of this thesis, the first assessment must be on inverter topology design, because of the strict requirement of remote-end connection. As line-commutated and capacitor-commutated converters cannot be connected to a weak AC network without extensive design with generator sets or active commutation schemes [14], the voltage source converter becomes the preferred topology for the inverter. This argument proves valid when considering existing practical applications for such converters. Examples are electrified offshore platforms operating in islanded mode, which are built using VSC converters [6].

The next step is to assess whether the rectifier should be designed as a CSC, making the hybrid HVDC topology with the VSC inverter, or if the rectifier should be VSC as well, creating the back-to-back HVDC VSC. The main argument for any current source converter is that the converter valves are cheaper, have lower losses and is very robust. It should also be noted that thyristors have been around for a long time and is proven very reliable. Meanwhile, the VSCs are more expensive and have only been around for a short time compared to thyristors.

There are several benefits of choosing a complete back-to-back HVDC VSC system over a hybrid one, mixing current source rectifier (CSR) and voltage source inverter (VSI), such as:

- VSR would operate at unity power factor and not requiring reactive power compensation, compared to the CSR that would need an active reactive power compensation scheme.
- Smaller footprint compared to the hybrid solution, as VSR would need less harmonic filters.
- VSR can operate with normal AC transformers already used in the infrastructure, without including a special converter transformer such as for CSR.

- The VSR has great fault-ride through capabilities enabling it to operate during abnormal events such as voltage dips, compared to LCC which is prone to commutation failure. For CSR to be able to operate, a CCC must be employed, introducing even more components to the converter.

- And the largest advantage: VSR and VSI can be constructed as identical converters, reducing amount of engineering needed, using the same control system design, common spare-parts and identical maintenance procedures, as well as components can be bought and assembled in larger quantities.

To conclude this chapter, the most beneficial topology for the back-to-back HVDC system, of which this thesis will further develop and base work upon, is the voltage source converter, and more specifically: The modular multilevel converter as both rectifier and inverter.

One interesting concept worth noting is the hybrid diode rectifier with VSI, which allows only for unidirectional power flow. As industrial loads do not need to send power to the grid, this limitation is not of concern. The rectifier could be designed as a twelve-pulsed diode rectifier, improving the harmonics and increasing the DC voltage. For a very budget-oriented power quality conditioning system it is an interesting solution, but as it does not possess blocking capability or control, it is not applicable for CERN.
Table 2.1: Comparison of HVDC converter topologies for application as the power quality conditioning system, gathered from [14].

<table>
<thead>
<tr>
<th>Criteria:</th>
<th>Current Source Converter</th>
<th>Voltage Source Converter</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>LCC</td>
<td>CCC</td>
</tr>
<tr>
<td>Power factor</td>
<td>Consumes reactive Power</td>
<td>Consumes reactive power</td>
</tr>
<tr>
<td>Reactive power support</td>
<td>No</td>
<td>Line capacitors support some</td>
</tr>
<tr>
<td>Commutation</td>
<td>Line commutated / Forced</td>
<td>Capacitor commutated / Forced</td>
</tr>
<tr>
<td>Grid connection strength</td>
<td>Need strong network (SCR=3)</td>
<td>Need moderate network (SCR=2)</td>
</tr>
<tr>
<td>Remote-end capability</td>
<td>No, need generator-set</td>
<td>No, need generator-set</td>
</tr>
<tr>
<td>Relative losses</td>
<td>Low</td>
<td>Moderate</td>
</tr>
<tr>
<td>Relative cost</td>
<td>Low</td>
<td>Moderate</td>
</tr>
<tr>
<td>Redundancy possibilities</td>
<td>High</td>
<td>Moderate</td>
</tr>
<tr>
<td>Control complexity</td>
<td>Low</td>
<td>Low</td>
</tr>
<tr>
<td>Harmonic filter needs</td>
<td>High, low-order harmonics</td>
<td>High, low-order harmonics</td>
</tr>
<tr>
<td>Footprint</td>
<td>Large</td>
<td>Large</td>
</tr>
<tr>
<td>Control response time</td>
<td>Fast (1-3ms)</td>
<td>Fast (1-3ms)</td>
</tr>
<tr>
<td>Converter transformer</td>
<td>Special converter transformer</td>
<td>Special converter transformer</td>
</tr>
<tr>
<td>Energy storage needs</td>
<td>External storage in DC bus</td>
<td>External storage in DC bus</td>
</tr>
<tr>
<td>Industrial experience</td>
<td>High, universal uses in industry</td>
<td>Moderate, used for HVDC</td>
</tr>
</tbody>
</table>
Chapter 3

Modular Multilevel Converter

In the previous chapter, it was established that the modular multilevel converter is the most beneficial choice of topology for both rectifier and inverter for the application as a power quality conditioning system. Therefore, the MMC will be used for further development of the back-to-back converter concept.

3.1 Back-to-Back MMC

The back-to-back HVDC Modular multilevel converter is a system of high complexity. It includes many different dynamics that allows it to control and shape voltages and currents in special ways. Before going into the mathematics and controls of the system, a qualitative explanation of its function is in its right place. The system, as presented in figure 3.1, consists of a rectifier and an inverter. The inverter is connected to a passive load representing a isolated distribution network. The main objective of the rectifier is to control the DC voltage of the bus, while the inverter will control the AC voltage to the load. The interesting aspect is that inside the converter lies an internal energy storage system, that allows to store and convert energy between AC and DC quantity.

The rectifier, in a very simplistic explanation, uses the AC power from the grid to charge this energy storage inside, and discharges it as DC power. At the same time, the inverter charges its energy storage from the DC power supplied from the bus, to discharge an AC voltage to the load. This is a simplified explanation, but it gives the over-all function of the system.
Figure 3.1: The principle of the back-to-back MMC system for a passive load.

The back-to-back HVDC modular multilevel converter consists of several components making up the converter and its functions. The overall structure of the system is shown in figure 3.2, and the function of the system and dimensioning of these components will be explained in the following chapters of the thesis.

Figure 3.2: Detailed look into the MMC in the back-to-back configuration.

3.1.1 Reference Projects

Several interesting HVDC projects have been commissioned over the last years which can relate to the topic of the thesis, of having a back to back HVDC converter supplying a passive network. No projects as of today have combined the BTB with islanded operation, but the principles of the projects, their construction and operation is the same. A list of many HVDC projects already commissioned is available in [17].
• Valhall and Troll HVDC, Norway: These two projects are both point-to-point connection of HVDC voltage source converters operating in islanded mode. They transmit power to off-shore platforms from the shore of Norway through subsea cables, reducing emissions of traditional generators placed locally. These projects are interesting because of the islanded operation, as the HVDC link transmits all power and the chosen technology is VSC because of the ability to commutate to a passive network. ABB was the supplier of these two projects, with their HVDC light technology [6].

• Trans Bay Cable, North America: The project was commissioned in 2010 by Siemens and is known as the first HVDC project using modular multilevel converter architecture. It is a point-to-point HVDC link transferring power from San Francisco to Pittsburg, California [18].

• Mackinac BTB, North America: This project is a back-to-back converter commissioned by ABB to enhance the power stability of the overall AC network by connecting two synchronous networks together in one converter station. This project relies on the VSC technology, as the need for commutation to weak network is necessary in case either connection side would have a black-out [19].

• Eagle Pass BTB, North America/Mexico: The first HVDC back-to-back converter using VSC and IGBT technology, commissioned by ABB in 2000 and transferring power between the two asynchronous grids of Texas, and Mexico.[20].

Table 3.1: Existing HVDC reference projects using VSC technology.

<table>
<thead>
<tr>
<th>Project</th>
<th>Type:</th>
<th>Year:</th>
<th>Technology:</th>
<th>DC voltage:</th>
<th>Rating:</th>
</tr>
</thead>
<tbody>
<tr>
<td>Valhall HVDC</td>
<td>PTP / island</td>
<td>2011</td>
<td>IGBT - VSC</td>
<td>150 kV</td>
<td>78 MW</td>
</tr>
<tr>
<td>Troll 3 &amp; 4</td>
<td>PTP / island</td>
<td>2015</td>
<td>IGBT - VSC</td>
<td>120 kV</td>
<td>184 MW</td>
</tr>
<tr>
<td>Trans Bay Cable</td>
<td>PTP</td>
<td>2010</td>
<td>IGBT - MMC</td>
<td>400 kV</td>
<td>400 MW</td>
</tr>
<tr>
<td>Mackinac BTB</td>
<td>BTB</td>
<td>2014</td>
<td>IGBT - VSC</td>
<td>140 kV</td>
<td>200 MW</td>
</tr>
<tr>
<td>Eagle Pass BTB</td>
<td>BTB</td>
<td>2000</td>
<td>IGBT - VSC</td>
<td>31.8 kV</td>
<td>36 MW</td>
</tr>
</tbody>
</table>

3.2 Mathematical Model of MMC

The mathematical model of the modular multilevel converter can be split into four separate parts for simplification. The first part describes the individual submodule dynamics. The second part determines the relationship between AC and DC side of the converter, focusing on system-level equations. The third part represents the interaction of the upper and lower arm in one phase, and the fourth models the interaction in the converter arms between different phases.
3.2.1 Fundamental Operation of the Submodule

The MMC consists of several sub-modules (SM) acting as separate units, connected together in series to form a converter arm. One submodule consists of two switches, two diodes and one capacitor. The name "modular multilevel" comes from the ability to connect these submodules in a modular way, as a piece of a larger converter, and the multilevel is defined by the amount of submodules connected in series. A modular multilevel converter is built up of six converter arms, two for each phase. Figure 3.3 shows how one converter arm is built up of several submodules, and the operation of each individual submodule. The operation of the submodule is controlled by switching the capacitor in and out, applying the capacitor voltage to the output terminal of the submodule. By controlling several submodules this way, one can shape the output AC voltage of the inverter, and sustain constant DC-voltage with the rectifier. The subscripts to be used in this main chapter are given as: 'j' Defines the phase (a, b, c) while 'u' means upper arm and 'l' is lower arm. 'N' Defines the amount of submodules in the converter, while 'i' is reserved for each individual module starting from 1 to 'N'.

\[
V_{c_m:i} = T_{on} \cdot V_c \tag{2}
\]

\[
V_{arm} = \sum_{i=1}^{N} V_{c_m:i} \tag{3}
\]

\[
Levels = N + 1 \tag{4}
\]

![Figure 3.3: MMC converter arm and fundamental operation of submodule.](image)
Table 3.2: Operation of SM based on switch states.

<table>
<thead>
<tr>
<th>Case</th>
<th>T1:</th>
<th>T2:</th>
<th>Voltage</th>
<th>State:</th>
</tr>
</thead>
<tbody>
<tr>
<td>I</td>
<td>1</td>
<td>0</td>
<td>Vc</td>
<td>On-state</td>
</tr>
<tr>
<td>II</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>Bypassed State</td>
</tr>
<tr>
<td>III</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>Blocked State</td>
</tr>
<tr>
<td>IV</td>
<td>1</td>
<td>1</td>
<td>-</td>
<td>Invalid State</td>
</tr>
</tbody>
</table>

Table 3.2 shows the states in which the submodule operates, where case I and II act as the fundamental operation, and case III is only used for blocking the operation of the submodule, in cases with start-up and fault handling. Case IV is an invalid state that the submodule must never reach, as it causes a short-circuit of the SM capacitor.

With this dynamic, the submodule can choose to charge or to discharge the capacitor depending on the polarity of current flowing through, to assure a constant voltage level when operating.

Looking into the definition of the control signal of the module, which essentially tells how many of the total modules of one arm is inserted at maximum AC amplitude. In an 'N+1' level converter there needs to always be 'N' modules inserted in total in the upper and lower arms of one phase. This does not mean that the upper arm must insert all modules at one point, but can keep some in the lower arm inserted as well. This is the converter’s ability to control. For example, with a modulation index of 0.8, the upper arm will have inserted 80% of its modules, while the lower will have inserted 20% of its modules. Equation (5) presents the definition of modulating index with the variable T, being 1 for on-state of the submodule, and 0 for the off-state.

$$m_j = \frac{\sum_{i=1}^{N} (T_{u,ji})}{N}$$ (5)

### 3.2.2 AC and DC Side Interactions

By going into the mathematical model of the MMC, the fundamental equation (6) presents the control variable of the MMC. It is derived for the most basic switch-mode converters in [21] and is called the modulation index. It is a variable that derives the relationship between the DC and the fundamental component of the AC voltage in voltage source converters, also called switch-mode converters.

$$\hat{v}_j = m_u \cdot \frac{V_{DC}}{2}$$ (6)
Translating (6) from peak phase voltage to RMS of line-line voltage, applicable to the three-phase systems gives (7).

\[ V_{LL} = \frac{\sqrt{3}}{2\sqrt{2}} \cdot m_a \cdot V_{DC} = 0.612 \cdot m_a \cdot V_{DC} \quad (7) \]

Looking into the ideal relationship between AC and DC side of the modular multilevel converter, not accounting for internal losses, then (8) must be true for the system. Unfolding (8) into currents and voltages gives (9). Inserting (7) into (9) gives the relationship of the AC and DC currents as a function of modulation index as (10).

\[ P_{AC} = P_{DC} \quad (8) \]
\[ I_{DC} \cdot V_{DC} = \sqrt{3} \cdot V_{LL} \cdot I_{ph} \quad (9) \]
\[ I_{ph} = \frac{2\sqrt{2}}{3} \cdot m_a \cdot I_{DC} \quad (10) \]

Furthermore, for steady state operation in ideal conditions with no losses, as the power-flow must remain constant, (11) can be used to calculate the DC current for the system.

\[ I_{DC} = \frac{P_{DC}}{V_{DC}} \quad (11) \]

With these fundamental equations presented in this section for the relationship between AC and DC voltages, currents and power, most system parameters can be calculated for both inverter and rectifier operation which classifies the overall system.

It is important to note that the modular multilevel converter has a control-range defined by the modulating index, and that the worst case of currents and voltages in the DC side should be calculated at the limit of this control range. This means that with a modulating index of 1, the current will be at maximum while at the lowest expected index, the voltage will be highest.

### 3.2.3 Upper and Lower Arm Dynamics

The fundamental equations for the upper and lower arm dynamics are independent of the operation of the converter, whether it is inverting or rectifying. The modular multilevel converter is built up of 6 converter arms, as seen in figure 3.2 with ’N’ number of submodules. Exploring the dynamics of the upper and lower arm gives the mathematical model of how the converter works, and also how the submodules should be dimensioned based on voltages and currents. Using equation (3) introduced in the submodule dynamics, one
converter arm can be modelled as a varying DC voltage source. This leads to figure 3.4, which shows the equivalent model of the modular multilevel converter. In the figure an artificial neutral point in the DC bus is implemented so that applying Kirchoffs voltage law (KVL) is possible. This artificial grounding is done based on the fact that the converter arms are entirely symmetrical, and it is not used in practical implementations for the converter. This mathematical model is well documented in [22] and [23].

![Converter Arm Model](image)

**Figure 3.4: MMC converter dynamics - Equivalent model.**

**Voltages**

As the DC voltage of the bus is constant in steady state operation, the upper and lower arm voltage of every phase must be equal to (12). This is valid for both inverter and rectifier operation.

\[
V_{DC} = V_{u,j} + V_{l,j}, \quad j = a, b, c
\]  

(12)

Following the logic further, the individual upper and lower arm voltage can be explained using (2) and (3) together with Kirchhoffs current law (KCL) in non-ideal conditions, accounting for the voltage drop over the internal resistance and the arm inductor. This results in equations (13) and (14).

\[
V_{u,j} = \sum_{i=1}^{n} (T_{u,ji} \cdot V_{C,u,ji}) + L_s \frac{di_{u,j}}{dt} + i_{u,j} R_{u,j}
\]  

(13)

\[
V_{l,j} = \sum_{i=1}^{n} (T_{l,ji} \cdot V_{C,l,ji}) + L_s \frac{di_{l,j}}{dt} + i_{l,j} R_{l,j}
\]  

(14)
The phase voltage at connection of the arm is defined in equation (15), by using KVL with the artificial earthing point together with either (13) or (14). This is a useful equation for inverter operation as the AC voltage will be controlled.

\[ V_j = -V_{u,j} + \frac{V_{DC}}{2} = V_{l,j} + \frac{V_{DC}}{2} \]  

(15)

**Currents**

Figure 3.4 shows all current dynamics of the mathematical model of the MMC. This part will explain the AC phase currents and individual arm currents together with the DC current, reserving the circulating currents for the next section. Positive current direction is defined as through the upper arm to the positive DC bus for all phases. Using the DC bus as nodes for KCL, equation (16) shows that the DC current flowing is the sum of all arm currents.

\[ I_{DC} = \sum_{j=a,b,c} I_{u,j} = -\sum_{j=a,b,c} I_{l,j} \]  

(16)

As the converter can be considered symmetrical between the upper and lower arm, then the flow of AC current at the connection point node is presented in equation (17) with the AC current also separated. Based on this fact, equation (18) presents the AC quantity of the fundamental frequency component of the arm current for the upper and lower arm.

\[ i_j(t) = i_{u,j}(t) + i_{l,j}(t) \]  

(17)

\[ i_{u,j}(t) = -i_{l,j}(t) = \frac{\sqrt{2}I_{ph}}{2} \cdot \cos(\omega t + \theta_j) \]  

(18)

Knowing that the converter is symmetrical not only between the upper and lower arms, but also between the phase arms, means that the total contribution to the DC current is equal. This results in the DC component of every arm being one third of the total DC current as shown in (19).

\[ I_{u,j} = \frac{I_{DC}}{3} \]  

(19)

Knowing both the AC and DC component, the total arm current of any arm and phase is given in (20) and (21). The circulating current, which will be presented in the next section is included for the complete accuracy of the model, shown by the 'diff' as the differential current between arms.
\[ i_{u,j}(t) = \frac{i_j(t)}{2} + \frac{I_{DC}}{3} + i_{diff,j} \] (20)

\[ i_{l,j}(t) = -\frac{i_j(t)}{2} + \frac{I_{DC}}{3} + i_{diff,j} \] (21)

Based on equation (18)(20)(21) the dimensioning current equations for the submodule based on maximum peak and RMS values are given by (22) and (23), which will be useful for deciding IGBT and capacitor components at a later stage.

\[ I_{arm,RMS} = \sqrt{\frac{I_{ph}^2}{4} + \frac{I_{DC}^2}{9}} \] (22)

\[ I_{arm,peak} = \frac{\sqrt{2} \cdot I_{ph}}{2} + \frac{I_{DC}}{3} \] (23)

### 3.2.4 Circulating Dynamics Between Arms

In operation of the modular multilevel converter, the capacitors will discharge and charge from cycle to cycle, of which capacitor voltage ripple is the result. During this time, the energy stored in the upper and lower arm, as well as between the other upper arms, is not constant. This difference in energy stored in the capacitor introduces an internal current in the converter that will circulate between the different phase-arms. This is called the circulating current, and through various circuit analyses it can be shown to be of double fundamental frequency [24].

There are two equations to define these dynamics. They are the differential currents in one phase, and the circulating current between the phases. The differential current is defined at the AC connection node, and follows equation (24), which is the average of the difference in the current in the upper arm and lower arm of a given phase. Equation (25), based on the differential currents, shows the circulating currents flowing in the arm, as depicted in figure 3.4.

\[
\begin{bmatrix}
I_{diff,a} \\
I_{diff,b} \\
I_{diff,c}
\end{bmatrix} = \frac{1}{2} \cdot \begin{bmatrix}
I_{u_a} - I_{l_a} \\
I_{u_b} - I_{l_b} \\
I_{u_c} - I_{l_c}
\end{bmatrix} - \begin{bmatrix}
\frac{I_{DC}}{3} \\
\frac{I_{DC}}{3} \\
\frac{I_{DC}}{3}
\end{bmatrix}
\] (24)

\[
\begin{bmatrix}
I_{z,ab} \\
I_{z,bc} \\
I_{z,ca}
\end{bmatrix} = \begin{bmatrix}
I_{diff_a} \\
I_{diff_b} \\
I_{diff_c}
\end{bmatrix} - \begin{bmatrix}
I_{diff_b} \\
I_{diff_c} \\
I_{diff_a}
\end{bmatrix}
\] (25)
The circulating current is dominated by a second order component as shown by (26). It possess other even order components such as the 4th, 6th and 8th, but they are of very small proportions and can be excluded.

\[ i_{z,ab}(t) = I_{z,ab} \cdot \sin(-2\omega_0 t) \]  

(26)

The circulating currents will be introduced further when explaining how the control system can suppress them, as these 2nd harmonics are stressing the submodule components.

### 3.3 Capacitor Balancing Strategy

In the HVDC modular multilevel converters, there are several submodules with charged capacitors that shape the output voltage through control and modulation. These capacitor voltages inhibits a DC component, as well as an AC component. This AC component is caused by the charging and discharging of the capacitors to operate the converter. When one submodule is in on-state more than it is in off-state, then the voltage will start to fluctuate, as the charge/discharge time is not balanced. This can potentially be a slow process resulting in an overvoltage in the submodule capacitors, exceeding the ratings of the IGBTs, and damaging the converter.

To be able to safely operate the converter, the capacitor voltages must be balanced at all times. There are several methods to do this, presented both in literature books and research papers, where some are already implemented in real converters. Some of these strategies are presented in [21] (chapter 5.6).

The capacitor balancing strategy is the last operation in the process of generating pulses to control the modular multilevel converter. The capacitor balancing receives the number of submodules that should be switched in each respective arm of the converter, and has to select the correct ones to fire to achieve balance. All the operations are seen in figure 3.5, and will be explained in the following sections.

![Figure 3.5: Process for controlling the modular multilevel converter.](image)
Voltage sensors used for balancing

The most reliable method is to install voltage sensors for all capacitor voltages and use a sorting algorithm to choose which submodules to be turned on, and in which order, to maintain equal voltage. This algorithm works by first measuring the polarity of the arm current, which translates to whether or not the capacitors are charging or discharging. Then the algorithm computes the order in which the submodules will conduct. For example, the least charged module will be the first one to be switched on during a charge cycle, and the module with highest voltage will be the first one turned on during a discharge cycle. This algorithm would run every cycle of the fundamental frequency and a strong computational power is required to compare all the voltage signals at every switching instant. The main concern with this method is the amount of voltage sensors needed, as with modular multilevel there can be many capacitors. The number of sensors follows the formula of $12^N$ for the back-to-back MMC converter, with ‘N’ being the amount of submodules. For example, a 31 level rectifier and inverter would require 30 voltage sensors across each of the 12 converter arms. This requires many communication channels for signals and considerable computing power.

Sensorless balancing

There are two methods for the sensorless balancing of capacitor voltages. The first method is to use “passive” balancing. It is based on rotating the modulation signal with increments so that every submodule has equal conduction time over a longer time period. For example a 5 level inverter with 4 submodules: After 4 periods of conduction, all four modules would have been the first to turn on once. This first method is based on the assumption that every capacitor voltage will deviate equally over a fixed time, which holds true for steady state operation. If there are transient events occurring in the system, then this balancing system will not restore the past deviation, but limit the future deviation occurring in steady state. This means that if a transient event happened, there might be capacitors that end up with a higher voltage and others with lower voltage. More research must be done on this solution if it was to be considered.

The second sensorless method is based on estimating the voltages through an algorithm called “Adaptive Linear Neuron (ADALINE)” [25]. It is not completely sensorless, as it requires three sensors per phase. Two for each arm inductor and one for the output phase voltage. This method has the feature that it can adapt during transient or irregular events such as voltage dip mitigation and still keep the capacitor voltages balanced. It is worth noting that this is still a new technique aimed at HVDC control systems with large amounts of levels. By comparing this method with nine sensors in total and a more advanced algorithm against the hundreds of voltage sensors for all capacitors of the 30
level back-to-back, it can be concluded that the capital costs can be reduced by using fewer sensors. It is still a new technique, so further research must be done. Therefore, the manual method of voltage sensors in every submodule should be used, until this technique is proven reliable.

3.4 Modulation Strategy

There exist several modulation strategies commonly adopted for the MMC. For low-level MMC it is typical to employ a carrier based strategy, as it is effective for higher switching frequencies. Selective harmonic elimination (SHE) modulation is a common strategy adopted for this, as it allows for elimination of selected harmonics that otherwise could be difficult or expensive to suppress with passive filters. Other carrier-wave based strategies as PS/PD-PWM are also used for applications with low to medium levels of harmonics. Many of these strategies are presented in [26]. Selection of the modulating strategy is not tied to the overall control system, as it uses the modulating index (reference signal) to create gate pulses. How these gate pulses are created is a mere question of modulating strategy developed, and will decide the switching frequency, harmonic distortion and switching losses, which are physical properties of the converter.

Phase Shift PWM (PS-PWM)

Phase shifted carrier waves used for pulse width modulation (PWM) is a common strategy because the natural balancing of on-time for each switch is included, was introduced earlier for capacitor balancing. This modulation strategy creates carrier-waves of equal amplitude, only phase-shifted between each other. There is one carrier-wave for each module, generating a gate-pulse when the control logic is true. For carrier based modulation strategies, the switching frequency should be a factor of 3 of the fundamental frequency, to reduce harmonic distortion, as shown in equation (27). The principle of this modulating strategy is shown in figure 3.6 with a low switching frequency, only used to enhance the details.

\[ f_{sw} = f_{(1)} \cdot 3k \quad , \quad k = 1, 2, 3... \] (27)
Figure 3.6: Phase-shifted carrier waves in pulse width modulation (f=50Hz) for a 5-level converter.

**Phase Disposition PWM (PD-PWM)**

The PD-PWM method uses several triangular carrier waves with differing amplitude and constant offset. By comparison with the reference signal the PWM for each module is generated. This principle is shown in figure 3.7. While not ensuring equal on-time for each switch, this strategy produces slightly less harmonics compared to PS-PWM. The PD-PWM comes in several sub-strategies which either phase shifts every other triangular carrier wave by 180 degrees, or that phase-shifts every carrier with a negative offset.

Figure 3.7: Phase-dispositioned carrier waves in pulse width modulation (f=250Hz) for a 5-level converter.
Nearest Level Modulation

The nearest level modulation (NLM) is the most commonly adopted modulation strategy for an MMC operating with many levels. It allows for operation for switching frequency equal to the fundamental frequency, efficiently reducing the associated switching losses of the converter. The drawback is that the harmonic distortion is increased compared to carrier-bases strategies. A common addition to the NLM is utilising the single PWM controlled switch, letting one submodule operate as PWM with higher switching frequency, reducing the total harmonic distortion of the output waveforms.

The NLM works by translating the modulating signal, which is continuous and sinusoidal, into a discrete stair waveform, directly telling the pulse generator how many modules to insert. This principle is presented in figure 3.8. A benefit of using NLM is the compatibility with advanced voltage balancing algorithms based on voltage sensor measurement for every submodule. As the reference for the pulse generator is discretised, it gives room for computation for which submodules should be switched next to achieve the best balancing of capacitor voltages. The strategy together with the benefit of capacitor balancing is presented in [27].

NLM is the most common strategy for high power MMC applications in practical operation. Then, based on the amount of levels, the single-switch PWM modulation can be reviewed if the THD must be improved.

![Figure 3.8: Nearest level modulation strategy for a 5-level MMC.](image)

Third Harmonic Injection

Third harmonic injection is a modulating strategy to allow for up to 15% increased RMS voltage for inverter operation. It utilises the third harmonic component in the AC voltage, effectively creating a third harmonic distortion to the grid. However, as a major drawback, it degrades the power quality in terms of THD. It might be a strategy to implement to increase the transient performance during fault-ride through [28].
3.5 Control System

The principal objective of the back-to-back HVDC modular multilevel converter in this thesis is to operate in islanded mode continuously. Therefore the objective is for the rectifier to control the DC voltage, and for the inverter to control the required AC voltage. For a passive load, it will draw the required power as long as the voltage is satisfactory. Active power control is not available for the MMC in this mode, but is not needed as the load will naturally draw the required power. On the other hand, reactive power control is available for the rectifier to support the upstream grid if needed. For the control systems described below, the parameters are in per unit, to introduce a universal control system that can be applied to any MMC system.

3.5.1 Control in Synchronous Reference Frame

Control in synchronous reference frame (SRF) is based on the direct-quadrature-zero (dq0) transformation, which is the mathematical Park and Clarke transformation of three-phase AC signals. The mathematical operations are given in appendix A, with a more thorough explanation. The benefit of this technique is to transform continuous alternating signals such as voltage and current into a reference frame that rotates with the frequency of the AC signals. This effectively means that AC signals can be viewed as DC signals, portraying the three-phase AC properties such as phase and magnitude, and possible unbalances. The dq0 sequence is represented in the d-q-plane, where the d-axis represents the real quantity, and q-axis imaginary quantity. Indirectly, the d-axis represents interaction with the active power, and q-axis is the reactive power.

For the transformation of AC signals to SRF, an angular frequency input is needed. For the rectifier, a robust phase-locked loop (PLL) can be used to synchronise to the supplied grid voltage, creating the angular frequency reference. A robust PLL is able to detect the angular frequency despite harmonics and unbalanced conditions in the AC signals [29]. For the inverter to control its output AC voltage, a reference angular frequency is needed as well. Since it is not possible to synchronise to its own produced AC voltage, two possible methods can be used to generate the reference angular frequency. If the electrical network fed by the inverter needs to be synchronised to the upstream grid, then it can use the same angular frequency reference as the rectifier. If no synchronisation is needed, then the inverter can use an artificial PLL, generating a constant angular frequency reference.

From power engineering theory, the positive, negative and zero sequence are commonly used to describe unbalanced conditions in load impedance, voltage and current. This can be combined with the dq0 transformation, resulting in the positive, negative and zero dq0 sequences. This strategy is called the dual synchronous reference frame (DSRF) control,
and it allows for interaction with negative sequence current injection to upstream grid and load during unbalanced fault-scenarios, as shown in [30]. This feature can be beneficial for the transmission system operator (TSO) and the surrounding electrical networks, as it can stabilise unbalanced conditions. The DSRF method increases the overall complexity of the controls, and it is not required for the standard control features of the back-to-back MMC system, which is to be simulated in this thesis. Even though the DSRF control is acknowledged as a beneficial method, the SRF control is used in this thesis for simplicity.

3.5.2 Outer Voltage Loops

Rectifier DC Voltage Control

The main objective of the rectifier is to control the DC voltage. This is done through creating the reference d-axis current for the inner current loop, by comparing the reference DC voltage to the measured DC voltage, creating an error signal feeding the proportional-integral (PI)-controller of the loop, as seen in figure 3.9. A logic saturation control is used to limit the reference output of the controller, which is the reference for the next control system, the inner current loop. The overall control loop can be represented by (28).

\[
I_{ds} = (V_{DC^*} - V_{DC}) \cdot (K_p + \frac{K_i}{s})
\]  

(28)

![DC Voltage Controller](image)

Figure 3.9: DC voltage controller for the rectifier.

Inverter AC Voltage Control

The inverter has the main objective of controlling and shaping the AC voltage for the load. This is done by creating the d-axis current reference for the inner current loop of the inverter. To do this, the error signal that is fed to the controller is computed as the difference in d-axis voltage reference and measurement. This loop can be represented by (29), and is seen in figure 3.10.
Reactive power control for the rectifier

The reactive power control is an outer loop control that creates q-component current reference to the inner current loop. This control is not mandatory for normal operation of the MMC, but provides additional benefits to the overall system.

The reactive power control for the rectifier is sometimes also called the AC voltage controller, as it can have stabilising effects on the upstream grid network. Using this control feature has the benefit of being able to support the grid during faults by injecting reactive power. In relative terms, this means that the converter consumes negative reactive power at the command of the control system. The reactive power control utilises the PI controller, with the error reference as the difference of positive d-axis voltage reference and the measured d-axis voltage. This is a feature that can potentially support the TSO’s grid from by helping to stabilise the voltage during faults. Figure 3.11 shows the loop using the d-axis voltage measurement and a set reference. The produced q-axis current reference should be limited during steady state operation, and once grid stabilisation is required, the limit can be lifted to the total rating of the rectifier.

Reactive power control for the inverter

Reactive power control for the inverter utilises the possibility of controlling the phase shift of the inverter voltage. If the reference q-axis current is set to zero, then the inverter output voltage will be phase-shifted to supply reactive power. If the q-axis current reference is calculated through the loop presented in figure 3.12, then the current will be phase-shifted, while the load voltage can be synchronised to the grid voltage. Equation (30) is used for the calculation of the q-axis current of the load. The ability of injecting
reactive power to the load beyond its needs is not possible, as it will only consume/produce the required apparent power. It is essential that the inverter is able to supply all reactive power demand of the load network, as it essentially is the "generator" for the load network. An enhanced method of increasing the reactive power capability is presented later in the thesis.

\[ I_q = \frac{Q_{\text{measure}}}{V_d} \]  

3.5.3 Inner Current Loop

The inner current loop is the main control-process of the VSC. With several inputs enhancing and controlling the different behaviour of the converter, it is the most complicated control loop. It operates in SRF as the previous loops, having two separate loops controlling each of the two current references, which is the d-axis and q-axis current. The inner current loop is identical for the rectifier and inverter.

From the mathematical model of the MMC, the converter control dynamics is decoupled with the feedback of the voltages across the internal inductance and resistance, enabling accurate tracking and preventing voltage droop. The two loops are controlled by the
means of PI controllers, fed by each of the loops errors, which is the difference between
the reference current and measured current. Going forward in the control system, the
regulated output of the PI controller is the new respective voltage reference, which is
summed up with the droop voltage and actual measured AC voltage, as seen in figure
3.13. It is further scaled with the measured DC voltage in per unit, to increase accuracy
and speed for tracking the references.

The inner current loop also accepts two external references from the outer loop, this is the
circulating current suppression control reference and the zero sequence control reference,
which is added onto the reference signal which will be used for pulse generation with
nearest level modulation.

\[ \text{Inner Current Loop} \]

\[ \begin{array}{c}
\text{i}_{d+}^* \\
\text{i}_{q+}^* \\
\text{i}_{d+} \\
\text{i}_{q+} \\
\text{V}_{d+} \\
\text{V}_{q+} \\
\text{V}_o \\
\text{m}_o \\
\text{V}_{dc} \\
\text{V}_{ref} \\
\end{array} \]

Figure 3.13: Inner current loop control in synchronous reference frame.

### 3.5.4 Circulating Current Suppression Control

The circulating currents in the MMC arms, as shown in the mathematical model, consist of
a DC component and a negative sequence double fundamental frequency AC component.
Circulating current suppression control (CCSC) is an outer loop control that effectively
suppresses the problematic AC component of the circulating currents in the VSC. It is
found implemented in most HVDC converter projects based on the MMC, as it reduces
component stresses, ratings, and losses, and it does not contribute to the power flow to
and from the DC bus. This circulating current comes at one cost: That it creates a high
frequency ripple in the DC bus voltage. In design, a trade-off between high frequency DC
voltage ripple and magnitude of the circulating current must be found unless the ripple
is filtered.

The CCSC works by feeding its reference to the inner current loop from the mathematical
model of the circulating currents. There are two main control architectures for CCSC that
are commonly adopted. The first is based on the proportional resonant (PR) controller,
which is able to control the AC signals without any transformation [31]. The second method is using dq0 transformation of measurements with PI controller, transforming the AC signal into dq0 reference frame to control it as a DC quantity [24]. It is important to note that the reference frame rotates with twice the fundamental frequency and in negative sequence direction as well. This rotating reference angle is based on the converters angular reference from the PLL, used for the dq0 transformation previously introduced.

Figure 3.14: Circulating current suppression controller in dq0 frame.
Chapter 4

System Design

Several guidelines exist for design practices used for HVDC stations today, for example technical brochures in CIGRE [9] [10] [11] [12], European commission regulations for HVDC [8], as well as recommended procedures from Det Norske Veritas (DNV GL) [13]. As some of these guidelines can be very comprehensive, they are not followed to every point in this thesis, but serve as an inspiration for several topics.

This chapter will present the energy aspect of the power quality conditioning system, as the main objective of the system is mitigation of voltage dips. The practical aspects and engineering of the back-to-back converter for the case study will also be presented, such as the network connection parameters, as well as design and ratings on component level. Lastly, special topics such as fault handling and extra features of the PQCS will be presented, which were presented in chapter 2.1.3.

4.1 Energy Storage Considerations

Understanding how voltage dips behave and understanding their statistical properties is important when it comes to designing the power quality conditioning system. As the back-to-back converter shall mitigate incoming voltage dips, a fundamental understanding of the need for stored energy is needed. In [16] the fundamental energy required for HVDC-MMC is introduced as 30-40 kJ/MVA per converter station, which for the back-to-back converter results in 60-80 kJ/MVA for the total system. This is normally used to assure that the voltage ripple in the submodule capacitor is below 10%, without any consideration to energy compensation. This chapter will further analyse the energy requirement of the total system based on voltage dip mitigation and statistics, and compare it to the original value from literature.
### 4.1.1 Dip Mitigation Strategies

The feature of dip mitigation is the power quality conditioning system’s most important requirement at CERN. The most severe transient fault condition in the overlaying grid is voltage dips for up to -50% in magnitude within 150 milliseconds. During these events, the converter should provide support in a way that ensures the electrical grid of CERN to have nominal voltage and constant power flow. This can be realised in two ways: By increasing the current drawn from the grid, and by supplying power from the integrated energy in the submodules of the rectifier and inverter.

The modular multilevel converter inhibits the internal submodule capacitor acting as an energy storage that ensures satisfactory voltage ripple and energy exchange between rectifier and inverter in such a way that the DC power interactions are not seen on the AC sides. The back-to-back converter already needs 60-80 kJ/MVA to ensure the satisfactory voltage ripple, which the converter must be designed for independently of chosen mitigation strategy.

#### Increased current control method

This mitigation strategy is realised by allowing the rectifier to increase the line current beyond the nominal value to cover the energy needs during the dip. An expected estimation is an increase in the current from between 1.2 to 1.4 per unit, with the initial storage of the MMC. This calls for increased component ratings for the rectifier to ensure that the reliability of the converter is not compromised, as operating beyond rated values, even for short duration, is not allowed. Another aspect are the upstream grid effects of drawing an increased current during voltage dips, as it may cause some unwanted transients and dynamics up to the power station. This solution was investigated in [7] using general back-to-back voltage source converters with an energy storage of 20 kJ/MVA in the DC bus. The paper concludes that by increasing the line current drawn from the grid to 2 times nominal current, the system is able to mitigate voltage dips of 50% magnitude for any duration. This solution is very interesting for the HVDC MMC, but the fact that the components of the rectifier must be heavily overrated in terms of current capability makes it a very costly solution.

#### Enhanced energy storage method

The better solution, which relies specifically on the features of the modular multilevel converter, is to optimise the internal energy storage in such a way that it is capable of mitigating the voltage dips. As described earlier, the rectifier can boost the DC volt-
age by increasing the line current. During a voltage dip, the rectifier will therefore be able to control the line current drawn from the grid to nominal value. This way, the current-rating of the components are capitalised on by drawing the maximum allowed power from the grid during a voltage dip. The rest of the energy needed by the load is supplied by the optimised submodule capacitors. For this aspect a dimensioning guideline can be established, similar to the existing value 60-80 kJ/MVA that is widely adopted. Having a larger energy-buffer brings other qualitative benefits as well, such as a more flexible compensation range. An example of this is the possibility of mitigating a total blackout for several milliseconds. The increased capacitance also reduces voltage ripple in the submodule voltage. In commissioning of the traditional HVDC MMC, increased capacitance is considered an unnecessary expense as dip mitigation is not of concern. In this thesis project, the enhanced energy storage method is chosen for dip mitigation, and a design guideline is presented in the next chapter.

4.1.2 Analysis of Voltage Dips

The analysis to be presented is based on the voltage dip measurements shown chapter 1, figure 1.2, which is available in appendix B. The thesis topic explicitly required that the system should compensate for the worst of cases, such as three-phase dips of -50% magnitude for 150 ms, which would require the maximum designed energy for mitigation.

Voltage dips possesses three categorising variables: The number of phases affected, their change in magnitude and the duration of the dip. The data set obtained does not specify the magnitude of change in every phase, only the worst phase. Thus, the assumption that the magnitude of the worst phase applies to the two other phases is made, this way, the missing information is accounted for while giving a positive margin. It should be noted that the voltage dip propagates from the upstream network through transformers of different connection (wye/delta) in such a way that it is reasonable to assume that all dips are of three-phase [2] (chapter 2.9). If data on every phase was available, the same study could be conducted using the average voltage magnitude of the three phases. For this analysis, two variables are left to consider: The magnitude of change referred to as dip magnitude, and the duration of the dip. With these two variables, a new function is introduced called dip severity. The dip severity is the product of the dip magnitude and dip duration as shown in (31).

\[
f(V, t) = \Delta V_{dip} \cdot t_{dip} = Dip \, severity
\]

The energy of any electrical system is defined by (32). In this equation, the two last variables are the same as defined for the dip severity.

43
\[ E = P \cdot t = I \cdot V \cdot t \] \hspace{1cm} (32)

Substituting (31) into (32) gives (33), which shows the “missing” energy caused by the dip, which must be compensated with the internal energy storage of the MMC.

\[ E_{\text{missing}} = I_{\text{dip}} \cdot \Delta V_{\text{dip}} \cdot t_{\text{dip}} = f(V, t) \cdot I_{\text{dip}} \] \hspace{1cm} (33)

Combining this result with the fact that the rectifier will draw nominal current during any voltage dip, a simplification can be done. By letting the current be 1 p.u in (33), the final equation summing up the relationship of the missing energy and the dip severity is shown in (34). This concludes that the dip severity is the missing energy, in the per unit system.

\[ E_{\text{missing}} = f(V, t) = \text{Dip severity} \] \hspace{1cm} (34)

A simple example of per unit calculation is performed in (35) using a three phase voltage dip of -50% magnitude, and a duration of 75 ms. The definition of energy in the per unit system is given by (36), where the base-value of time is 1 second.

\[ E_{\text{missing, p.u}} = 1 \text{p.u} \cdot 0.5 \text{p.u} \cdot 0.075 \text{p.u} = 0.0375 \text{p.u} \] \hspace{1cm} (35)

\[ E_{\text{base}} = P_{\text{base}} \cdot t_{\text{base}} = P_{\text{nom}} \cdot 1 \text{s} \] \hspace{1cm} (36)

The dip severity for the voltage dips recorded at CERN is presented in figure 4.1.(a), which is based on the data seen in appendix B. The dip severity is shown as a histogram with distribution-function that is fitted using MATLAB. The distribution function created from the histogram is the Log-logistical distribution, commonly used in statistics for random events and financial analysis. Figure 4.1.(b) shows the probability function in red, and the cumulative function, which is the integration of the probability function. The cumulative function portrays how the energy storage can be dimensioned based on the needed coverage of voltage dips, which is shown in the y-axis as percentage. What this figure concludes, is that the required energy to mitigate 98% of all dips, is half of what is required for 100%. This is a huge benefit as the internal energy storage can be reduced by half with sacrificing only 2% of the overall coverage. Information extracted from this graph is that 98% of all voltage dips that can be expected in the network, can be mitigated by supplying an energy of 0.0375 in per unit.
Figure 4.1: (a) Dip severity of all voltage dips causing a major event, with a fitted Log-Logistic distribution. (b) Representation of Log-Logistic probability function (red) and the resulting cumulative function (blue), also called confidence-band function.

To fit these statistical results into a more practical illustration, figure 4.2 shows the effect of two storage systems, one capable of discharging 0.075 p.u of energy, and the other of 0.0375 p.u. The essence of this figure is that all events above the selected energy-curve will be completely mitigated, while those under will only be partially mitigated. It is to be noted that the available energy presented in this figure is not the same as the installed energy, which is investigated in the next chapter. For the energy based mitigation strategy it is seen that the mitigation capability is very versatile. It can for example mitigate voltage dips of smaller magnitudes for an extensive period, or larger magnitudes for a very short duration. One limitation is the internal submodule capacitor time constant that defines how fast the capacitors can discharge to compensate a large drop in magnitude. It might be that the capacitors can only handle -50% voltage dip, and not -80% as theoretically shown in the figure, which illustrates the need for a very small time constant.
Figure 4.2: Measured voltage dips and the dip severity visualised - Blue curve is the 98% severity case, and red is the 100% dip mitigation case.

### 4.1.3 Energy Storage Calculations

As the theoretical energy needed to compensate the dip is calculated, the actual installed energy must be dimensioned based on the physical properties and the fundamental dynamics of the capacitor and the converter as a whole, with the statistical analysis as input. The energy of every submodule is given by equation (37), which shows that it is only dependent of the capacitor voltage. As the capacitor voltage diminished, the energy stored will be quickly discharged.

\[
E_c = \frac{1}{2} \cdot C \cdot V_c^2 \tag{37}
\]

To be able to reach steady state after such a discharge, a limit must be set so that the capacitor voltage can recover quickly. The time constant of the capacitor discharge dynamic shown in (38) should be reviewed, as it defines how quickly it can discharge the energy. As the equivalent capacitance and resistance of the system are very small, then the time constant will also be very small, giving the energy storage the ability to discharge very quickly.

\[
V_c(t) = V_0 \cdot e^{-t/\tau} = V_0 \cdot e^{-t/R \cdot C} \tag{38}
\]
Another aspect to review is how much the capacitors in the submodules can safely discharge, without sacrificing the integrity of the converter operation and power quality of the load. The threshold for discharging is decided by the steady state modulating index of the inverter. If the capacitors discharge below the set threshold, then the inverter will run in overmodulation, which generates harmonic distortion to achieve a constant RMS voltage for the load. Effectively, with a modulating index of 0.8, the inverter allows for the DC voltage drop to 0.8 p.u without sacrificing power quality. Thus, the capacitors must supply all the needed energy to mitigate voltage dips while discharging from 1 p.u to 0.8 p.u. From (37) the energy supplied from 1 p.u to 0.8 p.u of the DC voltage is 36% of the installed energy in the capacitors. Inverting this factor, it means that the installed energy capacity must be 2.77 times the theoretical energy storage needed.

An example of this is that if 10 MJ of energy is installed, then only 3.6 MJ can be discharged to mitigate, or the other way around, that if 3.6 MJ of energy is needed, then 10 MJ must be installed (a factor of 2.77). This calculation can be verified with a graphical solution as shown in figure 4.3, using equation (37), where the difference in energy between 1 and 0.8 p.u of voltage is 36%. It can be discussed whether or not the default modulating index could be adapted for this purpose, but it is not recommended as it affects other aspects such as electrical losses, a higher DC bus voltage and other aspects.

![Figure 4.3: Energy of a capacitor as a function of voltage.](image-url)
To conclude the energy calculations, for the 98% dip coverage system which needs 0.0375 p.u of available energy, the stored energy rating of the system must be 0.103875 in per unit (2.77 times larger). Imagining a one MVA system, this translates to 104 kJ/MVA. Comparing this to the value commonly adopted in literature, it is only slightly above the required energy for fundamental operation as 60-80 kJ/MVA. This result is plotted in figure 4.4 as the blue curve, together with the 100% coverage system needing 204 kJ/MVA as the black curve and the commonly adopted value of 70 kJ/MVA as the red curve.

It is important to note that the red curve representing the default energy of any MMC system, proves efficient in dip mitigation without any optimisation. Thus, a turnkey system would be able to have a voltage dip coverage in the range of around 93%.

![Figure 4.4: Voltage dip mitigation capability based on installed energy in the back-to-back system. Voltage dip data as presented in appendix B included. All voltage dips beyond selected curve will be mitigated.](image)

Figure 4.4: Voltage dip mitigation capability based on installed energy in the back-to-back system. Voltage dip data as presented in appendix B included. All voltage dips beyond selected curve will be mitigated.
4.2 System Level Parameters

4.2.1 CERN Electrical Network

For design of a back-to-back HVDC modular multilevel converter, several parameters must be defined before component design can be initiated. The required parameters are the grid parameters, transformer parameters and operating conditions for the converter.

The electrical network feeding the LHC is presented in figure 4.5. The main transformers EHT 4 & 5 are fed from the French grid operator RTE, and they operate in parallel with a total rating of 220 MVA. This equivalent is defined as transformer 1 for further study. The complete general services- and Meyrin network at CERN is not shown in the figure but can be seen in Appendix E. These two networks have an alternate distribution path fed by other transformers from the 400 kV RTE bus as well, so not all power is fed from transformer 1. Therefore, the transformers feeding the LHC machine directly are the ones connected to P2, P4, P6 and P8. The effective equivalent of these four feeding points is called transformer 2. By connecting the back-to-back HVDC MMC to the secondary side of EHT 4 and 5, the entire LHC machine network can be protected from one single converter of 220 MVA rating. The same applies to four individual systems of 38 MVA connected to each point of the LHC, at 18 kV level.

![Electrical distribution network feeding the LHC machine.](image)

The equivalent network parameters tied to the connection of the Large Hadron Collider at CERN is presented in table 4.1. As seen in figure E.1, cables are used to supply power from transformer 1 and to the 6 EHT102 transformers. All the cables are all shorter than 10 km and can be neglected for the study as the impact of the impedance is very low (it is proven as the diameter of the LHC is 8.6 km, and all cabling inside this radius would be shorter).
Table 4.1: Parameters for the LHC machine network at CERN.

<table>
<thead>
<tr>
<th>Network Parameters</th>
</tr>
</thead>
<tbody>
<tr>
<td>400 kV RTE:</td>
</tr>
<tr>
<td>Primary Voltage</td>
</tr>
<tr>
<td>short-circuit Power</td>
</tr>
<tr>
<td>X/R Ratio</td>
</tr>
<tr>
<td>Z0/Z1 Ratio</td>
</tr>
<tr>
<td>EHT4/5:</td>
</tr>
<tr>
<td>Rating</td>
</tr>
<tr>
<td>X p.u</td>
</tr>
<tr>
<td>R p.u</td>
</tr>
<tr>
<td>Voltage</td>
</tr>
<tr>
<td>Configuration</td>
</tr>
<tr>
<td>Grounding</td>
</tr>
<tr>
<td>EHT102:</td>
</tr>
<tr>
<td>Rating</td>
</tr>
<tr>
<td>X p.u</td>
</tr>
<tr>
<td>R p.u</td>
</tr>
<tr>
<td>Voltage</td>
</tr>
<tr>
<td>Configuration</td>
</tr>
<tr>
<td>Grounding</td>
</tr>
</tbody>
</table>

4.2.2 Voltage Level Considerations

Setting up the case study for protecting the LHC machine network against voltage dips, there are two available options. CERN has both a 66 kV network, as well as several 18 kV distribution networks as shown in figure 4.5. What this means is that there are two possible voltage levels and thus several possible solutions for size and connection voltage of the power quality conditioning system. As the distribution network at 66 kV is connected with cables to the 18 kV networks, then there is low risk of voltage dips originating in these networks, making both voltage levels a valid placements of the system. When assessing the most beneficial solution, the alteration of the surrounding grid is not considered. This means that a system placed at the 66 kV level must have a rating of 220MVA. Otherwise, a new transformer would have to feed the cables L1 and L9 so that a 160 MVA system at 66 kV can be realised. It should also be noted that four systems of 38 MVA at 66 kV is not feasible, because of the high voltage requirement for compared to the system rating, which would require excessive investment.

The possible solutions are as follows:

1. One 220 MVA system connected to 66 kV.
2. Four 38 MVA systems connected to 18 kV.
The first system needs power electronics rated for 220 MVA, while the second only needs a total rating of 160 MVA. While this can seem like a big advantage to go for the smaller converters, it is known in the HVDC industry that bigger is better. Firstly, a 220 MVA system would have a higher efficiency than several smaller ones, and secondly, it utilising the fact that it will have more submodules, and thus more levels, which further enhances the quality of the system. This implies that the bigger system would not require harmonic filters, while four smaller converters most certainly would require harmonic filters on both rectifier and inverter side. There are also less civil engineering costs for one bigger system than several smaller ones, and less overall components and complexity in maintenance.

The thesis topic description originally expected detailed component specifications for both the 66 kV and 18 kV connection points for the back-to-back system. Since the 66 kV solution for a 220 MVA system is identified as the most advantageous solution, the sole focus of the thesis is put into the study at these ratings.

Figure 4.6: The LHC machine network with the BTB HVDC system to be studied.
4.2.3 Converter System Parameters

From the network parameters, the individual rectifier and inverter should be rated for 220 MVA for this study. From theory and selection of steady state operation condition, a modulation-index of 0.8 is commonly adopted from literature [14] as it is a good trade-off between regulation-range and efficient design of the power electronics. With this modulating index, the operating voltage of the HVDC-MMC converter is:

\[ V_{DC} = \frac{V_{LL}}{0.612 \cdot m} = \frac{66kV}{0.612 \cdot 0.8} = 134.8kV \]

During a voltage dip while at maximum operating power, the rectifier will not be able to regulate past the nominal current and sustain the DC voltage. Thus, the inverter will operate at lower DC voltage while increasing the drawn DC current. Where modulating index is at maximum (m=1.0) the DC voltage will regulate to a minimum of:

\[ V_{DC_{min}} = \frac{V_{LL}}{0.612 \cdot m_{max}} = \frac{66kV}{0.612 \cdot 1} = 107.8kV \]

While the inverter is operating at this DC voltage, the maximum DC current is achieved. Operating beyond this, the inverter is not allowed to go into over-modulation, and therefore the current will not increase beyond this maximum value.

The dimensioning DC voltage for the system will be 135 kV, which will be imposed on every individual arm of the converter. The total blocking voltage of all submodules should thus be rated for this as maximum DC voltage. The required number of submodules and their individual voltage ratings will be reviewed in the component design section.

Current Calculations

Internal losses are not accounted for in the systems calculation, as the complexity increases while the accuracy is negligible. Knowing that the phase currents for the system are constant in steady state as well as during a dip, and circulating currents are suppressed, the currents at both inverter and rectifier side is calculated as:

\[ I_{phRMS} = \frac{S}{\sqrt{3} \cdot V_{LL}} = \frac{220MVA}{\sqrt{3} \cdot 66kV} = 1.92kA \]

The maximum nominal DC power is 220 MW, thus the maximum DC current is:

\[ I_{DC,\text{max}} = \frac{P_{DC}}{V_{DC,\text{min}}} = \frac{220MW}{107.8kV} = 2.04kA \]
This is an abnormal state, only reached during special operating conditions of the MMC when modulation index reaches one. The steady state DC current is 220 MW/135 kV = 1.62 kA. During this condition the AC line currents from the grid are still at nominal value. As the DC current and phase current are calculated, the arm current parameters can also be calculated. The arm current is composed of three components, a DC component, an AC component of fundamental frequency and the circulating current as negative double-fundamental component, where the latter one can be considered non-existent as it is suppressed with by the control system. During the worst-case operation the maximum arm current is defined by the maximum DC current. The currents can be calculated as:

\[
I_{\text{arm,DC,max}} = \frac{I_{\text{DC,max}}}{3} = 0.68 \text{kA}
\]

\[
I_{\text{arm,RMS}} = \sqrt{\left(\frac{I_{\text{DC,max}}}{3}\right)^2 + \left(\frac{I_{\text{ph,RMS}}}{2}\right)^2} = \sqrt{\left(\frac{2.04 \text{kA}}{3}\right)^2 + \left(\frac{1.92 \text{kA}}{2}\right)^2} = 1.176 \text{kA}
\]

\[
I_{\text{arm,peak,max}} = \frac{I_{\text{DC,max}}}{3} + \frac{I_{\text{ph}}}{2} = \frac{2.04 \text{kA}}{3} + \sqrt{2} \cdot \frac{1.92 \text{kA}}{2} = 2.035 \text{kA}
\]

The steady state arm currents of the system can be calculated based on the equations presented so far. The steady state RMS current of the arm is calculated to 1.10 kA while steady state peak arm current is 1.9 kA. This gives the system a required current rating of 6.5% higher for the RMS and 6.1% higher for peak, compared to steady state operation. A safety margin will be evaluated when choosing the internal submodule components with industrial solutions in mind.

![Figure 4.7: Overview of converter and network system parameters.](image)

Figure 4.7 shows the overall simplified network and system parameters that will be applied for the simulation study at a later stage. There the load system will be defined more clearly, as well as the equivalent which transformer 2 represents.

To conclude the current calculations, the maximum DC current, the peak values, and the RMS of these will be the dimensioning values for the submodules of the inverter and rectifier. As the necessary parameters on system level for the converter is calculated, the design on component level can be further investigated.
4.3 Converter Component Design

The modular multilevel converter introduced in chapter 3 consists of multiple submodules, which are built up of several components. The submodules of such a converter are identical, featuring a modular construction. As the previous chapter calculated the required parameters, the submodule can now be designed. This part focuses on how to dimension the main components of the submodule, as well as reviewing important aspects which should be kept in mind. Figure 4.8 shows the submodule as a two-terminal device, with its main components and overall systems which will be reviewed.

![Detailed overview of the MMC submodule](image)

Figure 4.8: Detailed overview of the MMC submodule - Including mechanical switch and thyristor bypass switch, IGBTs, submodule capacitor, voltage sensor, cooling loop, and auxiliary system design.

4.3.1 Submodule Switching Devices

The submodule inhibits two IGBT modules, which can consist of one or several series connected switching devices. The two key parameters for the dimensioning of IGBT modules are their current and voltage ratings. For any IGBT module used in MMC and HVDC applications, it is typical in the industry to derate the voltage provided by the data-sheet to a range of 50-70%. This is done so that the switch can fully utilise the current rating with a safe margin and for transient voltages that might appear. After this derating, the IGBT module voltage must match the voltage provided by the submodule capacitor. Table 4.2 shows the industrial voltage ratings of the IGBTs, with the derating values that will be used in further calculations. When looking at the industrial devices available, it should be known that it is beneficial to use switches with the highest voltage rating that can handle the maximum arm current. The current capability needs to be rated for the maximum arm current that is expected in the converter, and must be calculated for the...
worst operational case, that is when the modulating index is one for both rectifier and inverter. This is thus 0.68 kA as the DC component, 1.176 kA RMS and 2.035 kA as the peak value, as previously identified.

Table 4.2: Nominal and derated voltage rating of industrial IGBTs.

<table>
<thead>
<tr>
<th>Industrial Standard</th>
<th>Derated Value</th>
<th>Percent Derating</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.7 kV</td>
<td>1 kV</td>
<td>58.8%</td>
</tr>
<tr>
<td>3.3 kV</td>
<td>2 kV</td>
<td>60.6%</td>
</tr>
<tr>
<td>4.5 kV</td>
<td>2.7 kV</td>
<td>60.0%</td>
</tr>
<tr>
<td>6.5 kV</td>
<td>3.9 kV</td>
<td>60.0%</td>
</tr>
</tbody>
</table>

The available IGBT-modules in industry exist in two packaging options, wire-bond and press-pack-modules. The wire-bond modules are often cheaper, with greater choice of ratings and providers, and more suitable for design where series connection of switches is limited. The press-pack option allows for easier series connection of the modules, has excellent thermal properties, and when a switch fails, it goes into a permanently closed state which is useful for failure conditions [32]. On the other hand, press-pack modules can be expected to be more expensive because of the added beneficial features, as well as the limitation in providers. A connection solution of clamps is also needed, as well as custom cooling plates that conduct. The wire-bond module is therefore identified as the most economic solution for the application and will be used for further study.

Series Connection of switching devices

One crucial aspect is how to choose the number of submodules and their individual voltage to reach the rated DC bus voltage. Assuming that the semiconductor switch with the highest voltage rating for the appropriate current rating is used, there are two options: To increase the number of submodules installed, or increase voltage rating of the submodule by increasing the amount of switches connected in series.

The latter solution is commonly used for very high DC voltages where it is not feasible to increase the number of submodules. One concern is the need of maintaining equal voltage distribution across the series switches, which is realised by snubber circuits and grading resistors in practical converters. It is also important to have reliable gate drivers for the series connected switches, as they must fire at the same time with high precision. This in turn increases complexity, losses and component count and degrades the reliability. The benefit of using series connection is simpler auxiliary distribution, fewer voltage sensors for the module capacitors and mechanical design aspects. With series-connection the individual modules will be larger and heavier as the converter still needs the same number of capacitors and energy, and having redundant modules will be more expensive. Having
smaller modules that are easier to maintain and handle, for example with replacement or diagnostics is beneficial.

For the rest of the design review, series connection of semiconductor switches will not be further investigated as it introduces several drawbacks compared to having single switches in the submodules.

**Industrial Standards and Ratings**

The switching modules available as off-the-shelf solutions are presented in table 4.3, with their respective voltage rating and collector current rating, which is the DC current the module can handle. Another important design parameter for the current is the maximum peak current rating, which is exactly 2 times the collector current for most industrial IGBT devices. The maximum calculated collector current required is 0.68 kA, while the maximum peak current is 2.035 kA, using the previous calculations. A safety margin of 10% to 20% can be applied towards the nearest industrial standard available. A device with a collector current ‘Ic’ of 1.0175 kA or higher is required, as the maximum peak current is the dimensioning value.

The 6.5kV IGBT modules have an ‘Ic’ rating of 1 kA, while the 4.5 kV module have 1.2 kA, and the 3.3 kV module 1 kA, 1.2 kA and 1.5 kA. Voltage should be the priority as it decreases the amount of switching devices and thus number of modules needed without series connection. Economic aspects can imply that the most powerful module, the 6.5 kA at 1 kA, is more sought after and thus more expensive with only one provider/manufacturer today. Thus the 6.5 kV, 1 kA module must be weighed against the 4.5kV module at 1.2 kA, which have several manufacturers and better tendering opportunities. Now, as the submodule needs a current rating ‘Ic’ of 1.0175 kA, the 6.5 kV module is not an option, as it leaves little room for an added margin in the rating.

**The 4.5 kV, 1.2 kA module** is the superior switching device, as it enables the most economical solution. An example of such a IGBT module is the FZ1200R45HL3 from Infineon [33], which will be used for this thesis in the following chapters. For future applications, the IGBT development should be followed as the ratings will increase, and the most powerful modules today will become cheaper as the big consumers move onto the larger flagship modules that will enter the market. It should be noted that if a higher margin for current capability is required, then the 3.3 kV module with 1.5 kA is a possibility. On the other hand, by using this module with lower voltage, more submodules would be required.
### Table 4.3: Industrial ratings for wire-bond IGBT modules.

<table>
<thead>
<tr>
<th>Current rating:</th>
<th>Voltage rating:</th>
<th>1.7 kV</th>
<th>3.3 kV</th>
<th>4.5 kV</th>
<th>6.5 kV</th>
</tr>
</thead>
<tbody>
<tr>
<td>400 A</td>
<td>I, S</td>
<td>-</td>
<td>I</td>
<td>-</td>
<td>A, I</td>
</tr>
<tr>
<td>500 A</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>A, I</td>
<td>-</td>
</tr>
<tr>
<td>600 A</td>
<td>I, S</td>
<td>-</td>
<td>-</td>
<td>A, I</td>
<td>-</td>
</tr>
<tr>
<td>650 A</td>
<td>-</td>
<td>-</td>
<td>A</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>750 A</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>A, I</td>
<td>-</td>
</tr>
<tr>
<td>800 A</td>
<td>-</td>
<td>A, I</td>
<td>A, I</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>1000 A</td>
<td>-</td>
<td>A, I</td>
<td>-</td>
<td>A</td>
<td>-</td>
</tr>
<tr>
<td>1200 A</td>
<td>I</td>
<td>A, I</td>
<td>A, I</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>1500 A</td>
<td>-</td>
<td>A, I</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>1600 A</td>
<td>A, I</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>1800 A</td>
<td>A, I</td>
<td>A</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>2400 A</td>
<td>A, I</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>3600 A</td>
<td>A, I</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
</tbody>
</table>

A = ABB, I = Infineon, S = Semikron

### 4.3.2 Submodule Capacitor

The submodule capacitor is the second main component for the function of this converter. It acts as an energy buffer, which allows the converter to reach the required DC voltage by charging and discharging dynamics. The crucial fact for this capacitor is that the arm current flows through it when it is switched in on-state by the IGBTs. This means that every capacitor must be dimensioned for the maximum allowed arm current of the converter, which increases the difficulty of choosing the right capacitor. In today’s industry, capacitors for this application can reach currents up to 1 kA, but it might be necessary to have several of these in parallel if the arm current exceeds the capabilities of a single unit. The voltage rating of the capacitor must match the voltage of the submodule. In practical design, often the capacitor decides the voltage of the module. The capacitance is dimensioned as needed, with energy storage in mind. To reach the desired energy and voltage rating, paralleling and series connection might be needed. Capacitors used for MMC application are typically dry-type metallised film, known for their self-healing properties and the eliminated risk of oil leakage. Several of the industrially available capacitors are made for MMC use, both in automotive applications and in converters for power transmission purpose. This is the DryDcap from ABB or E59 from Electronicon, whose parameters are listed in table 4.4.

From the IGBT design, the 4.5 kV module is chosen for a conceptual design. With a derating of 60%, the submodule will be rated at 2.7 kV. The dimensioning current for the capacitors is the RMS current, as it contributes to the losses and heat generation. The dimensioning RMS current of the submodule capacitors is 1.19 kA. From the parameters
Table 4.4: Industrial capacitor standards for MMC application.

<table>
<thead>
<tr>
<th>Type</th>
<th>Voltage rating</th>
<th>Current rating</th>
<th>Capacitance</th>
<th>Energy</th>
</tr>
</thead>
<tbody>
<tr>
<td>ABB DryDCap [34]</td>
<td>Up to 4 kV</td>
<td>Up to 1 kA</td>
<td>Up to 200 mF</td>
<td>Around 20 kJ</td>
</tr>
<tr>
<td>Electronicon E59 [35]</td>
<td>Up to 4 kV</td>
<td>Up to 1 kA</td>
<td>Up to 10 mF</td>
<td>Around 20 kJ</td>
</tr>
</tbody>
</table>

Presented in Table 4.4, it is concluded that two capacitors must be connected in parallel to reach the required current capabilities. From industry, the capacitance manufacturing tolerance is about ± 10% in every capacitor, with the self-healing process could lead to an additional capacitance deterioration of -20% in the course of the lifetime. Thus, the capacitance should be rated with an added 20% margin.

It is known from the energy storage analysis that the converter will require 104 kJ/MVA of converter rating to cover most voltage dips. For the 220 MVA back-to-back system, this is translated to a total of 22.88 MJ, or 1.91 MJ per converter arm. To continue this calculation, the number of levels must be established through equation (39).

\[ N = \text{ceil}(V_{DC}/V_{sm}) = \text{ceil}(135kV/2.7kV) = 50 \]  

(39)

The converter will consist of 50 modules and operate as a 51 level MMC for both rectifier and inverter, with the redundant submodules coming into consideration at a later stage of the thesis. With total arm energy of 1.91 MJ, this means that each individual module has 38.2 kJ of installed energy. The submodule capacitance is calculated to 10.48 mF using formula (40).

\[ C_{sm} = \frac{2 \cdot E_{sm}}{V_{sm}^2} = \frac{2 \cdot 38.2kJ}{2.7kV^2} = 10.480mF \]  

(40)

This means that for the case when two capacitors are connected in parallel to share the current, each capacitor must be 5.24 mF. Calculated with a 20% margin, this means 6.288 mF each. Thus, each capacitor must be rated for 2.7 kV, with a current of approximately 600 A and capacitance of 6.288 mF. From the data-sheet of Electronicon E59 DC capacitor [35], a good fit is found as the model with dimensions of 520x175x880 mm, having a volume of 100 litres and weighing approximately 110 kg. Each submodule will then have 220 kg of capacitors.

4.3.3 Arm Inductance

The arm inductance, also called DC inductance, has several functions in MMC application. Firstly, it limits the rise of current during short-circuit and the second harmonic circulating currents, and secondly it allows the converter to control the reactive power. Each arm has one equivalent inductance, for both rectifier and inverter, totalling to 12 arm
inductances. In practical aspects, these are realised as outdoor air-core reactors, either stackable in height or centre-tapped, effectively reducing component count by covering both the upper and lower arm. A typical value gathered from literature is to dimension the arm inductance to 0.15 p.u of base AC input [21]. This value could be optimised further, as the converter will be covered by circulating current suppression control, effectively reducing the circulating second harmonic currents. If the converter is well protected against short-circuit currents, this inductance could be reduced from the value introduced in literature. The inductance is considered a qualitative variable, only determined by the needs for short-circuit protection and circulating currents. Once the inductance and arm currents are known, the apparent power rating must be the product of ohm’s law, set as the maximum arm current squared, times inductance in per unit. Insulation level should correspond to the AC voltage of the grid connection.

4.3.4 Gate Driver and Auxiliary Power

The IGBTs needs to be controlled through gate drivers located in the submodule. This introduces a design challenge, as these drivers need power to generate gate pulses. The importance of this is to have a power source that is not connected to local ground that the converter utilises. A solution to this challenge is to siphon power from the submodule capacitor, and depending on the voltage level and auxiliary power requirement, there are two possibilities as presented in [21], (chapter 2.8). If the power requirement is low (1 to 10 W), the power siphon can be realised by a simple resistive voltage divider together with a small galvanic transformer. If power requirement is higher, the first solution will be less efficient with current squared, and a DC/DC converter together with galvanic isolation is needed. Another solution is to create a separate feeding bus-bar system from an isolated source, connected to auxiliary emergency power source.

4.3.5 Cooling and Mechanical Equipment

The losses of a modular multilevel converter is presented in [36] as approximately 99.5\% per converter. This is under ideal conditions, and for a back-to-back system with two converters, the ideal efficiency is theoretically 99\%. A common margin applied is to use 98\% efficiency for a back-to-back MMC system, with the possibility of optimisation.

The losses of the system will dissipate as heat, and since the surrounding air would heat up relatively quickly, an external cooling solution must be installed. It is typical to employ a water-to-water cooling system for these HVDC converters in populated areas, utilising special coolant or de-mineralised water.
When constructing the mechanical assembly of the converter, modularity is of essence. The submodule should be considered as a two-terminal device, meaning that it should only require two bus-bar connections for the main powering. The modules should be easy to access if replacement is needed and should be mounted in brackets to allow for a lifting mechanism to easily insert and remove a single module. This is important as the modules can weigh a lot, primarily because of the capacitors. The converter module assembly should also be constructed with isolated spacers, ensuring no connection path and respecting the required creepage/clearance distance in air for the individual submodule voltage.

4.4 Fault Operation and Handling

Protective systems are a very important part of the overall system as the converter is susceptible to malfunction if operating outside the operational limits. The back-to-back HVDC system is vulnerable to many types of faults, and as such, protective measures must be made. These faults are represented in figure 4.9. This figure is a graphical representation of fault locations, and for the grid and load side faults, phase-phase faults also apply. The submodule fault (c) represents all malfunctions of the submodule, and it is not limited only to short-circuit to ground.

Figure 4.9: Fault scenarios in the BTB HVDC converter. (a) Shows the grid-side fault. Figure (b) shows the load-side fault, (c) the submodule fault, (d) DC fault (pole-pole), and (e) DC fault (pole-ground).
4.4.1 AC Grid Fault

The converter must be designed for a possible fault situation located in the upstream grid. Unlike the voltage dips that the converter is designed to feed constant power to load, the possibility of having a more severe fault is exist, such as a three-phase short-circuit. In such cases, the main objective of the converter is to ride through the fault without tripping, while ensuring that it can reach steady state operation quickly after the fault is cleared. Naturally, the converter control system will maintain the power supply to the load as far as the energy storage is dimensioned. If the faults are less severe, example short-circuits with high resistance to ground, the converter will treat it as it does with voltage dips, working to maintain the integrity of the load by drawing power from the healthy phases of the grid combined with the energy of the internal storage.

4.4.2 Load Network Fault

The back-to-back MMC is a sensitive system, not able to operate while providing high short-circuit currents. This rises concern on how selectivity is obtained if a fault in the load network is present. If the converter cannot supply the short-circuit current at fault location, as well as to the other distributed loads that are healthy, then the fault will draw all energy present and the rest of the load network will be compromised. In most cases with short-circuit to ground, the short-circuit current is limited by a high grounding resistance at transformer connections, where the fault is detected as well. The most severe case is thus identified as the three-phase short-circuit, where the fault is localised close to the converter. This type of short-circuit is also be of concern further downstream, if the short-circuit currents are very large.

A possible solution to ensure the selectivity is to enable an active bypassing mechanism to supply the short-circuit current from the mains of the upstream grid directly. The challenge with this is to detect if such an event is present, that would require increased supply of short-circuit current. One method is to measure the rise of current to a certain threshold, as the converter should be capable of supplying 1.1 times the nominal current. If this happens, it could bypass to feed the potential short-circuit, and return to normal operation once the downstream fault is cleared. In addition, if this was a false trip, the integrity of the load network is not affected by the transition between converter supply and direct grid supply, as this would require to be seamless.
4.4.3 Active Bypass System

In the case that the converter must be shut down, or is unavailable, it is of great importance to have a system that can bypass the converter such that the load network remains connected to the grid. AC breakers would be an effective measure, but if fast switching is needed, active devices should be used. Considering this, the bypass system can be designed with normal breakers combined with a static thyristor-based AC switch. The thyristors can be fired when fast transient events cause the need for it, while the breakers can enable the bypass for longer duration, for example during a maintenance or sudden unavailability. If the converter detects a situation that requires blocking of the current, to protect the components, a signal would be sent to both inverter and rectifier to block all IGBTs, and to fire the thyristors to instantly bypass the system. This solution can be used to supply the short-circuit currents previously discussed, to ensure selectivity of the downstream network without re-designing the protection systems. The proposed static thyristor AC switch is shown in figure 4.10, in parallel with the back-to-back HVDC MMC.

The control system of the MMC lets the load network AC voltage be synchronised with the grid AC voltage, so that if a fast bypass-switching is performed, then there is no sudden phase-displacement seen from the load. It is important to state that the inverter will supply the required reactive power to the load and leakage inductances in transformers, and that the bypass system must overtake this delivery when it connects. At any time, there might be a small phase difference between the voltages between the grid and load, which will define the blocking voltage of the thyristors when idle.

The static thyristor switch must be dimensioned based on the line current from the grid, and the voltage defined in (41). If the grid and inverter are synchronised, the phase voltages will be of same magnitude and polarity, and the effective dimensioning blocking voltage is close to zero, as shown by (41).

\[
V_{\text{bypass}}(t) = \frac{\sqrt{2}}{\sqrt{3}} \cdot V_{\text{grid}} \cdot \sin(\omega t) - \frac{\sqrt{2}}{\sqrt{3}} \cdot V_{\text{load}} \cdot \sin(\omega t + \theta) \quad (41)
\]

If the synchronisation between grid and load is not guaranteed, then the blocking voltage must be dimensioned after (42), for when they are of opposite polarity and maximum amplitude.

\[
|V_{\text{bypass}}| = 2 \cdot \sqrt{2} \cdot V_{\text{base}} \cdot \sin(\omega t \theta) \quad (42)
\]
Figure 4.10: The static thyristor AC switch for bypassing the converter.

4.4.4 Submodule Bypass System

The bypass system of each submodule consists of a controllable thyristor rated for high current and the module voltage, and a mechanically spring-loaded load switch. This principle is commonly used for half-bridge modules in MMC application as they are not well protected against faults in the DC bus and internal faults in general. The bypass solution allows for a gentler fault diagnosis process and allows for elimination of faulty modules to ensure redundancy. If a fault of unknown location is detected in one submodule, then the thyristor can help localise the exact module while providing a conduction path as to not interrupt the converter. The redundancy of this converter is ensured by the load switch, permanently bypassing a faulty module until it can be replaced or diagnosed during a scheduled maintenance. The bypassing thyristor-switch must be dimensioned based on the rated submodule voltage, and the peak short-circuit current of a DC fault in the DC bus between pole and ground. This means it should be able to handle the highest peak current for short duration and the RMS of the short-circuit for the time it takes to clear the fault with blocking operation. The thyristor is only allowed to conduct on the current path until the zero crossing, and can only conduct in one direction, thus it would not be wise to let it operate continuously with the parallel bypass IGBT module. During an internal short-circuit the thyristor should be able to conduct and redirect the fault current from the IGBT modules, which have a lower tolerance to overcurrent.
4.4.5 Submodule Fault

If a submodule was to fail during operation, the controls must detect this immediately and fire the internal bypassing thyristor to withstand the possible short-circuit currents, or to ensure operation of the converter arm if an open state fault is present. Table 4.5 shows the most probable cases of fault in the submodule, and the method of detection. The issue if an open state is present in the converter arm is that the arm current will not be allowed to flow. This means that the converter would not work in this state and that the fault module must fire its thyristor to ensure a conduction path. The challenge here is to detect if either of the IGBT or gate drivers are faulty, as the capacitor voltage would not give any indication. In the cases where only the submodule voltage can be detected as relatively constant or charging/discharging beyond a certain threshold even if the balancing strategy is employed, it can be assumed defective and the localization of this module is pinpointed very fast. In the case of IGBT module fault, detection is a bit more challenging. Two localization methods for open circuit faults are presented in [37], one to detect abnormal ripple dynamics in the arm current, and the other to calculate the submodule capacitance at every sampling time using the arm current and submodule voltage.

<table>
<thead>
<tr>
<th>Case</th>
<th>Component fault:</th>
<th>Detection</th>
</tr>
</thead>
<tbody>
<tr>
<td>I</td>
<td>IGBT 1 (T1)</td>
<td>Special algorithm</td>
</tr>
<tr>
<td>II</td>
<td>IGBT 2 (T2)</td>
<td>Special algorithm</td>
</tr>
<tr>
<td>III</td>
<td>Gate Drivers</td>
<td>Special algorithm</td>
</tr>
<tr>
<td>IV</td>
<td>SM Capacitor</td>
<td>Measurement of voltage</td>
</tr>
<tr>
<td>V</td>
<td>Voltmeter</td>
<td>Measurement of voltage</td>
</tr>
</tbody>
</table>

4.4.6 DC-bus Fault

A fault in the DC-bus of the MMC converter have the potential to be fatal and destroy the converter if not protected. The equipment in the DC-bus should be carefully reviewed and reduced to eliminate the possibilities of having a short-circuit. As the DC bus will be realised by indoor bus bars over a very short distance, the probability of a fault can be eliminated by mechanical design. It is already known for point-to-point HVDC, which involves overhead lines or cables that pole-to-pole fault are very rare, and that pole to ground fault is the most common among DC faults. Whether or not to employ a strategy for protection of the converter station is a difficult decision to make. It entails having special detection of fault condition and thyristor bypass switches for every submodule. Nonetheless, being prepared for a pole to ground fault should be considered, as human
factor could be one of the causes. If the fault is detected in the converter, then the protective bypass thyristors in each individual module should fire as the IGBTs are blocking. Then the AC breakers should disconnect to extinguish the energy supplied from the grid to the fault, while the static thyristor AC switch is supplying power to the load.

4.5 Transformer-independent Converter

4.5.1 Transformer-less Connection

The HVDC VSC topology offers the option of going transformer-less, that means no extra transformer will be needed for the converter, neither on the input and output. It is popular in the industry to insert a wye/delta transformer on the input of an HVDC station, and a delta/wye on the output such that the zero currents are isolated and not allowed to flow between the converters. The zero currents can also be limited by using floating neutral wye transformers. By installing these transformers, an increase in cost and maintenance is required, and additional spare parts. If an installation of a completely new grid system with a potential back-to-back converter is considered, it will need transformers anyway; example is 400 kV to 66 kV, and 66 to 18 kV, the investment in wye/delta transformers might be worthwhile for better performance and reduced cost in control systems. If the installation of such a back-to-back converter was to happen in an existing grid with transformers already installed and operating without delta connection, then the transformer-less connection is a big advantage as any transformer configuration will work. The zero currents can cause big damage to the converter if allowed to flow, as they are a three-phase DC quantity. This can happen during asymmetrical faults on either side of the back-to-back converter, and in turn create power oscillations in the DC bus as well as disturb the output voltage/current and create imbalance in the isolated CERN grid.

This control system for the zero current is used for applications where bulky transformers are at a huge disadvantage, such as in offshore platforms where physical space is limited, as well as for places where it is not feasible to install a new transformer. It is an established technology already used but it needs testing in simulations for proof of concept with more advanced control systems, mainly positive and negative sequence dq0 transformation, where negative sequence is suppressed.

To be able to control the zero sequence currents flowing through the converter, the zero-sequence control loop must be implemented for the converter. It operates in alpha-beta-zero frame where the zero current is of AC quantity. The proportional-resonant (PR) controller is then tuned and able to control the zero-sequence reference, fed to the inner
current loop. The loop is shown in figure 4.11. It works by injecting an opposite zero sequence to cancel out the unwanted current flowing in the system. This method of control is presented in [38].

![Zero Sequence Controller](image)

Figure 4.11: Zero sequence current controller - Using PR regulator.
Chapter 5

Simulation Studies

5.1 Simulation Model

5.1.1 Matlab & Simulink

Matlab & Simulink is a well-developed simulation environment used for numerical analyses. The extension, SimPowerSystem, developed by Hydro Quebec is a tool included with Simulink used for electromagnetic transient (EMT) simulation. With this, electrical systems based on linear and non-linear components can be effectively simulated in great detail. It is commonly used for power electronics, rotating machines, grid analysis and load flow studies. In this thesis, Matlab & Simulink 2018b is used, with SimPowerSystem.

5.1.2 Aggregate MMC Model

As simulation-models become more detailed and advanced in the field of power electronics, it is natural that they become more process demanding to compute, and as such require more time to simulate. The main objective is to simplify the simulation models as much as possible, while keeping the necessary details and dynamics to still be scientifically accurate. When simulating the modular multilevel converter, there can be hundreds of semi-conductor switches actively switching on and off while operating at a high sampling rate, with many non-linear dynamics operating at the same time. To increase performance, the strategy of aggregate modelling has been introduced to the MMC model, introduced in the SimPower extension of SIMULINK. This increases simulation time by orders of magnitude while keeping the internal dynamics. The aggregated model of the MMC relies on assuming perfect capacitor balancing, so that all submodules in each individual arm are connected to the same duplicated capacitor. Since capacitor voltage balancing is only
a physical property that is solved with computational power by sorting the measurements and generating the correct pulses, it has no effect on the result of the simulation to assume perfect condition. At the same time, the entire arm is simulated as one unit, where the modulating signal decides the equivalent total submodule voltage inserted. The losses, blocking operation and circulating current are still kept. Essentially, each converter arm is modelled as a variable series capacitor voltage source, as seen in figure 3.4 in an earlier chapter. With this strategy, a very high amount of submodules in the converter can be simulated efficiently.

The limitations of the aggregated model is that individual submodule fault cannot be simulated, and that the capacitor balancing scheme cannot be documented.

Development of the model

The model was developed through literature review of HVDC MMC control strategies and operation, using several books and international publications [22], [12], [39], as well as with experimentation. The online course “Multilevel Converters for Medium/High-Power Applications” [40] was also used as inspiration and to learn the fundamentals of MMC.

For a remote-end back-to-back MMC converter operated under unbalanced network conditions, there are no complete works of such a control system for the specified application in this thesis at the time of writing. Thus, the works of several separate systems have been combined, such as synchronous reference frame control, circulating current suppression control, zero sequence control, islanded mode operation, and more. The development of the simulation model has been the most time-consuming task of this thesis and consists of over 250 hours of modelling and parameter refining. It has been done in the following steps:

1. Simulation of individual devices such as IGBT and thyristor switches controlled with simple pulses, together with three-phase generation and load systems.
2. Development of a simple three level voltage source inverter, showcasing operation and function using open loop controls without feedback.
3. Development of simple low-level converters using closed loop control systems, for example an inverter with an ideal DC source representing the rectifier.
4. Model development of the 'N' level inverter with ideal rectifier and closed loop control, with verification of control systems working optimally.
5. Combining the 'N' level inverter and rectifier as the back-to-back HVDC MMC system, and simulating voltage dip scenarios and recording results.
5.1.3 Simulation Parameters

The arm inductance is included as 0.15 p.u, and circulating current suppression is enabled. An internal arm resistance of 0.03 ohm is included, representing the IGBTs based on realistic values. The DC voltage is 135 kV, with a steady state modulation index of 0.8 for inverter and rectifier. The rest of the parameters for controllers, base values, etc. can be seen in appendix D. A discrete variable-step solver is selected in the simulation environment, with a step-size of 20 microsecond. This gives a large resolution in the measured signals and keeps satisfactory details of the power system simulation. The tuning of the PI controllers are performed with parametric study, where a Matlab-script performed hundreds of simulations while changing the proportional and integral constant automatically and recording the responses. This method can be run while the computer is otherwise not used for computational power, and can tune several controllers simultaneously. This script is seen in appendix D.

The simulated transformers of the system is based on the parameters presented in table 4.1 in the previous chapter. Transformer 1 is the two 110 MVA transformers operating in parallel, with the same per unit rating form the table. Transformer 2, on the other hand, is simulated as the equivalent of the EHT102 transformer, scaled to 220MVA rating. This is done to represent the network in the most realistic way. With this, the four feeding points of LHC, as introduced earlier as P2, P4, P6 and P8 is simulated as one equivalent load system, for simplification of the simulation model.

Simulating realistic loads for the system is very important to give a good representation of how it would work in the real world. The load system for the simulations consists of two parts, one is a linear load with high power factor representing general electric consumption, and the other, a non-linear load operating as a constant power consumer with low power factor. The non-linear load could represent possible power converters regulated to optimal power based on the available voltage, and will always draw constant P and Q. Examples of this are the commonly used 12-pulse thyristor converters at CERN. Harmonics of the non-linear load are not represented, as these would be suppressed with harmonic filters in real applications, and so the inverter is the only source of harmonics in the load network for simulation.

The control system is build up of the control loops presented in chapter 3. The overview of the control system for both inverter and rectifier is seen in figure 5.1, with the actual simulation model shown in appendix D.2.
Figure 5.1: Detailed control system model - Overview. Simulation model of the entire control system used for the BTB MMC study. Exact systems are presented in appendix D.2.

5.2 Converter Start-up and Operation

Establishing the start-up and steady state operation of the converter is a crucial aspect of the feasibility of the converter. The start-up charging current is controlled by inserting the charging resistors, as shown 5.3, which gives the converter an initial energy. The controllers and breakers can systematically be operated, and the converter can safely charge up the submodule capacitors and reach steady state in about 1 second, in the simulation model. Table 5.1 shows the necessary steps during the start-up of the converter. As the converter has obtained an initial charge of 0.4 p.u of energy in each rectifier and inverter, it is safe to bypass the start-up resistors and let the converter regulate to steady state operation. In the simulation, these resistors are 17 ohm each, rated for nominal current and the grid phase voltage. The steady state of the converter is set to 1 p.u for the DC voltage, and 1.035 p.u for the inverter AC output, as to account for the voltage drop across transformer T2. The energy is also charged up to nominal value of 1 p.u, calculated from the capacitor energy equation, as seen in figure 5.2.
Figure 5.2: Converter start-up and energising simulation - (a) is the output power from the inverter to load, (b) is the power drawn from the grid to feed rectifier, (c) is the DC link power, showing the interaction of the two converters. (d) is the controlled DC bus voltage, (e) is the instantaneous energy stored in the submodules of the inverter and rectifier, and (f) is the controlled AC voltage at inverter output.
Table 5.1: Converter start-up process in simulation.

<table>
<thead>
<tr>
<th>Time:</th>
<th>Event:</th>
</tr>
</thead>
<tbody>
<tr>
<td>t = 0.0 s</td>
<td>Energising of transformer T1</td>
</tr>
<tr>
<td>t = 0.1 s</td>
<td>Start energising of converter with start-up resistor</td>
</tr>
<tr>
<td>t = 0.4 s</td>
<td>Bypass start-up resistors, enable DC regulator</td>
</tr>
<tr>
<td>t = 0.5 s</td>
<td>Enable AC regulator</td>
</tr>
<tr>
<td>t = 0.6 s</td>
<td>Switch on linear load</td>
</tr>
<tr>
<td>t = 0.7 s</td>
<td>Switch on non-linear load</td>
</tr>
<tr>
<td>t = 1.0 s</td>
<td>Steady state reached</td>
</tr>
</tbody>
</table>

![Diagram of converter start-up process](image)

Figure 5.3: Start-up resistors for charging of the converter.

5.2.1 Steady State Operation

The steady state parameters not shown in the start-up process will be displayed in this part. After reaching steady state operation at time equal 1 second, figure 5.4 shows the submodule voltages and currents. Figure (a) and (c) displays the rectifier and inverter submodule voltage in per unit, where the base is set as the DC voltage divided by 'N', the amount of submodules, which is 2.7 kV. Figure (b) and (d) shows the arm current flowing in one phase of each the rectifier and inverter. Here the base of the current is the nominal AC current, which is 1.924 kA.

The steady state submodule operation verifies what was calculated in chapter 4. The submodules have an voltage ripple of approximately 11%, and the voltage is composed of an AC quantity as well as a DC quantity. As capacitors can handle this voltage very well (industrial standard is 24kV), this operation is verified. For the IGBT’s, the 4.5 kV module was selected and derated to 2.7 kV. From the figures, the IGBT can handle this submodule voltage well given the derating, as it operates with 2.7kV DC and a ripple of 11% AC.
Figure 5.4: Steady state operation of the submodule voltage and current.

5.2.2 Controller Responses

To verify the main control objectives of the overall control systems for the rectifier and inverter, the step response is shown in figure 5.5. A step response of -0.1 p.u is applied at time 1 seconds for the DC voltage controller, and the measured DC voltage can be seen to regulate in 0.2s to steady state. This response is dependent on the time it takes to discharge the submodule capacitors, and not the speed of the control system. In figure (b) a step of 0.1 p.u from 1.035 p.u is applied at time 1 seconds, and the d-component of the output inverter voltage is observed to regulate quickly. The response starts within 1 millisecond, and the inverter voltage reaches steady state after approximately 50 ms.
5.3 Voltage Dip Mitigation Feasibility

The main feature and application of the back-to-back HVDC converter is to mitigate the voltage dips occurring in the outside 400 kV grid. The voltage dips are modelled through the 400 kV main source of the model, which can be controlled to supply reduced voltage amplitude in any phase for a short duration. There are two types of dips to be discussed in this chapter. The first type are symmetrical dips which have equal magnitude in all phases. The second type is asymmetrical dips with different amplitudes in each phase, which is more challenging for the control system. Figure 5.6 shows the simulated voltage dips as line-line voltages, to be applied for the model. These are purely reduced source voltages, without any short circuit currents flowing in the system. Figure 5.7 shows the effect of a three-phase -50% voltage dip over 75 ms for a linear load, which through Ohm’s law concludes that the total delivered/consumed power will be approximately 0.25 per unit. Unlike this case, CERN consists of both linear and non-linear loads, where the non-linear ones will try to draw increased current to keep the power constant. With such severe voltage dips, it is not possible to satisfy the power demand with an increased current, and the effect will look similar to the worst case, with just linear loads.
Figure 5.6: Ideal voltage dips simulated in Simulink - Figure (a) and (b) shows a three-phase dip of -50% magnitude and duration of 75 ms, while (c) and (d) shows a one phase dip in phase A of -50% magnitude and duration of 75 ms, while phase B and C are healthy. Line-line voltages are used.

Figure 5.7: Consequence of voltage dip without a mitigation system. A three-phase dip of magnitude -50% and duration of 75 ms is applied to a linear load.

5.3.1 Three-Phase Dip Mitigation

The three-phase dip of equal magnitude is considered a balanced voltage dip, and is the case to be simulated in this sub-chapter. When the simulation-time equals 1.4 seconds, a three-phase balanced voltage dip as shown in figure 5.6 is applied to the simulation model. The result of this simulation is seen in figure 5.8. In this figure the applied voltage dip at rectifier side is observed in (a), and the main objective to keep constant power to load is achieved in (b). While the dip is present, the drawn power from the grid is reduced to 0.5 p.u as seen in (c), while the internal energy of the converters is discharged to the load to keep the delivered power to load at exactly 0.955 p.u. The DC bus power in (d)
is seen oscillating caused by the energy interaction between the rectifier to inverter after the dip is cleared. The fact that the DC power peak reaches 1.45 p.u is not harmful, since the DC current flowing is split equally between the three converter arms of both inverter and rectifier. This results in an overcurrent of around 25% that lasts for one half-cycle, which the IGBT handles well. In (e) and (f) the energy dimensioning can be observed to be properly dimensioned for the worst case of voltage dip, which is the simulation case. As explained earlier in chapter 4.1 when calculating the energy storage, the minimum allowed DC voltage is 0.8 p.u, otherwise the inverter will reach over-modulation. At this DC voltage, the internal energy storage should have supplied 34% of its installed energy, which can be seen in (f) as the energy is discharged to approximately 0.66 p.u. The objective for the inverter to create and maintain the AC voltage at nominal value is further verified in figure 5.9, showing excellent waveform, of which the harmonics are investigated at a later stage.

Figure 5.10 shows the grid and inverter side voltages and currents transformed to dq0 quantities, which is the same reference frame used for signals in the control system. In (a), the voltage dip at grid side is seen as the three-phase -50% magnitude, of 75 ms duration. The maximum allowed current, controlled by both rectifier and inverter is set to 1.05 p.u. This limit is seen in (b) as once the dip is present, the converter operated with 1.05 p.u current drawn for grid. In (c) the modulation index of the rectifier is seen adapting to the voltage dip, to assure that a nominal current is drawn from the grid so that the converter rating is utilised effectively. In (d) and (e) the result of the inverter output is displayed in dq0 quantities. The d-component of the output inverter voltage is 1.035 p.u which is the reference of the control system, this to account for the voltage drop across transformer T2, so that the load has 1 p.u voltage. The current in (e) is showcased to being constant, and has a q-component equal to the reactive power demand of the load and leakage inductance of T2, -0.285 p.u. The modulating index of the inverter shown in (f) is seen approaching over-modulation in positive peak and is already somewhat in over-modulation in the negative peak. This is caused by the circulating current suppression, but the converter dynamics allows a slight over-modulation without harmonic distortion having significant consequences on the output voltages and currents.

Results are concluded for the three-phase dip of -50% magnitude and 75 ms, which after the statistical dip analysis is considered the worst dip to be mitigated, to be satisfactory. The load sees no effect of the voltage dip happening, while the converter can operate under rated conditions, except for the spike in arm current (result of DC power oscillation) which lasts for one period and magnitude of 1.5 times the nominal arm current.
Figure 5.8: Three-phase voltage dip - Voltage, power and energy dynamics. A three-phase dip of -50% magnitude and duration of 75 ms is applied. Figure (a) shows the overlaying grid voltage, (b) and (c) shows the active and reactive power of respectively the rectifier and inverter. (d) shows the power transferred in the DC bus, resulting from the rectifier and inverter interaction, (e) is the DC bus voltage during the dip and (f) shows the instantaneous energy stored in rectifier and inverter and how it discharges to supply the missing power.
Figure 5.9: Three-phase voltage dip - Inverter output AC voltage.

Figure 5.10: Three-phase voltage dip - dq0 measurements and modulating index. A three-phase dip of -50% magnitude and duration of 75 ms is applied. Figure (a) and (b) shows the measured and transformed dq0 voltages and currents at the AC grid connection on the rectifier side, while (c) shows the applied modulation signal from the control system to control the rectifier. (d) and (e) is the transformed dq0 measurements for the load side, at the output of the inverter, while (f) is the applied modulation signal to control the inverter.
5.3.2 Single-Phase Dip Mitigation

A single-phase voltage dip is an asymmetrical condition. This condition can prove to be challenging to control, and an asymmetrical condition in the dq0-plane will create an oscillation in a signal that otherwise should be constant. In power theory with positive, negative and zero sequences, once an asymmetrical condition is present, a negative sequence will appear. Using normal synchronous reference frame (SRF) control system, this will introduce an oscillation as the dq0 plane does not separate the sequences. Having the dual sequence reference frame (DSRF) control can be beneficial as the negative sequence is detected separately during these asymmetrical conditions. Nonetheless, it is proven possible to use the normal SRF control system during asymmetrical conditions, and as such, it is used for this simulation of dip mitigation.

Figure 5.11 shows the grid voltage, the power dynamics of the rectifier and inverter, the DC bus power and voltage, and the instantaneous energy in the converter. Figure 5.13 displays the dq0 voltage and current for both rectifier and inverter, and their respective modulating index signals. The noticeable difference in this simulation, compared to the previous three-phase one, is that the energy demand is not stressed to its maximum. The severity of the dip is only one third of the previous voltage dip, as only phase A is affected with the -50% magnitude for 75 ms. We see on the inverter side in figure 5.11(b) that the power delivered to the load is still constant, and in (f) that stored energy in the converter is used to compensate the missing energy drawn from the AC grid. Figure 5.13 (d) and (e) show that there is no negative or zero sequence present, which confirms that the load network is healthy and balanced despite having unbalanced voltage at the rectifier side, as seen in figure (a) as oscillation in both d and q component. The purpose of the inverter to create and maintain the AC voltage at nominal value is confirmed in figure 5.12, even when asymmetrical conditions are present on the grid side.

Results of the single-phase voltage dip are thus satisfactory and prove the feasibility to keep the load network balanced with constant power flow even during asymmetrical conditions in the overlaying AC grid.
Figure 5.11: Single-phase voltage dip - Voltage, power and energy dynamics. A single-phase dip of -50% magnitude in phase A, and duration of 75 ms is applied. Figure (a) shows the overlaying grid voltage, (b) and (c) shows the active and reactive power of respectively the rectifier and inverter. (d) shows the power transferred in the DC bus, resulting from the rectifier and inverter interaction, (e) is the DC bus voltage during the dip and (f) shows the instantaneous energy stored in rectifier and inverter and how it discharges to supply the missing power.
Figure 5.12: Three-phase voltage dip - Inverter output AC voltage.

Figure 5.13: Single-phase voltage dip - dq0 measurements and modulating index. A single-phase dip of -50% magnitude in phase A, and duration of 75 ms is applied. Figure (a) and (b) shows the measured and transformed dq0 voltages and currents at the AC grid connection on the rectifier side, while (c) shows the applied modulation signal from the control system to control the rectifier. (d) and (e) is the transformed dq0 measurements for the load side, at the output of the inverter, while (f) is the applied modulation signal to control the inverter.


5.4 Power Quality Feasibility

5.4.1 Total Harmonic Distortion

Power converters are known to produce harmonics during operation. Harmonics in power systems are defined as AC signals with higher frequency, superimposed on the fundamental signal. Harmonics cause issues with the overall power quality of the grid, and sensitive equipment can be compromised. The sum of harmonic content in a grid is called Total Harmonic Distortion (THD), which is calculated using equation 43.

\[
THD = \sqrt{\frac{V_2^2 + V_3^2 + \ldots + V_n^2}{V_1}}
\]

(43)

The simulation environment MATLAB & SIMULINK with simpower have a tool called fast fourier transform (FFT) analysis, that computes each individual harmonic component as well as the THD of any signal and displays the results graphically. This tool is used to compute the harmonic distortion caused by the converter systems on both load side and grid side. The harmonic content generated by the converter is as previously discussed in theory, a factor of the switching frequency and modulation strategy. Converters of many levels employ the nearest level modulation to reduce switching losses, instead of using carrier-based modulation strategy for even lower THD. When employing nearest level modulation (NLM), it is possible to let one submodule be PWM modulated, to improve the THD of the system. The modulation strategy for the simulation model is carrier based (phase-shifted PWM (PS-PWM)) at fundamental frequency, which approximates the NLM strategy with one module acting as PWM controlled, switching at higher frequency to reduce THD. Two cases for THD performance is simulated, one at the NLM strategy of a carrier with 50Hz, and another with the carrier frequency at 1350Hz, to compare results, which is efficiency of the converter versus THD produced.

Table 5.2: Total harmonic distortion simulation results - recorded in steady state operation at time equal 1.8 seconds, and of phase A.

<table>
<thead>
<tr>
<th>Signal</th>
<th>NLM (50 Hz)</th>
<th>Carrier (450 Hz)</th>
<th>Carrier (1350 Hz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Inverter voltage:</td>
<td>0.68%</td>
<td>0.57%</td>
<td>0.53%</td>
</tr>
<tr>
<td>Inverter current:</td>
<td>0.20%</td>
<td>0.13%</td>
<td>0.06%</td>
</tr>
<tr>
<td>Grid voltage:</td>
<td>0.99%</td>
<td>0.73%</td>
<td>0.62%</td>
</tr>
<tr>
<td>Grid current:</td>
<td>0.64%</td>
<td>0.39%</td>
<td>0.19%</td>
</tr>
</tbody>
</table>

The results from the simulations shows clearly that the nearest level modulation have the highest THD out of the three cases, but as previously mentioned, it is the most efficient strategy available. The other methods with higher frequency carriers improve the harmonic performance but sacrifices efficiency as all switches turn on and off several times.
times during a period. The grid-code for a connection voltage of 69kV or lower sets a strict allowed THD of no more than 5% for both voltage and current, and requires that no single harmonic component is of 3% or greater. With this in mind, having 0.68% THD from the inverter and 0.99% THD at connection of rectifier, no filters will be needed as the system complies with the grid requirement.

A closer look at the FFT analysis can be seen in figure 5.14, where the harmonic spectrum is displayed graphically and each individual harmonic component is presented relative to the fundamental magnitude. The lower harmonic components up to the 13th are seen as negligible, while the most dominant components (over 0.1% of fundamental) being the 15th, 21th, 25th, 27th, 31th and the 39th. If increased harmonic performance is needed for the system, implementing high frequency (HF) filters for the 15th harmonic is recommended.

Figure 5.14: Harmonics in inverter output voltage with nearest level modulation - Using FFT analysis from SIMULINK.
5.4.2 Reactive Power Support

Supplying the load with reactive power is a necessary function for the inverter. Naturally it will produce all reactive power demanded by the load, and the inverter must be rated for the maximum apparent power. To reduce this necessary rating, one can utilise the fact that the inverter can provide both positive and negative reactive power. In most cases of industrial loads, there will be an inductive reactive power consumed (positive reactive power). By installing AC capacitor banks or high frequency filter to improve harmonics, negative reactive power can be supplied from passive components. Even if the inverter can supply positive reactive power, there might never be a need as most loads are inductive. The passive elements can be switched with breakers to control the bulk reactive power supply, while the inverter will adapt to satisfy the load. By having capacitor banks of for example -50 MVAr installed, the inverter can supply ±50 MVAr, so the total circuit can supply between 0 and -100 MVAr. This means that when the load is consuming 50 MVAr, the inverter is supplying no reactive power, and is operating at maximum efficiency.

\[
Q_{\text{load}} = Q_{\text{inverter}} + Q_{\text{passive}}
\]  

\[
S_{\text{inverter}} = \sqrt{P_{\text{nominal}}^2 + Q_{\text{inverter}}^2}
\]

Figure 5.15: Enhanced reactive power support for load network. Using passive components to optimise reactive power capability of inverter with reduced apparent rating.

A simulation is made focused only on the reactive power support of the inverter. The load demand is presented in table 5.3, which is used for the simulation. A static AC capacitor bank represented by a capacitive load of -50 MVAr inserted in the load network, as shown by figure 5.15. The converter starts in steady state at time equal 1 second. The result of the simulation is seen in figure 5.16.

For the simulation, the load network consumes 210 MW of active power at all times, while its reactive power demand changes. Base power value is set to 220 MVA, as previously.
The leakage inductance of transformer T2 between inverter and load is reduced by a factor of 50, to simplify the results by reducing its reactive power demand. At steady state (t=1.0 second), the capacitor banks is seen to provide all necessary reactive power, and the inverter provides zero reactive power. At time equal 1.3 second, the demand of the load exceeds what the static capacitors supplies, and the inverter supplies the rest. At time equal 1.8 second, the load demands zero reactive power, so to balance the network, the inverter must consume the reactive power produced by the capacitors. Throughout these results, reactive power consumed by the rectifier is zero, so all reactive power is produced locally.

Table 5.3: Reactive power support - Load demand in simulation.

<table>
<thead>
<tr>
<th>Time:</th>
<th>Reactive power consumed by load:</th>
</tr>
</thead>
<tbody>
<tr>
<td>t = 1.0 second</td>
<td>50 MVAr (0.227 p.u)</td>
</tr>
<tr>
<td>t = 1.2 second</td>
<td>100 MVAr (0.454 p.u)</td>
</tr>
<tr>
<td>t = 1.6 second</td>
<td>0 MVAr (0 p.u)</td>
</tr>
</tbody>
</table>

Figure 5.16: Reactive power support from inverter - simulation. (a) Shows the reactive power supplied by inverter, (b) is the reactive power from static AC capacitors. (c) Shows the reactive power consumed by the load network, and (d) is the apparent power supplied by the inverter.
5.4.3 Circulating Current Suppression

The circulating current suppression control described in chapter 3.2.4 is simulated in the developed model. It is crucial to have the CCSC employed as it reduces stress on the components caused by the double fundamental current flowing between the converter arms. Figure 5.17 shows the simulation of this control system. At time equal 1.4 seconds, the CCSC is enabled and the effects are seen immediately. The effects of this control are that the submodule voltage ripple is slightly reduced, the arm current has a better current quality with lower harmonics, and the circulating currents in both rectifier and inverter are reduced. For example in the rectifier, the original circulating current is around 0.07 p.u, which is reduced to 0.02 p.u with the controller. The negative effects of employing this suppression control is that a ripple in the DC voltage appears. The ripple magnitude is a consequence of how much of the circulating current is suppressed by the controls, and a design trade-off needs to be made. In figure (h), the DC voltage is extensively zoomed in upon, and the ripple is seen as 0.02 p.u peak-to-peak. This small ripple creates no outside effects on the AC voltage generated by the inverter, and is of no concern.
Figure 5.17: Circulating current suppression controller (CCSC) function is proven - in (d) the controller is turned on at time = 1.4 seconds. Figure (a) and (e) shows the submodule voltage of each converter in the aggregated model. (b) and (f) shows the arm current in phase A of each converter. Figure (c) and (d) shows the AC component of the circulating current of the two converters, and (h) shows the effect of CCSC on the DC bus voltage.
Chapter 6

Techno-Economical Studies

6.1 Reliability Analysis

The reliability of the modular multilevel converter is one of its great features. Being able to assure operation even if a submodule fails, by enabling a spare module that is already connected and charged to take over the operation of the failed submodule, is a powerful tool. Given the converter designed in earlier chapters, with 51 levels of operation, exactly how many redundant submodules should be installed? This is an important question which is answered with a "Fault Tree analysis" (FTA) together with statistical calculations. Works which has carried out a reliability analysis related to the submodule in MMC is presented in [41], [42].

This analysis is based on several factors that will affect the number of needed submodules. Firstly, the FTA must be completed to reveal the most critical components in case of failure. Secondly, the failure rate data must be obtained for these critical components, which is the first parameter. The second parameter is the expected maintenance schedule, where the converter will be put out of operation so that failed submodules can be replaced by new ones. The maintenance schedule could be several times a year, to annual, biannual or every third year, for example. This fits very well with the overall maintenance schedule of the LHC and long shutdowns, where a major maintenance could be performed every third year or so. The system would require annual maintenance as well, but to include intervention in the converter itself might be needed more seldom.

Fault Tree Analysis

The objective of any FTA is to establish which components are the most critical, leading to the total failure of the analysed system, which in this case is defined as the failure of
the entire submodule. There are many components in the submodule, and some are more prone to failure than others. For example, the bypass thyristor and load switch, which are only used once special circumstances are present, might have a notable failure-rate, but the very low operation time eliminates this from consideration as critical component. Factors that will affect several submodules at the same time are not considered, such as an overall control system failure, signalling failure, or cooling failures etc.

Figure 6.1 shows the FTA with what is defined as the critical components that leads to a submodule failure. If either of the two IGBT switching devices fails, the submodule would enter a state of open circuit, not letting current pass. If a gate driver fails, the switches will be permanently in one state, causing overall failure. If one capacitor fails in such a way that it is an open circuit, then the other capacitor will not be able to handle the entire arm current. If one capacitor fails to closed state, the other capacitor is short-circuited. Lastly, if the individual voltage sensor fails, the balancing algorithm will not be able to function properly for this submodule, causing undervoltage or overvoltage, essentially failing the submodule. All components are thus concluded to be independent of each other in causing a total failure of the submodule.

Failure Rate Data

The failure rate data for typical power electronic components are specified in the unit Failure in Time (FIT), which defines how many failures are expected in 1 billion hours of operation. These values are often from testing the components with accelerated ageing, or with many components simultaneously. Failure data for the capacitor is gathered from [34], while IGBT data comes from a confidential manufacturer as a general rate of 100
FIT. The failure rate of the IGBT gate driver is assumed 150FIT, as presented in [43], while the voltage sensor is estimated to 50 FIT.

Table 6.1: Failure rate for the critical components in the submodule.

<table>
<thead>
<tr>
<th>Component</th>
<th># amount</th>
<th>FIT:</th>
</tr>
</thead>
<tbody>
<tr>
<td>IGBT</td>
<td>2</td>
<td>100 x 2</td>
</tr>
<tr>
<td>Capacitor</td>
<td>2</td>
<td>100 x 2</td>
</tr>
<tr>
<td>Voltage sensor</td>
<td>1</td>
<td>50</td>
</tr>
<tr>
<td>Gate driver</td>
<td>2</td>
<td>150 x 2</td>
</tr>
<tr>
<td><strong>∑</strong></td>
<td><strong>-</strong></td>
<td><strong>750</strong></td>
</tr>
</tbody>
</table>

With table 6.1 presenting each individual components FIT data, and knowing that all critical component failures are independently causing total failure of the submodule, the total FIT data for the submodule is the sum of all individual failure data. Knowing that there are two IGBTs, two capacitors, and two gate drivers, the total FIT is equal to 750 FIT with equation 46.

$$\lambda_{tot} = \sum_{i=1}^{n} \lambda_i = \sum_{i=1}^{n} X_{FIT_i}/10^9 \text{hours}$$

(46)

Failure rate Calculation

Before starting calculations, some assumptions must be made. When defining operational hours, the converter and every submodule is assumed operating 24 hours of every day, and the failure rate of every component (FIT) is constant through its lifetime (often defined as constant hazard rate). Having the failure rate represented as FIT, defined by 1 billion hours of operation is an abstract measure in relation to the converter operation with a lifetime of 25 years. The FIT can be translated into a more understandable measure called Mean Time to Failure (MTTF).

With a total FIT of 750, equation 47 gives a MTTF of 152.2 years per failure. This means that the average time before failure of one single module, is 152.2 years. Mean time does not give the full picture, as statistics are involved and essentially with a constant probability of failure through its lifetime, mean can be translated to a 50% chance of failing after 152.2 years.

$$MTTF = \frac{1}{\lambda_{tot}} = \frac{10^9}{X_{FIT \_failure}} \cdot \frac{\text{hours}}{\text{years}} = 114.15 \cdot 10^3 \cdot \frac{\text{years}}{\text{failure}}$$

(47)

Going into more statistical calculation, it is reasonable to assume that the probability of failure follows the exponential distribution, which by definition explains it so that
the more time passes, the more likely it is that the components will fail. This assumes that the burn-in time, or otherwise called "infant mortality", of the system has elapsed. The variable \( F(t) \) shown in equation (49) is the confidence band used in the statistical calculations, which translates to quality and precision of the calculations.

The exponential distribution functions is defined as:

\[
f(t) = \lambda \cdot e^{-t \cdot \lambda}
\]

\[
F(t) = 1 - e^{-t \cdot \lambda} = 1 - e^{-t \cdot \text{MTTF}^{-1}}
\]

Table 6.2 sums up the conclusion for reliability through redundant submodules. With 50 submodules of every arm, multiplied with the results for \( F(t) \), the calculated redundant modules are rounded upwards. A safety margin should be applied to further increase reliability in case of sudden operation outside operating conditions for some modules. For a three-year maintenance schedule of the converter, two modules are expected to fail in every arm between each maintenance. Adding a margin to this, the converter should operate with 4 extra modules for increased redundancy for the three-year maintenance, adding up to 54 modules per converter arm.

Table 6.2: Failure rate calculation results based on maintenance period.

<table>
<thead>
<tr>
<th>Maintenance (t):</th>
<th>Expected failures ([F(t)]):</th>
<th>Number of modules:</th>
<th>Added margin:</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 year</td>
<td>0.65%</td>
<td>0.325</td>
<td>2</td>
</tr>
<tr>
<td>2 year</td>
<td>1.31%</td>
<td>0.655</td>
<td>3</td>
</tr>
<tr>
<td>3 year</td>
<td>1.95%</td>
<td>0.975</td>
<td>4</td>
</tr>
<tr>
<td>5 year</td>
<td>3.23%</td>
<td>1.615</td>
<td>5</td>
</tr>
<tr>
<td>10 year</td>
<td>6.36%</td>
<td>3.180</td>
<td>8</td>
</tr>
<tr>
<td>25 year</td>
<td>15.15%</td>
<td>7.575</td>
<td>16</td>
</tr>
</tbody>
</table>

6.2 Footprint Estimation

The footprint analysis in this chapter is defined as the physical space requirements of the proposed converter system in the case study. The reference project "Mackinac back-to-back HVDC" can be used to develop a footprint estimation. This project has 200 MVA power rating and has AC connections of 138 kV. This means that compared to the thesis project, this reference project has approximately the same amount of power electronics, but a larger switch-yard because of the higher AC voltages and harmonic filters used for the converter. Using the satellite map tool Google Maps, the footprint of the project is approximately measured.

The Mackinac station employs an area of 4900 \( m^2 \), whereas 600 \( m^2 \) is the converter hall.
building, and an additional 1500 m² is outdoor components directly related to the HVDC operation, which is the wall-bushings, 138/66 kV converter transformer, harmonic filters, separators, circuit breakers and cooling. The rest of the area, 2800 m², is used for utility AC components for the transmission grid, which is not of interest. Height of the converter building is not known but estimated to 8 meters, and there is no information if a cellar exist. The size of interest of the Mackinac back-to-back converter is 2100 m², as shown in appendix F as a visual analysis. For a 220 MVA version with 66 kV connection and no filters, where transformers are already installed, the footprint is optimised to a lower value. A generous estimation could be done, resulting in a footprint of 2500 m², or a equivalent plot of 50x50 meters.

The process of estimating the footprint of the system can be done in the following steps:

1. Gather the physical properties and size of the individual components.

2. Estimate the size of the individual submodule to be used in the rectifier and inverter.

3. Evaluate configurations to build the converter arms with several modules (physical mounting racks) and calculate a footprint of the modular racks acting as building blocks.

4. Overall footprint of the converter valves can be calculated based on the number of modules and racks needed. Thus, the control room, cooling system and other miscellaneous space needed can be estimated roughly, and the footprint of the valve hall is finished.

5. The AC switch-yard with reactors, breakers, separators and bypass system can be estimated with a margin, possibly as twice the size of the valve hall.

A submodule consists of several components, and most noticeably in a physical perspective, the capacitors. For a typical submodule with 20 kJ of energy, the capacitor normally takes over 60% of the volume. The developed submodule in this thesis has two capacitors of 20 kJ each, which will account for over 75% of the volume of each submodule. Based on the Electronicon E59 dry DC capacitors presented in previous chapters, the overall volume can be calculated for the individual submodule. The capacitor in mind is measured to 175x880x520 mm (length,depth,height) and weights approximately 90-100 kg. Mounting two of these side by side, the total dimension for two capacitors is 350x880x520 mm. Depending if a cooling plate is in between, or an air-gap, as the capacitors produce heat, the total dimension can be rounded to 450x880x520 to allow for flow of air. Constructing a casing for the power electronics of the converter, assuming it will account for 25% of the total volume, makes the dimension of 450x220x520 mm, fitting on the connection terminals of the capacitors. A total dimension for one submodule is then 450x(220+880)x520 mm, 450x1100x520 mm, with a volume of 0.2574 m³.
Having the dimension for a proposed submodule, the converter valve can be constructed based on optimal placement. The height of the converter is the largest factor in total area needed, and as one submodule will weigh slightly above 200kg, building the converter tall might be unwise for bearing strength, and ease of maintenance and construction. A limit of 3 meters height is imposed for a proposed design. Assuming all submodules need an air-gap of 40cm in height, and a initial height of 50cm, it is possible to stack three submodules in height before 3 meters is reached. Exactly how many submodules should be placed side-by-side before supports have to be placed is depending on the strength of the mechanical properties. A proposed layout is having 3 modules in height, and four side by side, creating a rack of 12 modules as 3x4. Assuming an air gap of 20cm on the side of each submodule, a rack will span 1.86 meters. Including the metal supports themselves, a final dimension of 2100x1100x2860mm is proposed, having supports of 12cm on each side. The needed floor-space for such a rack is then 2.1m x 1.1m, or 2.31 $m^2$. The proposed converter rack with all dimensions is presented in appendix F, figure 2.

Five racks are needed for each converter arm which there are twelve of. In total, 60 racks are needed, requiring a total area of 140 $m^2$. The converter will need space between racks and converter arms/phases, as well as for the DC bus bars to respect insulation distances in air. Quadrupling the area of all the converter racks gives a good estimate of 560 $m^2$, while respecting required air-distances. Some space of the building must also be reserved for the control room, cooling plant, auxiliary systems as well as general infrastructure. A total size of such a building can then be estimated to 1000 $m^2$. Considering that the Mackinac project has a hall of 600 $m^2$, without further information about height or if a cellar is used, then 1000 $m^2$ is reasonable to assume for the thesis project.

In conclusion, for the footprint of a 220 MVA back-to-back MMC converter where no filters are needed, and transformers already placed, a converter hall of 25x40 meters (or equivalent) should suffice. An outer area of 1500 $m^2$ would be enough for bushings, bus-bars, separators, circuit breakers and measurement transformers. This totals to 2500 $m^2$, or the equivalent of a 50x50 meter plot.

### 6.3 Converter Cost Estimation

Estimating the cost of a system with such high complexity is a challenging task. As the general VSC and MMC technologies are rather new, the literature is still inexperienced in this field. There exist some references to literary works investigating the economic aspects of such converters. In [9], an economical estimation of VSC converter costs is presented as 0.102 M EUR per MVA for each converter station rating, with an accuracy of $\pm$ 30%. For the project in this thesis, it means that the total cost for a back-to-back is 0.204 M
EUR per MVA assuming equal rating of rectifier and inverter, resulting in a total of 45 M EUR for a 220 MVA system.

One good example from already realised projects is the Mackinac back-to-back station, introduced in chapter 3.1 as one of the reference projects. The Mackinac station is a 200 MVA system built with VSC technology that had an investment cost of 68 M EUR, presented in [44]. This project gave a cost of 0.34 M EUR per MVA for a back-to-back system, which is somewhat higher than of 0.204 M EUR per MVA. This considered, the Mackinac project includes new transformers and a completely new switch-yard connecting three 138 kV terminals, giving it a higher price tag than what would be considered for this thesis project. Another project from the same source, based on VSC back-to-back converter, is Kriegers Flak, connecting the Danish electrical grid with the central European grid in Germany. This is a converter with 500 MVA rating and a total cost of 125.7 M EUR, giving the per rating cost of: 0.2514 M EUR/MVA.

The defined costs from these previous sources include the AC switch-yard and converter transformers, which can be a big contributor to the overall cost. At the same time, the proposed back-to-back system with more energy storage than normal will have an added cost. An assumption is that the cost of the increased number of capacitors is equal to the cost of the projected converter transformers included in the cost estimates.

With the basis of cost estimation from literature and reference projects, these can be compared to an actual projection of the proposed converter through estimating cost of each individual component. It is done in two steps;

1. Estimation of the individual submodule cost.

2. Estimation of the total converter and system cost.

**Submodule cost:**

The costs of the submodule components are gathered by several methods. The IGBTs, bypass thyristor and gate drivers are from publicly available prices of manufacturers. The capacitor prices are estimated from experience in metallic film dry capacitors and typical price per kilo-joule of energy. Together, these components make up most of the submodule costs. Other factors, which are harder to find information for is estimated within reasonable price ranges. Of this is the cooling plates and tubing, mounting brackets and assembly work, a bypass load switch, the voltage sensor for the capacitors, auxiliary power converter (DC-DC) siphoning power from the capacitor to feed gate drivers, busbars and wiring, integration of auxiliary signals and bus system, and other minuscule costs. These individual costs are presented in table 6.3.
Table 6.3: Estimated costs of the individual submodule.

<table>
<thead>
<tr>
<th>Component type</th>
<th>Name:</th>
<th>Amount:</th>
<th>Cost:</th>
<th>Total cost:</th>
</tr>
</thead>
<tbody>
<tr>
<td>Individual Submodule cost</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>IGBT</td>
<td>Infineon FZ1200R45HL3</td>
<td>2</td>
<td>2000 Euro</td>
<td>4000 Euro</td>
</tr>
<tr>
<td>Bypass thyristor</td>
<td>Generic presspack</td>
<td>1</td>
<td>1500 Euro</td>
<td>1500 Euro</td>
</tr>
<tr>
<td>Bypass load switch</td>
<td>Generic switch</td>
<td>1</td>
<td>400 Euro</td>
<td>400 Euro</td>
</tr>
<tr>
<td>Gate Drivers</td>
<td>For IGBT/Thyristor</td>
<td>3</td>
<td>300 Euro</td>
<td>900 Euro</td>
</tr>
<tr>
<td>Auxiliary power supply (DC-DC)</td>
<td>Driver power: 30 W</td>
<td>1</td>
<td>1000 Euro</td>
<td>1000 Euro</td>
</tr>
<tr>
<td>Capacitor</td>
<td>3kV, 600A, 20kJ / 100kg</td>
<td>2</td>
<td>2500 Euro</td>
<td>5000 Euro</td>
</tr>
<tr>
<td>Voltage sensor</td>
<td>3-4kV sensor</td>
<td>1</td>
<td>600 Euro</td>
<td>600 Euro</td>
</tr>
<tr>
<td>Cooling plates &amp; tubes</td>
<td>For IGBT/capacitors</td>
<td>1</td>
<td>1000 Euro</td>
<td>1000 Euro</td>
</tr>
<tr>
<td>Discharge circuit</td>
<td>Safety mechanism</td>
<td>1</td>
<td>1000 Euro</td>
<td>1000 Euro</td>
</tr>
<tr>
<td>Assembly materials</td>
<td>Cables, brackets, mechanical</td>
<td>1</td>
<td>2500 Euro</td>
<td>2500 Euro</td>
</tr>
<tr>
<td>Assembly cost</td>
<td>Assembly, cabling &amp; mounting</td>
<td>1</td>
<td>2500 Euro</td>
<td>2500 Euro</td>
</tr>
<tr>
<td>SUM</td>
<td>-</td>
<td>-</td>
<td>20400 Euro</td>
<td></td>
</tr>
</tbody>
</table>

System costs:

The system cost comprises several aspects that can be hard to estimate. The total converter valves cost is comprised of all submodules together. For a 51-level converter with 4 redundant modules in every arm, the total amount of submodules in the converter is 660. The cost of the individual submodule was calculated to 20.4 k EUR, which is rounded to 22 k EUR accounting for a margin. This multiplied with the individual submodule cost makes the total converter valve costs. Beyond this, the aspects such as control system design, arm reactors, AC switch-yard design, cooling system for the losses, civil engineering, and general engineering and commissioning must be reviewed.

The AC switch-yard will consist of bus-bars from transformer to valves, separators and circuit breakers, surge arresters, bushings for the converter hall, and voltage/current transformers for measurement. Majority of the cost of this post is 66 kV circuit breakers.
The system must also feature an charging resistor circuit in the AC lines, controlling the current during startup. This is made up of one set of 66 kV circuit breakers rated for nominal current, as well as three resistors sized appropriately to handle the charging current.

Civil engineering of the converter hall could result in approximately 10 M EUR - for a 1000 $m^2$ building, height 6 meters. Another plot of 1500 $m^2$ should be prepared for outdoor AC components and cooling towers. In total this sums up to a plot of 2500 $m^2$ needed, estimated in the footprint calculations. A price for this plot is estimated to 2 M EUR.

Other costs: For a 220 MW system at max rating, a cooling of 2% is needed in the worst case. This is 4.4 MW of heat that needs to dissipate. An estimation for a primary cooling plant is estimated 500.000 EUR per MW, which translates to roughly 2.2 M EUR for the total losses of 4.4 MW. This includes equipment such as cooling towers, heat exchanger pumps and so on to be interfaced with a closed-loop wet cooling with de-mineralised water. The de-mineralised cooling system is estimated to 1 M EUR, which is the piping and loops connected to the converter itself as well as the process of purifying intake water. In addition, water availability and resource cost for the converter is an economic factor not to be forgotten. Water availability (infrastructure) to the hall is estimated to 1 M EUR, as the loops will need replenishing of water, as the heat transfer process includes vaporising of water over time. This is a rough estimate, as the converter can be expected to operate below 4.4 MW losses in total, as well as the fact that dissipation to air is not accounted for.

A bypass thyristor system in parallel to the back-to-back, with control would consist of several press-pack thyristors in each direction of every phase. In addition, this system needs cooling, dedicated control system, utility and a building. Estimated total cost of such a system is estimated at 3 M EUR, based on experience.

Control system with hot-swap functionality would cost several millions to implement in engineering. Estimating 2 M EUR per set of control systems, with materials, implementation and verification, totalling at 8 M EUR if both rectifier and inverter inhibits live hot-swap functionality, in case one system should fail.

Table 6.4 accounts for all system costs, and the result is rounded to 62.5 M EUR with an included margin. The calculation is based on rough estimations, and should be considered with a error of ± 30% as done in the literature.
Table 6.4: Estimated total system cost for the converter station.

<table>
<thead>
<tr>
<th>Component type:</th>
<th>Description:</th>
<th>Amount:</th>
<th>Cost:</th>
<th>Total cost:</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power converter</td>
<td>All submodules</td>
<td>660</td>
<td>22K Euro</td>
<td>14.52M Euro</td>
</tr>
<tr>
<td>Primary Cooling system</td>
<td>4.4MW system</td>
<td>4.4MW</td>
<td>500K Euro/MW</td>
<td>2.2M Euro</td>
</tr>
<tr>
<td>De-mineralized cooling</td>
<td>Cooling loops</td>
<td>1</td>
<td>1M Euro</td>
<td>1M Euro</td>
</tr>
<tr>
<td>Water availability</td>
<td>Intake Water</td>
<td>1</td>
<td>1M Euro</td>
<td>1M Euro</td>
</tr>
<tr>
<td>Control system</td>
<td>For converter</td>
<td>4</td>
<td>2M Euro</td>
<td>8M Euro</td>
</tr>
<tr>
<td>Arm reactors</td>
<td>Air-core, 66 kV, ~2 kA, ~16 mH</td>
<td>12</td>
<td>250K Euro</td>
<td>3M Euro</td>
</tr>
<tr>
<td>Start-up charging</td>
<td>Resistors and CB</td>
<td>1</td>
<td>1M Euro</td>
<td>1M Euro</td>
</tr>
<tr>
<td>AC yard equipment</td>
<td>CBs, separators, fuses, CT/VT</td>
<td>1</td>
<td>3M Euro</td>
<td>3M Euro</td>
</tr>
<tr>
<td>Thyristor AC breaker</td>
<td>AC bypass system</td>
<td>1</td>
<td>3M Euro</td>
<td>3M Euro</td>
</tr>
</tbody>
</table>

\[ \sum \text{SUM: (components)} \] - - 36.72M Euro

Spare parts 10% of comp. costs - - 3.672M Euro

Civil engineering | 1000m² converter hall | 1 | 10M Euro | 10M Euro |
Plot of land | 2500m² available yard | 1 | 2M Euro | 2M Euro |
System design and engineering - 1 | 6M Euro | 6M Euro |
Commissioning and installation cost - 1 | 4M Euro | 4M Euro |

\[ \sum \text{SUM: (total)} \] - - 62.392M Euro
Summarising the different methods of estimating the total cost, it is clear that the estimation conducted in this chapter is comparable to the values presented in literature. The thesis estimation value of 62.5 M EUR is then used for further economic value in the next chapter, and it is presented as the final system cost estimation.

Table 6.5: Summary of cost estimation methods for the back-to-back system.

<table>
<thead>
<tr>
<th>Approach</th>
<th>Price per MVA:</th>
<th>Total Cost:</th>
</tr>
</thead>
<tbody>
<tr>
<td>Literature</td>
<td>0.204 M EUR/MVA</td>
<td>44.88 M EUR</td>
</tr>
<tr>
<td>Mackinac project</td>
<td>0.340 M EUR/MVA</td>
<td>74.80 M EUR</td>
</tr>
<tr>
<td>Kriegers Flak</td>
<td>0.254 M EUR/MVA</td>
<td>55.88 M EUR</td>
</tr>
<tr>
<td>Thesis estimation</td>
<td>0.284 M EUR/MVA</td>
<td>62.5 M EUR</td>
</tr>
</tbody>
</table>

### 6.4 Economic Evaluation

The net-present-value is a useful tool to evaluate if a certain investment is economically beneficial in a long-time perspective. Equation 50 shows the calculation method, where the parameter ‘t’ equals time in years, r is the discount rate, and C is the cost. Typical discount rate often used in such calculations are 3% and 5%. C0 represents the initial investment cost, calculated in chapter 6.3, while Ct is each individual year’s economic result, subtracting the annual costs from the gained revenue. In the case for the power quality conditioning system, the result will be the yearly socioeconomically gain for CERN to increase its availability, minus the yearly maintenance costs and losses of the system. The economic gain for CERN to employ the back-to-back system is presented in appendix C as 6.877 M EUR, which is rounded to 6.850 M EUR for this analysis.

\[
NPV = \sum_{t=1}^{T} \frac{C_t}{(1+r)^t} - C_0
\]

Typically calculated maintenance cost for a HVDC-VSC is a fixed amount of 1% of the investment cost annually [9]. While CERN is having a long shutdown on the Large Hadron Collider, it is keeping its annual budget for system improvements and upkeep to maintain the machine availability for the next physics run. The economic value of the power quality conditioning system will thus be constant, even during long shutdowns, as it improves availability of the invested capital during the time without the LHC operating. This approach is taken instead of dividing the annual budget during shutdowns over to the other years of operation, effectively giving the same result.
A factor that will affect the annual costs are the electrical losses of the system. They are assumed to be 2%, as an added margin from the results presented in [36], which is the worst-case scenario for the power quality conditioning system. During shutdown, losses will be zero as the converter is bypassed by a circuit breaker. The electrical price per MWh is assumed to be 50 Euros in this study, based on typical price for large industrial customers. The LHC is also assumed to be operative approximately two thirds of the year, accounting for the year-end technical stop.

\[
E_{\text{year}} = P_{\text{system}} \cdot T_{\text{on}} = 220 \text{MW} \cdot 66.7\% \cdot 8760 \text{h} = 1.285 \text{TWh} \tag{51}
\]

\[
E_{\text{loss}} = E_{\text{year}} \cdot K_{\text{loss}} = 1.285 \text{TWh} \cdot 2\% = 25.7 \text{GWh} \tag{52}
\]

The annual cost of losses when the machine is in operation is 25700 MWh times 50 Euros, which equals 1.285 million Euros. Typical components used in power electronic systems have a lifetime from 20 to 30 years. For the overall converter system, a lifetime of 20 years is considered as this is new technology for advanced applications, and there will always be new requirements in the future. During the periodic long shutdowns of the LHC, where extensive upgrading and refurbishing is being done, the power-losses of the system will be zero. The sequence assumed for the analysis is that the LHC will go into a long shutdown during year 4, 5, 9, 10, 14 and 18, and last the entire year. The total NPV analysis is presented in table 6.6 using the discount rates of 3%, 5% and 5.73%, with the latter one being the break-even discount rate.

It is seen that the NPV for the 3% case is positive, summing up to 16.81 million Euros. This is 27% of the initial investment cost, meaning it is a good investment if this discount rate is realistically feasible. The second case of 5% is also positive, with a NPV result of 3.92 million Euros. This gives an indication that the investment feasible if the discount rate is considered higher than the 3%. The break-even discount rate is calculated to 5.73%, meaning that the NPV result is zero for the investment, as seen in the table.
Table 6.6: Net Present Value analysis for the proposed system.

<table>
<thead>
<tr>
<th>Year</th>
<th>Revenue:</th>
<th>Cost:</th>
<th>Result:</th>
<th>NPV (r=3%)</th>
<th>NPV (r=5%)</th>
<th>NPV (r=5.73%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>-62.5</td>
<td>0.00</td>
<td>-62.5</td>
<td>-62.5</td>
<td>-62.5</td>
<td>-62.5</td>
</tr>
<tr>
<td>1</td>
<td>6.85</td>
<td>-1.885</td>
<td>4.965</td>
<td>4.80</td>
<td>4.70</td>
<td>4.67</td>
</tr>
<tr>
<td>2</td>
<td>6.85</td>
<td>-1.885</td>
<td>4.965</td>
<td>4.66</td>
<td>4.48</td>
<td>4.42</td>
</tr>
<tr>
<td>3</td>
<td>6.85</td>
<td>-1.885</td>
<td>4.965</td>
<td>4.52</td>
<td>4.27</td>
<td>4.18</td>
</tr>
<tr>
<td>4</td>
<td>6.85</td>
<td>-0.60</td>
<td>6.25</td>
<td>5.53</td>
<td>5.12</td>
<td>4.98</td>
</tr>
<tr>
<td>5</td>
<td>6.85</td>
<td>-0.60</td>
<td>6.25</td>
<td>5.37</td>
<td>4.88</td>
<td>4.71</td>
</tr>
<tr>
<td>6</td>
<td>6.85</td>
<td>-1.885</td>
<td>4.965</td>
<td>4.14</td>
<td>3.69</td>
<td>3.54</td>
</tr>
<tr>
<td>7</td>
<td>6.85</td>
<td>-1.885</td>
<td>4.965</td>
<td>4.02</td>
<td>3.51</td>
<td>3.34</td>
</tr>
<tr>
<td>8</td>
<td>6.85</td>
<td>-1.885</td>
<td>4.965</td>
<td>3.90</td>
<td>3.34</td>
<td>3.16</td>
</tr>
<tr>
<td>9</td>
<td>6.85</td>
<td>-0.60</td>
<td>6.25</td>
<td>4.77</td>
<td>4.01</td>
<td>3.77</td>
</tr>
<tr>
<td>10</td>
<td>6.85</td>
<td>-0.60</td>
<td>6.25</td>
<td>4.63</td>
<td>3.82</td>
<td>3.57</td>
</tr>
<tr>
<td>11</td>
<td>6.85</td>
<td>-1.885</td>
<td>4.965</td>
<td>3.57</td>
<td>2.89</td>
<td>2.68</td>
</tr>
<tr>
<td>12</td>
<td>6.85</td>
<td>-1.885</td>
<td>4.965</td>
<td>3.46</td>
<td>2.75</td>
<td>2.53</td>
</tr>
<tr>
<td>13</td>
<td>6.85</td>
<td>-1.885</td>
<td>4.965</td>
<td>3.36</td>
<td>2.62</td>
<td>2.39</td>
</tr>
<tr>
<td>14</td>
<td>6.85</td>
<td>-0.600</td>
<td>6.25</td>
<td>4.12</td>
<td>3.14</td>
<td>2.85</td>
</tr>
<tr>
<td>15</td>
<td>6.85</td>
<td>-1.885</td>
<td>4.965</td>
<td>3.17</td>
<td>2.38</td>
<td>2.14</td>
</tr>
<tr>
<td>16</td>
<td>6.85</td>
<td>-1.885</td>
<td>4.965</td>
<td>3.08</td>
<td>2.26</td>
<td>2.03</td>
</tr>
<tr>
<td>17</td>
<td>6.85</td>
<td>-1.885</td>
<td>4.965</td>
<td>2.99</td>
<td>2.16</td>
<td>1.92</td>
</tr>
<tr>
<td>18</td>
<td>6.85</td>
<td>-0.60</td>
<td>6.25</td>
<td>3.66</td>
<td>2.59</td>
<td>2.28</td>
</tr>
<tr>
<td>19</td>
<td>6.85</td>
<td>-1.885</td>
<td>4.965</td>
<td>2.82</td>
<td>1.95</td>
<td>1.71</td>
</tr>
<tr>
<td>20</td>
<td>6.85</td>
<td>-1.885</td>
<td>4.965</td>
<td>2.74</td>
<td>1.86</td>
<td>1.62</td>
</tr>
<tr>
<td>Sum:</td>
<td></td>
<td></td>
<td></td>
<td>16.81</td>
<td>3.92</td>
<td>-0.01</td>
</tr>
</tbody>
</table>

The conclusion of the NPV analysis is abstract, and is dependent on the definition of what is a reasonable discount rate to be used by CERN. Since CERN is a large organisation, where funding is received from the member states, a lower discount rate could be feasible for such studies. The 3% discount rate result could be regarded as the annual price index increase (approximately 2%), with global loans for the investment of close to 1% rent. If this assumption is reasonable, then the investment is concluded as very beneficial for CERN.

Many assumptions are included in this economical study. First off, the economic gain is only computed based on lost time, not considering the equipment damage caused by voltage dips and costs of personnel. It is also very hard to document long-term damage caused by voltage dips, which can cause components to fail in the future, and where the root cause is hard to identify. This risk is thus reduced with the mitigation system. Losses of the system are also accounted for in the worst case of the MMC, by assuming 2% where it can be optimised closer to 1.5% or less. It also assumes that the converter is using 220
MW, while in reality it might operate at lower loading as well. The assumed yearly maintenance of 1% of the investment could be considered rather large, and could possibly optimised to 0.5% given that spare parts are already accounted for in the investment cost. The investment cost is also assumed to be 62.5 million Euros, when in the system cost analysis, it is regarded with a margin of ±30%.

Whether the LHC will be in operation for 20 years is a big assumption as well. In the case that a new circular collider is to be built, the LHC may be a part of the injection chain, and the interruption of the LHC will thus affect the newest collider. In the other case where the LHC will be upgraded to a more powerful version, this system will be valid for at least 20 years. For both cases, a life-time expectancy of 20 years is reasonable to assume. Other features of the system such as reactive power compensation is not accounted for in the economical analysis. The social benefits of the project is not accounted for neither, which might be an important factor. By enabling such a project, a fundamental knowledge of modular multilevel converters and design is gained by industry and by CERN, which would become a flagship project of knowledge transfer for this technology.

6.5 Further Applications

Further application of the power quality conditioning system can be categorised in two groups:

- The entire power quality conditioning system as back-to-back HVDC MMC to mitigate voltage dips for networks requiring high precision and power quality.

- The technology behind the PQCS developed in the thesis, such as individual applications of the rectifier and inverter respectively. This includes practical usage of submodules in applications for increased energy storage with enhanced submodules, the control strategies, thyristor bypass system etc.

For the first category, other solutions exist to manage and mitigate voltage dips occurring in the network. These solutions are based on parallel compensation that injects a counter voltage to stabilise the "missing" voltage of the dip. These solutions are the dynamic voltage restorer (DVR), and the static synchronous compensator (STATCOM) with integrated energy storage. The STATCOM is identified as potentially suitable for this purpose but has a response speed of several milliseconds. The DVR response time is under 1 ms, which makes it suitable for high precision applications such as CERN.

The main requirement for using the back-to-back MMC for mitigation of voltage dips and power quality enhancement is the fast response and high precision, however it is very costly compared to the slower STATCOM with energy storage. Applications for such
high precision outside CERN could be factories that require very high precision, such as battery and semiconductor production. Another futuristic possibility is the use of this system to feed fusion plants operating at very high precision to stabilise plasma through very strong magnets. Another application for the back-to-back converter is as an efficient hybrid distribution network, tapping DC power from the bus while also inverting to AC again, exploiting the possibility of integrating energy storage to the DC bus to supply both AC and DC power, or connect DC generation from renewable sources to the AC network, all while ensuring excellent power quality.

For the second category, the possibilities are endless. Modular multilevel converter is a trending topology that sees more and more uses as research and development is continuously advancing. This is everything from motor drives to multi-terminal DC grids and sophisticated rectifiers and inverters. An MMC operating with passive networks is especially beneficial, and applications in maritime industry and off-shore have large potential. The future of DC interconnection grids also relies on powerful and sophisticated converters to allow multi-terminal DC grids, which will see use of modular multilevel converters. Figure 6.2 sums up many possible applications of the future.
Chapter 7

Conclusion and Future Work

7.1 Conclusion

The power quality conditioning system is proven functional and feasible in this thesis, based on the requirements of the project. The modular multilevel converter as the topology for the back-to-back HVDC system provides powerful features and design possibilities. Based on statistical analysis of voltage dips and energy dimensioning, simulation studies have verified the proposed system’s ability to mitigate voltage dips. The result of the statistical analysis is that the energy storage can be optimised based on the desired coverage from voltage dips. An optimum design choice is identified as the 98% coverage of voltage dips, requiring only half of the energy compared to a 100% coverage system. The methods presented in this thesis are not only a proposal, but also a guideline of how any system can be designed in the future, no matter which voltage level, converter rating or other design criteria. The back-to-back system also possesses several powerful features such as reactive power support, steady state regulation, and excellent redundancy and harmonic performance. It is the ultimate power quality conditioning system for any industrial network operating with high precision and requirements in electrical supply. The system is also proven feasible as the concepts of HVDC MMC already are realised in the industry today. For CERN, a 220 MVA system connected to the 66 kV network is proposed with component specifications based on industrial standards and off-the-shelf components. The space requirements of the system are identified as 2500 square meters, based on presented calculations, as well as review of an already existing project.

Economical calculations are performed based on the system proposal, giving an estimate of 62.5 million Euros, with a margin of $\pm 30\%$. The estimated cost is cross-referenced with literature and existing projects today, to validate the dedicated estimations. A net-present value analysis of investing 62.5 million Euros in the proposed system results in
a positive value of 16.81 million Euros for a discount rate of 3%, indicating that it is a strong investment for CERN. Overall, this thesis has shown that the back-to-back HVDC modular multilevel converter can be used to build a very powerful power quality system, mitigating all transient voltage disturbances within its rated design range.

7.2 Future Work

This thesis has covered all subjects and topics defined in the initial thesis project definition, including conceptual design, feasibility study and evaluation of costs and other aspects. Based on this work, future studies could continue this research and development further by investigating the following aspects:

- Study of AC grid stabilisation and reactive power injection to upstream grid with the HVDC MMC. Explore the possibilities of providing support to the transmission network, and discuss the benefit of this for the transmission system operator (TSO).

- Internal submodule fault and detection handling studies. Investigating and simulating internal submodule faults and methods of detection, as well as arm-arm short circuits of the converter (also called flashover fault).

- A study focused on the very detailed submodule design, including in-depth analysis of how to siphon auxiliary power from internal capacitors in the submodules. Investigate efficiency of internal voltage divider across capacitor versus a DC-DC converter to feed gate drivers. Also, see if an alternative source can be used for auxiliary power. A battery system for the auxiliary power could be investigated as a potential solution.

- Look more in detail on the load-side fault scenario. Study of potential solutions, and if differential relays or other solutions not dependent on short circuit current can be used for fault detection and selectivity. If the anti-parallel thyristor switch is the preferred solution, then a detection method of potential faults must be developed. The transition from bypass mode to converter operation, and back, must also be studied.

- More detailed economic studies.
References


Appendix A

dq0-Transformation Theory

Dq0 transformation theory in electrical power engineering is based on mathematical computation to transform AC quantities (rotating signals) into stationary DC quantities. It is a useful tool to analyse three phase systems in the dq0 frame because control systems based on PID controllers can use these DC quantities as references. Transforming AC signals to dq0 is done by rotating the real and imaginary axis with the angular system frequency from the alpha-betta-zero frame, essentially creating a relative rotation speed of zero, and thus in steady state the signals appear as DC.

The transformation matrix to dq0 plane is given by:

\[
\begin{bmatrix}
  u_d \\
  u_q \\
  u_0
\end{bmatrix}
= \frac{2}{3}
\begin{bmatrix}
  \cos(\theta) & \cos(\theta - \frac{2\pi}{3}) & \cos(\theta + \frac{2\pi}{3}) \\
  -\sin(\theta) & -\sin(\theta - \frac{2\pi}{3}) & -\sin(\theta + \frac{2\pi}{3}) \\
  1/2 & 1/2 & 1/2
\end{bmatrix}
\begin{bmatrix}
  u_a \\
  u_b \\
  u_c
\end{bmatrix}
\]

The inverse transform is given by:

\[
\begin{bmatrix}
  u_a \\
  u_b \\
  u_c
\end{bmatrix}
= \begin{bmatrix}
  \sin(\theta) & \cos(\theta - \frac{2\pi}{3}) & 1 \\
  \sin(\theta - \frac{2\pi}{3}) & \cos(\theta + \frac{2\pi}{3}) & 1 \\
  \sin(\theta + \frac{2\pi}{3}) & \cos(\theta + \frac{2\pi}{3}) & 1
\end{bmatrix}
\begin{bmatrix}
  u_d \\
  u_q \\
  u_0
\end{bmatrix}
\]

These two equations are identical for transforming three phase currents to dq0 plane, and back. For power, the following equations represent the active and reactive power with dq0 quantities.

\[
\begin{bmatrix}
p \\
q
\end{bmatrix}
= \begin{bmatrix}
u_di_d + u_qi_q \\
u_qi_d - u_dii_q
\end{bmatrix}
\]

Introducing the transformation theory behind dual synchronous reference frame (DSRF) requires theory of symmetrical components transformation. During balanced conditions
Figure A.1: dq0 transform showcased in stationary abc-frame.

all systems consists of only positive sequence components. Only during unbalanced conditions does DSRF give additional information, as the negative sequence inhibits information on the power exchange between the unbalanced phases. To introduce DSRF control, one must first compute the symmetrical components of the current and voltages. Once the positive and negative components are identified, using the formulas below, then they can be transformed to the dq0 frame separately. What is an important detail is that the negative sequence (v2) is rotating in negative direction, which requires a negative angular frequency in the trigonometric functions presented in the dq0 equations above.

\[
\begin{bmatrix}
 u_a \\
 u_b \\
 u_c
\end{bmatrix} = \begin{bmatrix}
 u_{a0} \\
 u_{b0} \\
 u_{c0}
\end{bmatrix} + \begin{bmatrix}
 u_{a1} \\
 u_{b1} \\
 u_{c1}
\end{bmatrix} + \begin{bmatrix}
 u_{a2} \\
 u_{b2} \\
 u_{c2}
\end{bmatrix}
\]

\[
\begin{bmatrix}
 u_0 \\
 u_1 \\
 u_2
\end{bmatrix} = \frac{1}{3} \begin{bmatrix}
 1 & 1 & 1 \\
 1 & h & h^2 \\
 1 & h^2 & h
\end{bmatrix} \begin{bmatrix}
 u_a \\
 u_b \\
 u_c
\end{bmatrix}
\]

\[h = e^{2\pi i/3}\]
Appendix B

Voltage Dip Measurement Data

Table B.1: Measured voltage dips at CERN from 2011, 2012, 2015, 2016 and middle of 2017, of which have caused the tripping of either LHC, SPS or PS, causing a major event.

<table>
<thead>
<tr>
<th>Year</th>
<th>Voltage Dip</th>
<th>Voltage Dip</th>
<th>Voltage Dip</th>
<th>Voltage Dip</th>
<th>Voltage Dip</th>
</tr>
</thead>
<tbody>
<tr>
<td>2011</td>
<td>30 -13.4%</td>
<td>40 -12.0%</td>
<td>40 -14.0%</td>
<td>40 -14.0%</td>
<td>60 -9.0%</td>
</tr>
<tr>
<td></td>
<td>40 -13.0%</td>
<td>44 -38.4%</td>
<td>50 -34.4%</td>
<td>21 -4.4%</td>
<td>80 -11.0%</td>
</tr>
<tr>
<td></td>
<td>50 -16.0%</td>
<td>60 -9.0%</td>
<td>60 -15.0%</td>
<td>30 -6.4%</td>
<td>80 -20.0%</td>
</tr>
<tr>
<td></td>
<td>50 -6.5%</td>
<td>60 -8.0%</td>
<td>60 -35.0%</td>
<td>30 -4.0%</td>
<td>80 -9.0%</td>
</tr>
<tr>
<td></td>
<td>50 -13.0%</td>
<td>60 -8.0%</td>
<td>60 -10.4%</td>
<td>40 -14.0%</td>
<td>88 -12.0%</td>
</tr>
<tr>
<td></td>
<td>60 -20.0%</td>
<td>60 -8.0%</td>
<td>60 -9.2%</td>
<td>40 -7.3%</td>
<td></td>
</tr>
<tr>
<td></td>
<td>60 -13.0%</td>
<td>60 -23.0%</td>
<td>60 -7.7%</td>
<td>40 -4.0%</td>
<td></td>
</tr>
<tr>
<td></td>
<td>60 -9.0%</td>
<td>60 -22.0%</td>
<td>60 -35.5%</td>
<td>46 -3.0%</td>
<td></td>
</tr>
<tr>
<td></td>
<td>60 -8.9%</td>
<td>70 -10.0%</td>
<td>60 -8.4%</td>
<td>50 -4.5%</td>
<td></td>
</tr>
<tr>
<td></td>
<td>60 -9.0%</td>
<td>70 -30.0%</td>
<td>60 -5.4%</td>
<td>50 -3.7%</td>
<td></td>
</tr>
<tr>
<td></td>
<td>65 -7.0%</td>
<td>70 -9.0%</td>
<td>60 -7.4%</td>
<td>54 -8.3%</td>
<td></td>
</tr>
<tr>
<td></td>
<td>70 -13.0%</td>
<td>75 -17.0%</td>
<td>80 -6.9%</td>
<td>60 -16.1%</td>
<td></td>
</tr>
<tr>
<td></td>
<td>70 -39.0%</td>
<td>75 -23.0%</td>
<td>80 -16.7%</td>
<td>60 -16.0%</td>
<td></td>
</tr>
<tr>
<td></td>
<td>70 -8.7%</td>
<td>75 -7.0%</td>
<td>60 -11.7%</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>70 -13.0%</td>
<td>75 -6.0%</td>
<td>60 -8.0%</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>75 -25.0%</td>
<td>80 -22.0%</td>
<td>70 -10.0%</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>80 -15.0%</td>
<td>80 -13.0%</td>
<td>70 -10.6%</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>80 -10.0%</td>
<td>100 -70.0%</td>
<td>70 -9.5%</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>80 -20.0%</td>
<td>100 -12.0%</td>
<td>70 -26.1%</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>80 -14.0%</td>
<td>220 -13.0%</td>
<td>70 -9.6%</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>80 -11.0%</td>
<td>70 -7.5%</td>
<td>70 -10.1%</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>80 -7.0%</td>
<td>80 -4.0%</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>90 -14.0%</td>
<td>80 -7.2%</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>100 -42.0%</td>
<td>80 -7.3%</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>100 -17.0%</td>
<td>80 -8.7%</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>600 5.0%</td>
<td>80 -9.0%</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>80 -10.4%</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>80 -10.9%</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>80 -11.9%</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>80 -13.0%</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>80 -14.3%</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>80 -16.7%</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>80 -24.0%</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>80 -33.4%</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>80 -39.5%</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>80 -9.4%</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>95 -26.0%</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>100 -12.4%</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>100 -5.9%</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>100 -12.5%</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>120 -11.3%</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>380 -9.2%</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Appendix C

Economical Analysis of LHC Availability

As the LHC is sensitive to voltage perturbations, the overall availability of the system is affected. It is important to know the actual costs related to the shutdowns caused by voltage dips in the grid. This study uses values from the 2016 and 2017 run of the Large Hadron Collider. The analysis is conducted three steps:

1. Establish value of availability for CERN, in per hour of operation
2. Discover the lost production time of the LHC caused by one major event
3. Evaluate the lost economic value with the number of events, the cost of hourly loss and the average production time lost because of this.

From table C.1 the LHC operated with a total physics time of 153 days, and in stable beam mode 49.2% in 2016. The LHC were in stable beam mode for 1839.5 hours total and operation time of 857.9h. As science and data is the product, and CERN only produces science during stable beam mode, it is fair to conclude that all investments goes into operations and having stable beams. The budget of LHC in 2016 were 283.4 M CHF, which is including maintenance and further investment costs for the future. Thus one can say that for 2016, CERN paid $283.4 \text{ M CHF}/(1839.5h+857.9h) = 105 \text{ K CHF/h}$

CERN pays 105,000 Swiss francs for every hour of operation and science production of the LHC throughout the year.

If the LHC dumps the beam, how long on average does it take to regain stable beam conditions? The main parameter for this estimation is the turn-around time, defined as the time it takes from a system dump, until the operators have regained stable beams in the LHC. For 2016 the average turn-around time for the LHC was 7.1 hours, and for 2017 it was 6.2 hours.
How does one define the lost science? First, the critical points where a dump is most and least fatal must be identified. If LHC just reached stable beam conditions, and it dumps, the system essentially loses the whole turn-around time from previous dump. If the LHC dumps the beam because of a perturbation, when it otherwise would dump the beam, it loses no operating time and can return to fill immediately.

Looking at figure C.1 at the three indicated times t1, t2 and t3, we can define the case of lost time if a voltage dip trips the system and causes dump of beam. At t1 the system has ramped up and entered stable beams, after some time to gain beam. If a perturbation happens here, we essentially lose the whole turn-around time as we will have to prepare again before stable beams are achieved. If a perturbation happens at t2, which is the time we would normally dump the beam anyway, we loose no operation time and the consequence are zero. Going from t2 to t3, we are filling and ramping up the energy, this is the preparation time called turn-around time. At the time of the dump, we essentially lose the time used so far in preparation, creating this linear curve for the consequence where peak being the total turn-around time. Assuming a voltage dip has a equally distributed chance of happening, the average time lost is the average of the trigonometric evaluation of the consequences. The average is half of the peak value, and using the 2017 values for average turn-around time as 6.2 hours, the average lost time is 3.1 hours.

Average turnaround time after beam dump: 3.1 hours. 1 perturbation = 3.1h + physical downtime, approx. 3.1 hours. This means that every perturbation that causes the LHC to dump the beam costs CERN 325.5 K CHF.

For 2016: 35 major events from voltage dips, where physical downtime was only 20% of total unavailability. For 2017: 13 major events from voltage dips tripping the LHC, physical downtime is summed to total of 1 hour. Data originated from CERN AFT - Accelerator Fault Tracking database.

2016: Economic gain if 35 perturbations in one year: 35*3.1h*105.000 CHF/h + physical downtime = 11.400.000 CHF + physical downtime, annually

2017: Economic gain if 13 perturbations in one year: 13*3.1h*105.000 CHF/h + physical downtime = 4.231.500 CHF + physical downtime, annually

There is a big difference between 2016 and 2017, as 2016 was a very affected year while 2017 had little events. The average between these years will be used for future calculations, while acknowledging that the data might be less accurate than reality. Physical downtime is not accounted for, as it results in a fraction of the total. Average value used is 7.815.750 CHF from just the lost availability and potential stable beam time of LHC.

Assuming the exchange rate of CHF to Euro is 0.88, the annual economic gain is 6,877,860 Euro.
Figure C.1: LHC beam operation cycle and consequence of beam dump.
Table C.1: Availability data of the LHC for 2016 and 2017.

<table>
<thead>
<tr>
<th>Function</th>
<th>2016 Run</th>
<th>2017 Run</th>
</tr>
</thead>
<tbody>
<tr>
<td>Total operation interval</td>
<td>213 Days</td>
<td>218 Days</td>
</tr>
<tr>
<td>Of which physics</td>
<td>146 days</td>
<td>126 days</td>
</tr>
<tr>
<td>Of which special physics</td>
<td>7 days</td>
<td>3.5 days</td>
</tr>
<tr>
<td>Total Physics time (including ramp)</td>
<td>153 days</td>
<td>140.5 days</td>
</tr>
<tr>
<td>Physics Achieved: ( fb^{-1} )</td>
<td>38.709</td>
<td>51.83</td>
</tr>
<tr>
<td>Availability Avg.</td>
<td>75.89%</td>
<td>82.90%</td>
</tr>
</tbody>
</table>

Filling data:

| Numbers of fills:                             | 762      | 762      |
| Numbers of fills reaching stable beams:       | 175      | 211      |
| Stable beams: End of Fill                     | 47% / 84 | 50% / 106 |
| Stable beams: Aborted                         | 48% / 86 | 45% / 95 |
| Stable beams: Aborted (special)               | 5% / 9   | 5% / 10  |

Stable beam duration data:

| Avg. Stable beam duration: end of fill         | 13.1h    | 10.7h    |
| Longest Stable beam duration: end of fill      | 37h      | 27.4h    |
| Avg. Stable beam duration: aborted             | 7.8h     | 4.6h     |
| Longest Stable beam duration: aborted          | 35.4h    | 15.4h    |

Turnaround Data:

| Avg. Turn around time                         | 7.1h     | 6.2h     |
| Longest turn around time                      | 22.8h    | 30.1h    |
| Shortest turn around time                     | 2.5h     | 2.2h     |
| Number of turnarounds considered              | 157h     | 193h     |

Reference:

Appendix D

MATLAB & SIMULINK Models and Scripts

Include picture/overview of SIMULINK models developed. Controls, overview, loads, parameter scripts, aggregate and physical model. Cap voltage balancing. Parametric PI tuning script, etc.

D.1 Matlab Scripts

Matlab script - system variables

Script for simulation parameters in simulink:

```matlab
%Script for 51-level MMC HVDC Back-To-Back DC Link converter:
clc
%Initial time constants:
Ts_Power =20e-6; %Power System sampling time.
Ts_Control=40e-6; %Control system sampling time.
Fc = 50; %Switching frequency IGBTs

%%Grid Parameters:
f = 50; %grid frequency.
w = 2*pi*f; %angular frequency.
V_prim = 400e3; %Primary dist grid.
V_grid = 66e3; %RMS L–L Voltage of BTB.
Skk = 12000e6; %Max. short circuit power, source.
xr_ratio = 14.28; %X/R ratio of grid.
```
%Base 400kV
17 \[ z_{\text{int}_{\text{400}}} = \sqrt{3} \cdot (V_{\text{prim}})^2 / S_{\text{k}}; \]
18 \[ R_{\text{int}} = \sqrt{\left( z_{\text{int}_{\text{400}}}^2 / (1 + x_{\text{r}} \cdot \text{ratio}^2) \right)}; \]
19 \[ X_{\text{int}} = R_{\text{int}} \cdot x_{\text{r}} \cdot \text{ratio}; \]
20 \[ L_{\text{int}} = X_{\text{int}} / w; \]
21 \[ z_{0z1} = 0.8; \]

%%Load Parameters:
22 \[ P_{\text{nom}} = 220e6; \]
23 \[ S_{\text{nom}} = 220e6; \]
24 \[ I_{\text{nom}} = S_{\text{nom}} / (\sqrt{3} \cdot V_{\text{grid}}); \]
25 \[ P_{\text{load}} = 110e6; \]
26 \[ Q_{\text{load}} = 0e6; \]
27 \[ S_{\text{load}} = \sqrt{P_{\text{load}}^2 + Q_{\text{load}}^2}; \]
28 \[ R_{\text{startup}} = 17; \]
29 \[ P_{\text{DynLoad}} = 100e6; \]
30 \[ Q_{\text{DynLoad}} = 50e6; \]

%%DC Link Parameters:
31 \[ V_{\text{dc nom}} = 135e3; \]

%%Submodule Parameters:
32 \[ n = 50; \]
33 \[ n2 = 50; \]
34 \[ C_{\text{pm}} = 10.48e-3; \]
35 \[ V_{\text{c pm r}} = 0 \cdot V_{\text{dc nom}} / n; \]
36 \[ V_{\text{c pm i}} = 0 \cdot V_{\text{dc nom}} / n2; \]

%%Converter Reactor:
37 \[ Z_{\text{base66}} = \left( \frac{\sqrt{3} \cdot (V_{\text{grid}})^2}{S_{\text{nom}}} \right); \]
38 \[ R_{\text{arm}} = 0.03; \]
39 \[ L_{\text{arm pu}} = 0.15; \]
40 \[ L_{\text{arm}} = L_{\text{arm pu}} + Z_{\text{base66}} / w; \]
41 \[ R_{\text{arm pu}} = R_{\text{arm}} / Z_{\text{base66}}; \]

%%Controller settings:
42 %%Rectifier Parameters:
43 \[ K_{\text{p Ireg r}} = 2; \]
44 \[ K_{\text{i Ireg r}} = 100; \]
45 \[ DC_{\text{lim}} = 1.05; \]
46 \[ K_{\text{p DCreg r}} = 8; \]
47 \[ K_{\text{i DCreg r}} = 150; \]

%%Inverter Parameters:
48 \[ K_{\text{p Ireg i}} = 2; \]
49 \[ K_{\text{i Ireg i}} = 200; \]
Kp_ACreg_i = 2; %Parameter of outer voltage control.
Ki_ACreg_i = 260; %Parameter of outer voltage control.

%% Filters for control signals in dq0;
Fn_filter=1000; %cutoff freq. for 2nd order filter.
Zeta_filter=1; %damping ratio of 2nd order filter.

%%Fault settings: %Enables voltage dip from source
T_fault = 1.4; % that last x milliseconds.

Script for statistical energy calculations:

x = xlsread('Dip_Dataset.xlsx'); %All voltage dip measurements.
y(:,1) = x(:,1)*0.001; %Dip Duration – Scaled to p.u.
y(:,2) = abs(x(:,2))*0.01; %Dip magnitude – scaled to p.u.
z = (y(:,1).*y(:,2)); %Final Dataset.

x1 = 0:.0001:0.08; %X.axis of propability function.
l = fitdist(z, 'Loglogistic'); %Fits dataset to log-logistic.
y1 = pdf(l,x1); %extracts y−coordinates.
i = cumtrapz(.01,y1); %Integration for confidence band.

figure; subplot (2,1,2); plot(x1,y1, 'LineWidth',2,'color', 'r'); title ('Dip Severity Distribution - Log-logistic'); xlabel('f(v,t) - Dip severity (p.u)'); ylabel('Propability function f(x)'); hold; plot (x1,i, 'LineWidth',2, 'color','b'); title ('Probability of dip severity & confidence band - Log-logistic'); xlabel('f(v,t) - Dip severity(p.u)'); ylabel('Probability'); grid; legend('Distribution function', 'Confidence function')

%Fitting LogLogistic dist. to histogram for Verification:
 subplot(2,1,1);
32 h = histfit(z, 30, 'Loglogistic');
33 h(1).FaceColor = [0, 0.4470, 0.7410];
34 h(1).BarWidth = 0.8;
35 h(2).LineWidth = 3;
36 set(gca, 'XLim', [0 0.08])
37 set(gca, 'YLim', [0 35])
38 title('Dip severity histogram & distribution fit');
39 ylabel('# of datapoints');
40 xlabel('f(v,t) - Dip severity (p.u)');
41 legend('Dip severity events', 'Qualitative distribution fit')
42 grid;

Script for iterative PI controller tuning:

1 system1 = 'BackToBack_HVDC_MMC_Aggregate';
2 open_system(system1);
3 %
4 % Testing values for controller:
5 Kp = [0.1 0.5 1 1.5 2 2.5 4 10];
6 Ki = [50 120 150 180 200 260 350 700 1000];
7 %
8 TestNum=0;
9 for x1=1:numel(Kp) %counts up to amount of variable 1.
10    Kp_Ireg_r = Kp(x1); %initializes new value for simulation:
11    Kp_Ireg_i = Kp(x1);
12    for y1=1:numel(Ki) %counts up to amount of variable 2.
13        TestNum = TestNum+1; %counts the amount of simulations done.
14        Ki_Ireg_i = Ki(y1); %initializes new value for simulation:
15        Ki_Ireg_r = Ki(y1);
16        sim(gcs); %runs simulation.
17    end
18 end

D.2 Simulink Model
This is the Aggregated 'n'-level B2B MMC model, this means:

- All power modules in one arm is modelled as a complete switching function with one shared capacitor.
- The model inhibits capacitor voltage dynamics that assumes perfect balancing algorithm.
- The model includes arm current and circulating current dynamics.

To use this model, Initialize the Matlab script.

- 'n' can be changed to edit the amount of mmc levels of the VSR and VSI.

Figure D.1: Main simulation model in Simulink - Front panel.
Figure D.2: The MMC converter arms of the inverter - Identical as rectifier.

Figure D.3: Electrical source of model. Able to program voltage dips applied to the electrical model.
Figure D.4: Equivalent model of T1, as CERN transformers presented in the system parameters.

Figure D.5: Equivalent model of T2, as CERN transformers presented in system parameters.
Figure D.6: Overall load network in the simulation model. Including dynamic power load, ideal load, and a switchable load for simulating load increase.

Figure D.7: The dynamic model, including constant power source and injection of harmonics if enabled.
Figure D.8: Overall control system for rectifier.

Figure D.9: Overall control system for inverter.
Figure D.10: The AC voltage controller of the inverter - creating d-axis current reference.

Figure D.11: The reactive power controller of the inverter - creating the q-axis current reference.

Figure D.12: The DC voltage controller of the rectifier - creating the d-axis current reference.
Figure D.13: The AC voltage controller of the rectifier - creating the q-axis current reference. Often called the reactive power support for the upstream network.

Figure D.14: Transformations of AC signals for the control system - Identical for both rectifier and inverter.
Figure D.15: Inner current controller of the MMC - Identical for both rectifier and inverter.
Figure D.16: Circulating current suppression controller (CCSC) for the MMC - Operating in dq-frame.
Figure D.17: Zero sequence controller developed in case zero sequence currents are allowed to flow. Based on PR controller and AC signals.

Figure D.18: Pulse generation for the MMC based on reference modulation signals produced by control loops.
Figure D.19: Power calculations used for the HVDC MMC system.

Figure D.20: Resistor for energising of the MMC converters during start-up.
Figure D.21: Thyristor bypass system for the MMC converter, allowing fault current to pass.
Appendix E

CERN Distribution Network

Figure E.1: Electrical distribution network feeding the LHC machine.
Figure E.2: Complete electrical distribution network of CERN.
Appendix F

Footprint Estimation

Mackinac Back-to-Back HVDC Station
138kV AC – 200MVA – DC-bus: 132kV

64m

20m

Figure F.1: Mackinac BTB HVDC converter station footprint - Captured using Google Maps.
Figure F.2: Proposed MMC submodule rack configuration and dimensions.