Upgrade of the ATLAS Muon Spectrometer Thin Gap Chambers and their electronics for the HL-LHC phase

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Outline

- ATLAS upgrade projects
- sTGC-NSW upgrade project
- Replacement of the EIL4 TGC chambers
- Upgrade of the TGC electronics
- Summary
ATLAS detector

- Great operation in Run1 and Run2
  - For example, more than 99% of TGC chambers were operational
LHC Plan

- Instantaneous luminosity to reach $7.5 \times 10^{34} \text{ cm}^{-2}\text{s}^{-1}$ at HL-LHC
  - Total integrated luminosity: $3000 \text{ fb}^{-1}$ after 10 years (in 2036)
  - Average pile-up of 200 interactions

Some ATLAS upgrade projects:
- Insertable B-layer
- New Small Wheel
- LAr calorimeter electronics
- Fast Tracker
- Muon system
  - Inner Tracker (ITK), Pixel and Strip
  - LAr and Tile Calorimeters
  - Trigger and Data Acquisition System
Upgrade of ATLAS Thin Gap chambers

• Phase-I, **NSW TDR: ATLAS-TDR-020**
  - Replacing the innermost muon end-cap station with the New Small Wheels (NSWs), which have small-strip TGC and MM

• Phase-II, **muon TDR: ATLAS-TDR-026**
  - Replacing the EIL4 TGC, innermost endcap station
  - Replacing the electronics of the TGCs at the 2nd muon station

Layout of the Phase-II ATLAS muon spectrometer
Current TGC at high event pileup

- Currently, endcap trigger decision is based on the big wheel TGCs

Combining the NSW and Big Wheel EM track segments can identify muons coming the interaction point, reducing large fraction of fake (eliminating B and C candidates)

Trigger efficiency **without** the EIL4 replacement (1.0-1.3) and NSW (1.3-2.5)
- Trigger efficiency drops significantly in the endcap region due to cavern background
Phase-I
ATLAS small-strip Thin Gap Chambers
ATLAS New Small Wheel

• NSW has 2 gaseous chamber technologies
  ▪ small-strip Thin Gap Chamber (sTGC)
  ▪ Micromegas (MM)
• NSW is designed to provide
  ▪ High-precision trigger and tracking capability
  ▪ To operate efficiently at Run-3 and beyond

Layout of a small sector
sTGC detector

- Used for both muon triggering (primary trigger device for NSW) and precision tracking in regions $1.3 < |\eta| < 2.5$
- Designed to provide angular resolution better than 1 mrad
- Two wedges of 4 layers each, for a total of 8 gas chambers
sTGC internal structure

- Pads: mainly for triggering
- Wires: azimuth coordinate
  - 50 um gold-plated tungsten
  - 1.8-mm pitch
- Strips: eta coordinate
  - pitch of 3.2 mm,
  - providing spatial resolution better than 150 um
- Gas mixture: 55% CO2 and 45% n-pentane
STGC alignment

- V-shaped and flat brass inserts
  - Position and rotation of strips
  - Alignment of gas gaps

Alignment pin

V-shaped brass insert

Alignment pin

Flat brass insert pin

L1, first strip
L2
L3, middle strip
L4, last strip

θ

d1
d0
d2

Pad
Strip
Honeycomb
Gas gap
Pad
Strip
Honeycomb
Gas gap
Pad
Strip
Honeycomb
Gas gap
Pad
Honeycomb

Layout of one quadruplet
sTGC Trigger

- Pad layers are staggered by half a pad to make “logical” pad towers
- Trigger algorithm consists of two steps:
  - Independent single wedge trigger: require hit in 3 out of 4 layers
  - Pad trigger: decision based on geometrical matching between the two wedge triggers

\[ L = 3 \times 10^{34} \, \text{cm}^{-1}s^{-1} \]
sTGC construction

Graphite spraying

Half-gap production

Wire winding of pad cathodes

Gap closing

Gap testing

Doublet assembling

Doublet testing

Quadruplet assembling

Adapter board mounting

Cosmic-ray testing

Wedge assembly and integration (CERN)
X-ray scans

- Measure gain uniformity of gas gaps at 3200 V
- Probe internal structure of gaps
- Gaps with poor gain uniformity are rejected
Cosmic tests

- Hit maps
- 2D efficiency maps
- Noise measurement
- Spatial resolution and misalignment correction

Number of cosmic muons counted in a QS1 gap during a period of approximately 13 hours
- Low hit count on the edges due to the finite size of the scintillators

Preliminary 2D efficiency of strip channels of a QS3 gap at a operation voltage of 3100 V.
STGC testbeam at CERN

- Three quadruplets tested with beam at CERN in October 2018
  - Quadruplets instrumented with 4 pad and 4 strip front-end boards
  - Data taken at 2.8 kV, 2.9 kV, 3.0 kV and 3.1 kV
  - Studies of gap efficiency and strip resolution
    - Analysis of data is ongoing
Integration at CERN

- Assemble sTGC quadruplets into wedges
- Install the electronics and services
- Integrate sTGC and MM into sectors
- Wheel assembly

Assembly of a small sTGC wedge

Both new JDs with spokes for small sectors
Phase-II TGC Upgrade Projects
ATLAS EIL4 TGC

• EIL4, made of two gas gaps, are not designed to be part of the trigger system in the endcap region
  ▪ Region of interest of ~ 1 m²
• EIL4 hit data can reduce significantly the fake trigger rate
  ▪ Providing an extra OR logic to the trigger system
• High hit rate at the HL-LHC degrades the rejection power of the current EIL4 TGC
Design of Phase-II EIL4 chambers

- Replace current EIL4 TGC (doublets) with triplet thin gap chambers
  - Finer granularity
  - More robust 2 out of 3 coincidence
- Expect the project to ramp up after the sTGC production is over

Gas gaps
TGC trigger for the HL-LHC

- Maintain trigger rates of single muons with low momentum at manageable level at the HL-LHC
- Upgrade to modern electronics
  - Increase trigger rate capacity up to 4 MHz (first-level trigger)
  - Allow robust trigger algorithm

![Diagram of proposed first-level trigger logic](image)
Upgrade of the TGC electronics

- All TGC electronics will be replaced, except the ADS boards
- Development is underway
- Prototypes of PS boards are produced with all requirements for HL-LHC
- Testbeam and irradiation tests done

ASD: Amplifier–shaper–discriminator
PS: Patch Panel ASIC and Slave ASIC
Testing of a PS prototype board

- Test of a prototype board at the H8 beam line at CERN done in Fall 2016
  - Demonstrate stable data transfer of 2 x 8 Gbps, and control and monitor of ASD boards through PP-ASIC

- Gamma irradiation test of PS board components (PP-ASIC, DAC and ADC chips) at Nagoya University
  - Demonstrate all components satisfy the requirements for the HL-LHC

<table>
<thead>
<tr>
<th>Component</th>
<th>Ionizing dose</th>
<th>Requirement for HL-LHC</th>
</tr>
</thead>
<tbody>
<tr>
<td>PP-ASIC</td>
<td>10 kGy</td>
<td>27 Gy</td>
</tr>
<tr>
<td>DAC, ADC</td>
<td>180 Gy</td>
<td>180 Gy</td>
</tr>
</tbody>
</table>
Phase-II TGC trigger performance

- Upgrade sector logic to exploit all hits available
  - Replace current TGC logic (2/3 & 3/4 coincidence) with track segment with requirement on number of hits (hits in at least 5 of the 7 layers)
- Combine NSW track segment with TGC track segment
  - Reduce trigger rate by 30%, mainly by eliminating fake triggers, in the region $1.3 < |\eta| < 2.4$ for nominal threshold $p_T = 20$ GeV
Summary

• Upgrades of the ATLAS TGC chambers are foreseen following the LHC upgrade program

• sTGC chambers will replace part of the inner ATLAS muon station in the endcap region
  ▪ Production is underway at all construction sites
  ▪ Integration at CERN is progressing well
  ▪ Performance of chambers are evaluated with cosmic muons and tests with beam at CERN

• Replacement of current EIL4 TGC doublets with triplets for the HL-LHC allows more robust triggering

• Phase-II upgrade of the TGC electronics improves TGC trigger with more refined algorithms, reducing significantly the fake trigger rate
Backup
sTGC Electronics

- NSW electronics overview scheme
  - Satisfy the Phase-II requirement on first-level trigger rate of 1 MHz
Phase-II TGC PS board

- Patch Panel ASIC and Slave ASIC (PS) board has all functionalities required for the HL-LHC

**PP-ASIC**
- 8 x 32 channels = 256 channels
- Eliminate timing differences, determine bunch crossing and synchronize to LHC clock

**FPGA**
- Data transmitter between PP-ASIC and sector logic
- Bandwidth of 16 Gbps

**DAC and ADC**
- Apply and monitor threshold voltage to ASD chips