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**Abstract:**

The main goal of WP6 is to develop novel high voltage/high resistivity (HV/HR) CMOS active sensors for High Energy Physics applications. Within the WP6.4 activities, Optimised Interconnection Processes (hybridization procedures) between depleted CMOS sensors and state-of-the-art readout chips were investigated. The studied AC and DC coupling processes require precise alignment between the active sensor and the chip so that each pixel is connected. The AC coupling techniques consisted in gluing both substrates with various glues using a precise pick and place process. Bump-bonded devices, where all the pixels were DC coupled with solder bumps or some pixels were DC coupled and others AC coupled, were also produced. HV/HR CMOS structures developed within the AIDA-2020 project (as part of the WP6.3 activities) were used as active sensors (H35demo and LFCPIX) and interconnected to the FE-I4 readout chip.
AIDA-2020 Consortium, 2019
For more information on AIDA-2020, its partners and contributors please see www.cern.ch/AIDA2020

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Executive summary

The aim of the WP6 is to investigate High Voltage and Resistive (HV/HR) CMOS Sensors for high energy physics and other applications. There are two types of active CMOS sensors: monolithic devices, where sensor and electronics are placed in a single substrate, and hybrid devices, where the active sensor and the readout electronics are placed in two separate substrates and interconnected with solder bumps (DC) or through capacitive coupling (AC). The hybridization process is technically demanding since the pixel size is extremely small (tens of micro-meters). Two active sensors developed within WP6.3 were interconnected in various forms to the ATLAS FE-I4 readout chip.

These two techniques have been investigated and optimised at various sites within the AIDA 2020 collaboration. For example, with the AC coupling of structures, various glues (including tape) were investigated for interconnection. A SET Accura 100 flip-chip machine was used for the hybridization. And it was shown that the use of pillars to aid the hybridization process improved the uniformity of the capacitive coupling significantly.

For the DC coupling of devices, the process known as under-bump metallization (UBM) was required. This was deposited on the sensor. The readout chips need to have solder bumps. A procedure to protect the wire-bond pads during the UBM deposition on the active sensor was developed and showed a significant improvement. Flip-chips were done with a SET FC150 machine.

These developments with AC and DC coupled devices have made the process more robust and have improved the reliability of the process. Various sites within AIDA 2020 can now produce devices using this technology.

1. INTRODUCTION

The goal of the WP6 is to investigate High Voltage and Resistive (HV/HR) CMOS sensors for high energy physics. Active CMOS devices can be monolithic, where sensor and electronics are placed in a single substrate, or can be used in hybrid devices, where the active sensor and the readout electronics are two separate substrates interconnected with solder bumps (DC) or through capacitive coupling (AC). The hybridization process is technically demanding since the pixel size is extremely small (tens of micro-meters). The aim of the WP6.4 activities is to investigate and develop technical solutions for the hybridization procedure, both for AC coupled and DC coupled devices.

AC coupled devices consisting of a depleted active CMOS sensor and a readout chip that have been fabricated before (see for example [1]). However, these previous devices were very small in size (typically few mm²). Within the WP6.4 activities the first full sized (2-4 cm²) AC and DC coupled depleted CMOS devices were fabricated and tested.

The hybridization step is complicated and requires the precise alignment between the active sensor and the readout chip. In AC coupled devices the measure of the quality of the hybridization procedure is given by the uniformity of the capacitive coupling between pixels (the spread of the capacitance of the connections should be small, ideally lower than 10%). This uniformity is needed to ensure successful operation of the devices. For DC coupled devices, the quality is mostly given by percentage of connected pixels (failure rates should be below 1% or so).

Section 2 presents the AC coupling studies carried out with test structures that allow a direct measurement of the capacitance of each connection. Several methods of gluing were investigated to fine tune the procedure. Section 3 presents the results of DC coupled devices produced with the
the wafer level packaging.

2. AC COUPLED STUDIES

Test structures to study the performance of different methods of fabrication of AC coupled devices
were designed and produced by INFN-GE [5]. The main idea is to use a matrix of capacitors to test
the uniformity of the glueing process. Two structures, each containing one side of the capacitor were
produced in 150 mm wafers (500 µm thick fused quartz) with 1.2 µm Al electrodes at MicroFab
Solutions (Trento). The structures are shown in Figure 1. The procedure is to deposit the glue on top
of one of the structures, and then align both structures (one with glue, one without) and apply pressure
to produce the hybrid device. By probing the pads in the edge of the device, the capacitance of the
different “pixels” can be measured. Some structures were fabricated with pillars, which ultimately
were shown to improve uniformity. Pillars of different height (3 and 5 µm) were deposited on 3
wafers through a photolithography process.

![Pattern pillars by mask](image1.png)

*Figure 1. Process of fabrication of test structures for AC coupling studies (left). Details of the structures are shown on
the right. The sample size is 1.5 x 1.5 mm². The pads to measure the capacitance of each pixel can be seen.*

To produce the assemblies, different glues were used: Araldite 2011, 2020 and Masterbond
(UV15DC80LV) and Tesa tape. The assemblies were fabricated at UNIGE, using an Accura 100 flip-
chip machine and a high temperature and pressure cycle to cure the glue. A detail of the assembly is
shown in Figure 2.
The best results were obtained with 5 µm pillars and Araldite 2011, applying a 20 N force and a curing cycle of 60 seconds at 100 °C. Measuring the capacitance using a probe with frequencies between 1 kHz to 5 MHz and applying 1 V (DC) with an oscillation of 50 mV, a spread of about 10% between the pixels was measured (see Figure 3). The mean capacitance was about 5 pF, which is in reasonable agreement with the expectations if the glue relative permittivity is assumed to be ε_r = 3.2. These encouraging results on test structures were followed by the fabrication of full-sized assemblies based on the H35demo depleted CMOS prototype.

The procedure presented above was used to produce AC coupled assemblies with the H35Demo active sensor [2] and the FE-I4 chip [4].

The H35Demo is a demonstrator chip produced in the 350 nm AMS technology by KIT, IFAE, UNIGE and the UNILIV. It is a large area chip, 18.49 x 24.40 mm², developed to investigate the
possibility to install AMS HV-CMOS devices in the ATLAS ITk\(^1\). The H35Demo chip has been produced on wafers of different resistivities: 20, 80, 200 and 1000 \(\Omega\)cm.

The H35Demo chip contains four pixel matrices: a standalone (monolithic) nMOS matrix, two analog matrices and a standalone CMOS matrix. The pixel size is 50x250 \(\mu\)m\(^2\) in all the matrices while the number of pixels is 16 rows \(\times\) 300 columns in the nMOS and CMOS matrices and 23 rows \(\times\) 300 columns in the analog matrices. The sensors are implemented through the p-n junctions made by the deep N wells in the p-doped substrate.

Within the WP6.4 activities, H35demo sensors were AC (This Section) and DC coupled (Section 3) to the FE-I4 readout chip as presented below.

A glue dispensing machine was used to deposit a thin layer of epoxy glue with good uniformity over the H35demo. A high-precision flip-chip machine was used to align and perform the gluing cycle (heat and apply pressure) in order to capacitively couple the sensors to the FE-I4 ASICs (see Figure 4).

During the production, several mechanical samples were assembled and inspected. Cross-section and metrology studies were performed on the glue interface to verify the parallelism and measure the distance between the H35Demo and FE-I4 pads. The measurements demonstrated that the process developed produces assemblies with a good parallelism, i.e. less than 100 nm difference in silicon to silicon distance over the whole assembly, and good control of the distance between the coupling pads on the H35Demo and the FE-I4 ASIC. Electromagnetic finite-element analysis was performed with accurate models of both chip metallisation to extract the expected coupling capacitance between the pads. A capacitance of 3.5 fF was estimated. A pulse of 300 mV from the H35Demo amplifier would then result in a 6500 e in the FE-I4 amplifier [6].

![Image of deposition of epoxy](https://example.com/epoxy deposition.png)

*Figure 4. Left: deposition of epoxy on the H35DEMO matrix by the automatic glue time-pressure dispenser of the Accura 100. Right: 100 \(\mu\)m thin H35DEMO-FE-I4 assembly on PCB. From [6].*

It should be noted that to industrialize the AC coupling procedure a wafer level process would be desirable. With this in mind, wafer level packaging at MicroFab was investigated to obtain larger detectors reassembling good tiles on a full wafer and thus carry out the AC coupling process at wafer level [5]. See Section 4.

\(^1\) ATLAS ITk has since decided against installing CMOS devices.
3. DC COUPLED STUDIES

Another approach that was investigated within the WP6.5 activities by IFAE was the DC coupling of depleted CMOS sensors to ASICs or a combination of both AC and DC coupling (were some pixels are AC and others DC coupled). To produce DC/AC coupled devices it is necessary to perform the full bump-bonding cycle (even if only a fraction of bumps is present). The procedure is the following:

- FE-I4 chips with solder bumps are used. A fraction of the bumps was removed (using a DAGE pull and shear machine) in some ASICs to combine AC and DC pixels.
- The under-bump metalization (UBM) has to be deposited on the H35Demo active sensor. This was done at CNM-Barcelona with electroless UBM. Kapton tape was placed on the wire-bonding pads to avoid shorts on them (this problem was caused by the short distance between pads in the H35Demo, of only 10 μm, see Figures 5 and 6).
- The hybridization process (flip-chip) consists of the alignment of the H35Demo and the FE-I4, and the heating and pressure cycle.

![Image: DC COUPLED STUDIES](image)

**Figure 5.** The bond pads and the UBM on the pixel pads after the UBM process.

![Image: DC COUPLED STUDIES](image)

**Figure 6.** (a) Shorts of wirebond pads after H35Demo UBM (before the tape method was employed). (b) Wirebond pad protection before UBM. (c) Assembly combining AC and DC coupled pixels after bump-bonding.
Several assemblies were produced at IFAE (see Figure 6) and inspected with X-rays. Figure 7 shows the full view of a device where the AC coupled pixel region, with no bumps visible, is indicated in red.

![Image](image_url)

*Figure 7. X-ray image of a hybrid CMOS device. The H35Demo active sensor has pixels that are DC coupled (with solder bumps) and AC coupled (red region) to the FE-I4 readout chip.*

The LFCPIX chip is a full-size prototype designed in LFoundry 150 nm HV-CMOS process [3]. The chip size is about 1 cm². Three different pixel matrices are included in the chip, one is optimized to be bump-bonded to the FE-I4 chip, one can be AC coupled to the FE-I4 and the third one is mostly intended for stand-alone usage.

The procedure described above was also used to produce LFCPIX assemblies DC coupled to the FE-I4 chip. As the wirebond pads are well separated in the LFCPIX, they needed no protection during the electroless UBM performed at CNM (Figure 9). The flip-chip was performed by IFAE (see Figure 8) as were the X-ray inspections (see Figure 9).

![Image](image_url)

*Figure 8: Good UBM on the pads of the LFCPIX device.*
4. **WAFER LEVEL PACKAGING**

Wafer Level Packaging (WLP) is a process developed with the goal of rebuilding a wafer structure starting from previously diced chips. The aim is to exploit this technique to build larger detectors (reassembling good tiles on a full wafer) and performing wafer-to-wafer bonding.
4.1 Process flow

The process flow is shown in Figure 11. The first step of the process consists in the application of a thermal release tape (by lamination) on a carrier, in order to protect the electronic components. The carrier is a support wafer which is placed inside the mold cavity to reduce its depth. It is possible to regulate the thickness of the final wafer, by using carrier wafers with different thickness.

The use of a carrier facilitates the pick and place phase. In this phase the chips are placed on the tape by using patterns for the alignment (Figure 12). A typical pick and place machine can reach a precision of 0.5 µm in the positioning of the chips.

Once the carrier is filled with chips, the compression moulding can start. The moulding material is first placed in an open mould cavity (where the chips were placed). The mould is closed with a top controlled force while heat and pressure are maintained until the moulding compound has cured. Then
the mould is removed and the moulding material is heated (foaming). Finally, the carrier and the tape are released (peeling). The wafer is ready to perform wafer-to-wafer bonding processes (see Figure 13).

![Figure 13: Example of a wafer built with the Wafer Level Processing.](image)

The carrier-tape removal operation is a very delicate process, in fact, this is the phase with the highest risk to damage the final wafer: the thinner is the wafer the higher is the risk to damage it. The tape-resin combination choice deeply affects the structural integrity of the wafer during the peeling phase.

### 4.2 Wafer Measurements

Six wafers were produced by MicroFab Solutions: two different filling schemes were used (full or cross) for three different wafer thickness (675 µm, 400 µm, 300 µm). The resulting wafers are strong enough to be handled. One wafer was damaged due to the force applied during the tape removal. The wafers were sent to INFN GE in order to measure their planarity and the precision of the chips positioning. The measurements were performed with a KLA P-7 Profilometer.

![Figure 14: Profile measurement of two wafers with different thickness (orange: 300 µm, blue: 400 µm).](image)

In Figure 14, the results of the profile measurement of two wafers with different thickness are presented (orange: 300 µm, blue: 400 µm). The wafer with 400 µm thickness presents a bending point in the separation between two chips, visible in both X and Y profiles. The wafer with 300 µm thickness does not present such a feature and the planarity is improved (overall bowing below 100 µm). The improvement is due to a different tape choice. The tape used for the 675 µm and 400 µm wafers was hard to separate from the moulding compound, therefore a high force was applied during
the tape removal. The new tape used for the 300 µm wafers (easily detachable from the moulding compound) avoided the formation of bending points and improved the planarity.
5. CONCLUSIONS

The WP6.4 activities were aimed at developing AC and DC hybridization procedures for HV/HR CMOS sensors. To this end, test structures were used to fine tune the AC coupling process. AC coupled devices based on the H35Demo and the FE-I4 ASIC were successfully produced and tested. In parallel, H35Demo devices that combine AC and DC coupled pixels to the FE-I4 chip were also fabricated. Finally, LFCPIX DC coupled devices were produced.

To optimize the interconnection process various improvements were developed and difficulties overcome. The difficulty in obtaining uniform capacitive coupling between the substrates was overcome with the use of pillars (Section 2). This pillar deposition technique was developed with industry at MicroFab Solutions (Trento). The problems that were encountered with the disposition of electroless UBM shorting to the wirebond pads on the readout chip was solved with protective tape. The electroless UBM process is more cost effective than the electroplating deposition and is widely used in the microelectronics industry. The process to obtain DC bump-bonded devices with SnAg bumps was developed on precise alignment machinery in serval AIDA institutes (IFAE, UNILIV and Geneva).

However, it is important to note that the focus of the WP6 activities has changed from hybrid coupled devices to monolithic devices (where no hybridization step is needed). Nonetheless the program within WP6.4 resulted in several advancements in key techniques highlighted above that may be of use in future interconnection processes. These improved techniques with both AC and DC coupled devices have been used to produce modules that have been delivered to the AIDA-2020 community.
6. REFERENCES


