Development of the Compact Processing Module for the ATLAS Tile Calorimeter Phase-II Upgrade

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on behalf of the ATLAS Tile Calorimeter System

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OUTLINE

• INTRODUCTION
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  – PHASE II UPGRADE

• TILE PPR DEMONSTRATOR
  – HARDWARE AND Firmware
  – TEST BEAM CAMPAIGNS

• COMPACT PROCESSING MODULE
  – HARDWARE AND PCB LAYOUT
  – ATCA CARRIER BOARD
  – FUTURE PLANS

• SUMMARY
INTRODUCTION
ATLAS Tile Calorimeter

- Segmented calorimeter made of steel plates and plastic scintillator tiles covering the most central region of the ATLAS experiment
- Measures energies of hadrons, jets, τ-leptons and $E_T^{miss}$
- 4 partitions: EBA, LBA, LBC, EBC
- Each partition has 64 modules
  - One drawer hosts up to 48 PMTs
- Light produced by a charged particle passing through a plastic scintillating tile is transmitted to the PMTs
- Scintillator tiles are read out using wavelength shifting fibers coupled to PMTs
- Around 10,000 readout channels
High Luminosity-LHC

- LHC plans to increase the instantaneous luminosity by a factor 5-7 around 2026 → **High Luminosity-LHC**
  - Expected number of collision per bunch crossing will increase up to 200
  - New Trigger and Data AcQuisition architecture with full granularity and digital inputs

- **TileCal**: Major replacement of on-detector and off-detector readout electronics
  - Aging of electronics due to time and radiation
  - Current readout system will not be compatible with the upgraded TDAQ architecture
  - Other detector elements as scintillators or PMTs will be kept
New readout strategy for HL-LHC

- On-detector electronics will transmit full digital data to the off-electronics at the LHC frequency → **40 Tbps to read out the entire detector and ~6,000 optical fibres**
- Buffer pipelines are moved to off-detector electronics
- Redundancy in data links and power distribution → improve system reliability
- **Tile PreProcessor** is the core element of the off-detector electronics
  - Data processing and handling from on-detector electronics
  - Clock and DCS distribution towards the TileCal modules
  - Interface with the ATLAS trigger and ATLAS readout systems (FELIX)

- **32** **TilePPr** boards in ATCA format: ATCA carrier + 4 **Compact Processing Modules**

- **32** **TileTDAQ-I**: Interfaces with L0Calo, Global, L0Muon and FELIX system
TILE PPR DEMONSTRATOR
Tile PreProcessor Demonstrator

- Fully functional prototype - Demonstrator
  - Double mid-size AMC (μTCA / ATCA carrier)
  - Xilinx Virtex 7 (48 GTX), Kintex 7 (28 GTX)
  - 4 QSFPs, TX+RX Avago MiniPODs
  - TI CDCE62005 jitter cleaner + ADN2814

- 1/2 of the Compact Processing Module
  - Operates 1 TileCal module → 160 Gbps
  - Half number of optical channels

- Interfaces with legacy and Phase II ATLAS readout systems (ROD, FELIX)

- CPM hw & fw design largely based on this system
Firmware

- 16 GBT links with on-detector electronics
  - 9.6 Gbps for uplinks, 4.8 Gbps for downlinks
- Different blocks for data handling, DCS configuration and monitoring
- 96 pipelines memories with 12.8 μs depth (48 PMT channels x 2 gains)
- TTC decodification
  - Level-1 Accept signal and commands
  - LHC clock recovery
- Three different readout paths:
  - FELIX (GBT)
  - ROD (G-Link)
  - Ethernet port (IPBus)
- Controlled through Ethernet – IPBus

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Test Beam setup

- Located at the **Super Proton Synchrotron (SPS)** North Area on the H8 beam line
  - **7 test beam campaigns** between 2015 and 2018

- Detector modules equipped with upgraded and legacy electronics for performance comparison
  - Front-end electronics configuration
  - Physics, calibration and laser runs
  - HV and LV control/monitoring
  - Data taking through FELIX / legacy system

- **Fully integrated** with the ATLAS TDAQ software and DCS system
  - Detector modules equipped with upgraded and legacy electronics for performance comparison

- **Demonstrator** module inserted into ATLAS experiment last July!!

**Beams of Hadrons, Electrons and Muons** were used to study the calorimeter response

Test beam setup at H8 line
COMPACT PROCESSING MODULE
Compact Processing Module - overview

- Single AMC board with full-size form factor (6HP*)
  - 32 channels through 8 Samtec Firefly modules
  - 14 channels through AMC connector
  - 60W power budget
- High bandwidth readout system
  - Up to 400 Gbps via optics
  - Up to 175 Gbps via electrical backplane

* Dimensions: 73.8 mm x 28.95 mm x 180.5 mm

1 TilePPR → 4 CPM + 1 ATCA carrier
Kintex UltraScale FPGA

- High-speed interface with on-detector electronics → 32 links@4.8/9.6 Gbps
  - Operation and readout of 2 TileCal modules: **96 PMT channels with 2 gains**
  - Real-time energy reconstruction @40 MHz **per channel and gain**
  - Data buffering of 10 µs **per channel and gain**

- High-speed interface with ATLAS trigger system and FELIX
  - Reconstructed energy **per cell** to TDAQi @40 MHz → 4 links@9.6 Gbps
  - Level-0 trigger selected events to FELIX @1 MHz → 1 link@9.6 Gbps

- Using KU115 as baseline and KU085 for prototyping
Artix 7 FPGA & Peripherals

- **Artix 7 FPGA** provides **slow control** and **monitoring** for all the peripherals
  - Configuration/monitoring of the Ethernet PHY, optical modules and sensors
  - Power management and monitoring through a LTC2980 chip
  - Implementation of a clock phase monitoring system based on the **DDMTD circuit**

- High-performance **jitter cleaner** to distribute the clock to the KU transceivers → **Silicon Labs SI5345**
  - LHC clock recovered from FELIX interface and distributed back to the Kintex UltraScale

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![Diagram](image-url)
Optical modules and mechanics

- 8 FireFly modules connected to the KU FPGA
  - Limited area on the PCB and front panel
  - 4 RX/TX channels up to 14 Gbps
  - 2 Firefly modules connected to a single MXC connector

- Fibre routing on the CPM PCB is challenging
  - Maximum bend radius of fibres is 7.5mm
  - Minimum fibre length + FireFly is 11 cm (Samtec)
  - Plastic clip wires to route the fibers - Essentra MWSET

Mechanical mockup of the Compact Processing Module
PCB layout design

- **Total of 14 layers** → 1.6 mm thickness
  - 8 layers for PWR/GND, 6 layers for signals
  - ISOLA FR408HR ($\varepsilon_r = 3.68$, tan $\delta = 0.0092$)

- **High-speed** layout design and **optimization**
  - Supression of impedance discontinuities: Differential vias, DC-blocking caps
  - Intra-pair skew compensation to reduce differential to common mode conversion
  - Post-layout simulations using IBIS-AMI models
  - Mixed-mode S-parameters computation for crosstalk studies: FEXT and NEXT

- **IR drops** on the more demanding power planes
  - VCCINT (0.95V) drains up to 15A
ATCA Carrier Base Board

- ATCA cutaway carrier
- Zone 1: Power distribution to CPMs and TDAQ-I - Max power of 400 W
- Zone 2: GbE + XAUI 10G
  - Base & Fabric: Communication with rest of the ecosystem
- Zone 3: Communication between CPMs and TDAQ-I / FELIX
- Three on-board mezzanines
  - CERN IPMC board
    - Power and sensor management
  - TileCoM Zynq-based board
    - FPGA remote programming
    - Interface with DCS system
  - 16 GbE port switch SODIMM
    - CPMs GbE communication
## Plans for upcoming years

<table>
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<th>Year</th>
<th>Activities</th>
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- **First prototypes**
- **Electrical tests**
- **Optical tests**
- **Firmware**
- **Validation**

- **2019**
  - First prototypes being manufactured now
- **2020**
  - Preproduction (25%) from Q3 2020 to Q1 2022
    - 8 ATCA carriers, 32 CPMs
- **2021**
  - Preproduction
  - Test bench design
  - Integration tests at CERN
  - Validation at test-benches
- **2022**
  - Tendering process
  - Final production
  - Validation and shipping
  - Final integration tests
- **2023**
  - Installation of ATCA crates
  - Tests in ATLAS with on-detector and Trigger electronics
- **2024**
  - Installation in ATLAS

**128 CPMs in total**
Summary

- New conditions imposed by HL-LHC requires the complete redesign of the TileCal on-detector and off-detector electronics

- Tile PreProcessor boards for the Phase II Upgrade under development
  - 32 x (ATCA carrier + 4 Compact Processing Modules) to read out TileCal
  - Total bandwidth of 40 Tbps between on-detector and off-detector

- Fully operational PreProcessor Demonstrator has been qualified
  - Capable of operate one TileCal module → ½ number of channels w.r.t. one CPM
  - Extensively tested in several test beam campaigns between 2015 and 2018

- First CPM prototypes are under production now
  - Largely based on PPr Demonstrator
  - 8 Firefly optical modules, Kintex UltraScale, Artix 7 → single AMC form factor
  - Many signal and power integrity studies done during layout design
  - Mechanical boards to plan the fiber routing – critical step
  - Preproduction in 2020, final production in 2022 and installation in 2024
Thank you for your attention!
Phase II on-detector electronics

- The **Phase II module** is composed of 4 mini-drawers (48 PMTs). Each mini-drawer have 2 independent read out sections for redundant cell readout
  - 12 PMTs + 12 front-end boards reading out 6 TileCal cells
  - 1 × MainBoard: operation and signal digitization of the front-end boards
  - 1 × DaughterBoard: data high-speed link with the off-detector electronics
  - 1 × High Voltage regulation board
  - 1 × Low Voltage Power Supply (LVPS): low voltage power distribution
DaughterBoard

• High-speed link with the back-end electronics
  – Data collection and transmission
  – Clock and command distribution
  – Data link redundancy

• Daughterboard version 5
  – 2 × GigaBit Transceiver (GBT) chips
  – 2 × Xilinx UltraScale+ FPGAs
  – 4 × SFP modules → ~40 Gbps

• TID tests with ~ 9 MeV electron beam

• SEE and SEL tests done with 58 MeV and 226 MeV proton beam
  – Soft error rate is low → Triple redundancy
  – No destructive effects observed
Front-End Boards and MainBoard

- **Front-end boards**: FENICS cards
  - PMT pulse shaping
  - Shaper with bi-gain output: $1 \times \text{LG} + 1 \times \text{HG}$
  - High precision slow integrator
  - Design based on current 3in1 cards
    - Improved noise and linearity
    - Improved calibration circuitry

- **MainBoard**
  - Digitize analog signals coming from 12 FEBs
  - Routes the digitized data from the ADCs to the DaughterBoards
  - Digital control of the FEBs
  - HG and LG, 12-bit samples @40 Msps
  - TID, NIEL, SEE tests performed
TilePPPr Demonstrator - overview

- First prototypes delivered at the end of 2014
- Extensively used in test beams and labs
- Power consumption below 60 W

- PCB stack-up: 16 layers
  - Dielectric Nelco N4000-13SI
- 4 QSFP modules: 160 Gbps
- Avago MiniPOD: 120 Gbps
- Backplane: 40 Gbps

- 320 Gbps

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- **Xilinx Spartan 6**
  - Slow control capabilities

- **Module Management Controller (MMC)**
  - Power connection management

- **AMC connector**
  - 12 V power connection
  - High-speed communication path

- **FMC connector**
  - Expansion functionalities

- **DDR3 512MB**

- **2 x CDR IC**
  - ADN2814
  - Clock/data from TTC

- **TTC input**

- **Xilinx Kintex 7 FPGA**
  - XC7K420T
  - 28 transceiver@10 Gbps

- **Xilinx Virtex 7 FPGA**
  - XC7VX485T
  - 48 transceiver@10 Gbps

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**FMC** connector

**DDR3 512MB**

**Xilinx Virtex 7 FPGA**

**TTC input**

**Xilinx Kintex 7 FPGA**

**Module Management Controller (MMC)**

**AMC connector**

**FMC connector**

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**Xilinx Spartan 6**

**Module Management Controller (MMC)**

**AMC connector**

**FMC connector**

**DDR3 512MB**

**Xilinx Virtex 7 FPGA**

**TTC input**

**Xilinx Kintex 7 FPGA**

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F. Carrió - Topical Workshop on Electronics for Particle Physics 2019
FPGA resource usage estimation

- Based on the occupied resources of the PPr Demonstrator
  - ½ channels of a Compact Processing Module

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**General logic:**
- state machines, de/multiplexer, encoder/decoders, etc

**RAM memory:**
- Pipeline buffers and monitoring
- Current fw is 12.8 us

**Clocking circuitry**

**Transceivers:**
- DaughterBoard, TDAQ-I, FELIX, Ethernet

**Energy and time reconstruction:**
- Logic resources < 1%
- Mainly DSP resources
Mezzanine boards

- **Compact, replaceable and upgradeable solution**

- **TileCoM - Computer on Module**
  - Embedded Linux – PetaLinux distribution
  - Remote programming, DCS monitoring, clock generation for standalone tests
  - Xilinx Zynq UltraScale+ XCZU2CG + 512 MB DDR4
  - 10 layers - DDR3 form factor (67.6 mm x 40.00 mm)

- **Ethernet switch module**
  - Unmanaged Ethernet Switch chip Broadcom BCM5396
  - 16 GbE connection between CPMs and TDAQ-I
  - 6 layers - DDR3 form factor (67.6 mm x 30.00 mm)

- **IPMC mezzanine board (CERN)**
  - Microsemi A2F200, DIMM-DDR3 VLP form factor
  - Hot swap, sensor monitoring, power management