Commissioning Readout for the new LHCb VELO

Karol Hennessy on behalf of LHCb VELO

September 6, 2019

University of Liverpool
Overview

- Detector description
- Vertex Locator (VELO) Electronics
- VeloPix ASIC
- Quality Assurance and Production tests
- Issues and their resolution
• Vertex Locator (VELO) for the upgraded LHCb detector
• Silicon pixel modules around the LHC beam interaction region
  • 50fb\(^{-1}\) integrated luminosity for LHC Runs 3 & 4
  • Very high radiation environment
  • maximum fluence approx. 8\times10^{15} \text{MeV} \cdot n_{\text{eq}}/\text{cm}^2
  • In vacuum and under active cooling

• LHCb has triggerless readout - full detector readout @ 40 MHz
Detector Active area = 0.12 m²
Sensor temp. = < −20°C
Distance from beam = 5.1mm
VeloPix ASIC

- Front-end ASIC driving the design of the VELO data acquisition system
- Part of the MediPix/TimePix family
- 130 nm CMOS technology
- 256×256 pixels of 55×55µm²
- Operates at LHC clock rate ~ 40MHz
- Time resolution - 25 ns
VeloPix ASIC

- Readout is data driven - only read out when they have “hits above threshold” (a.k.a. zero-suppression)
- **Binary readout** @ 40 MHz
- **VeloPix** is optimised for high speed readout
  - Peak hit rate: 900 Mhits/s/ASIC
  - Max data rate: 19.2 Gb/s
  - Total VELO: 2.85 Tb/s
- Power consumption < 1.5 W·cm$^{-2}$
- Radiation hard 400 Mrad, and SEU tolerant
- Non-uniform radiation dose

**Average data rate**

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Hybrids

- VeloPix Hybrids
  - 20 high-speed data links @ 5 Gb/s
  - 4 hybrids per module (2 per side)
- GBTx Hybrid
  - Timing and control signals
  - GBLD as a line driver

GBT - [http://cern.ch/go/6rsK](http://cern.ch/go/6rsK)
Hybrid, Cables, Feedthrough

- High speed flex tapes
  - Stripline tech. 200 µm track & gap, 175 µm Pyralux
  - length 550, 561, 575 mm

- Vacuum Feedthrough board
  - bringing all LV, HV, data, control signals to/from modules in vacuum
Opto-Power Board

- Situated on VELO tank exterior
  - Connects to Vacuum Feedthrough Board
  - Fibres to counting room at surface ($\approx 300$ m)
- Interface for data, control, monitoring signals and powering for VELO modules
  - FeastMP DC/DCs for power
  - Voltage monitoring
  - Optical transceivers (VTTx/VTRx) for driving to/from backend
- Control via GBTx and SCA

GBT-SCA - http://cern.ch/go/Zcc9
Backend DAQ and Control - PCIe40

- Single control and readout board for the entire experiment
- Can be used for ECS or DAQ or both
- Common hardware, shared firmware components
- PCIe Gen3 x16
- Intel Arria10 FPGA (10AX115S4F45E3SG)
  - High power consumption - up to 80W FPGA, 157W card
- up to 4 PCIe40 per chassis (ASUS ESC4000-G3, 2x Xeon 3 GHz, 8x 8 GB DDR4)

PCIe40 - http://cern.ch/go/HQ6P

- 48 bi-directional links (or 96 uni-directional) @ ~5 Gb/s
- Output bandwidth 100 Gb/s (measured).
High Speed Pathways

ECS - Experiment Control System
- Bi-directional with GBTx ASIC
- 4.8 Gb/s
- Use of GBLD as electrical line driver (emphasis and amplification functionality)

DAQ - Data Acquisition
- Uni-directional (from VeloPix to back-end)
- 5.12 Gb/s
- VeloPix has some internal emphasis

Similar electrical transmission lines for ECS and DAQ - expect similar performance. CTLE - Continuous Time Linear Equaliser
VeloPix Data readout

- Pixel data is aggregated into groups of $2 \times 4$ called **SuperPixels**
  - 30% reduction in data size
- Data is sent out-of-time $\Rightarrow$ timestamp stored in SuperPixel data packet
- Custom serializer - Gigabit Wireline Transmitter (GWT)
  - Low power - 60 mW
  - 5.12 Gb/s line rate
- GWT protocol
  - scrambled data (30 bit multiplicative)
  - parity check, no error recovery
  - low tolerance for header errors
  - $\Rightarrow$ minimise bit error rate
Production and Testing
Component tests are performed at CERN, Santiago and Glasgow.

Production of the VELO modules is performed at Manchester and NIKHEF.

Assembly of the VELO modules onto their halves are performed at Liverpool.

Final testing and installation will happen at the experiment site next year.

Testing performed at every stage.

Poster by Edgar Lemos Cid (USC)
Quality Assurance

- IV curves, power consumption monitoring, voltage drops
- Band Gap Calibration - best estimate of sensor temperature
- VeloPix equalisation and Noise scan
- Testpulse data taking over high speed links
- Bandwidth saturation tests of HS links
- All full module tests compared to individual component tests

Velo Module: Electrical Testing Checklist

Krisztof De Bruyn
August 13, 2019

https://www.everleaf.com/8979645788hswedjkyjy1

1 Setup of Opto- & Power Board

□ a: The latest stable firmware to use is lhcdaq_firmware_v81_20190406_1_apc_working.suf and has 6 GBT and 20 GWT links. Connect the optical fibres to the VTTx sockets according to the following mapping: (see Fig. 1)

<table>
<thead>
<tr>
<th>Link</th>
<th>0</th>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
<th>5</th>
<th>6</th>
<th>7</th>
<th>8</th>
<th>9</th>
<th>10</th>
<th>11</th>
</tr>
</thead>
<tbody>
<tr>
<td>MPO 0: Fibre ID</td>
<td>6</td>
<td>2</td>
<td>4</td>
<td>8</td>
<td>10</td>
<td>-</td>
<td>12</td>
<td>11</td>
<td>9</td>
<td>7</td>
<td>5</td>
<td>3</td>
</tr>
</tbody>
</table>

□ b: Launch the MiniDAQ configuration panel using the alias accept or accept. (see Fig. 2)

□ c: Make sure the (default) settings for the MiniPd and Subdetector Type match the fibre mapping: (see Fig. 2)

<table>
<thead>
<tr>
<th>Link</th>
<th>MiniPd Subdetector</th>
<th>1 Rx</th>
<th>2 Tx</th>
</tr>
</thead>
<tbody>
<tr>
<td>MiniPd</td>
<td>OIB</td>
<td>Velo</td>
<td>Velo</td>
</tr>
</tbody>
</table>

□ d: Click the buttons Set Polarity and Set Detector. The yellow squares should turn green.

□ e: Launch the OIB configuration panel using the alias accept. (see Fig. 3)

□ f: Step 1: Click the two activate buttons. All five boxes in the B column should get ticked and the three LEDs showing Tx & Rx Ready should become green.

□ g: Step 2: Click the Power On button for GBTs/GWTD, Link1, Link2 and the title you wish to power, or use the All On button. The LEDs should switch from red (off) to green (on) and the displayed voltages should be non-zero.

□ h: Step 3: Click the All Config button. The LEDs should switch from yellow (Not Set) to green (OK).
QA of High speed links

- PRBS test for high speed readout
- Slow control communication tests with OPB and VeloPix
- Timing and fast control checks
Testbeam Q4 2018

- Performed at CERN just prior to the Long Shutdown of SPS
- VeloPix and sensors had been tested in previous beam tests, but never with **full high-speed readout**, and **complete LHCb slow control and DAQ chain**
- Synchronised with Timepix 3 telescope. Allows to check time alignment < 1ns
Testbeam Q4 2018

- Successfully took high-speed data from VeloPix synchronised between 3 module planes
- HV scans, Time-over-Threshold scans, Ikrum (Krummenacher current) scans
- Synchronisation tests
- Some firmware bugs found and fixed
- Integrated with LHCb PCIe40 firmware and software

Poster by Antonio Fernandez Prieto (USC)
GBTx operation down to -38°C

- Upon testing first prototype modules, communication with the GBTx (v2) chip was lost when cooling down to -30°C
- Confirmed on several prototypes
- Investigation using environmental chamber (down to -38°C)
- Using the GBTx I2C programming dongle we see the state is stuck at “WaitDESLock” at low temperatures (< -10°C)
- Replaced 1.49V DCDC supplying GBTx with 1.57V and improved locking. → clue
GBTx Testing in the cold

• CDR circuit frequency lock and phase alignment
• PLL has more noise at low T
• Increase CDR phase detection charge pump current ($I = 0.375 \times \text{<val>} \ \mu A$)
  • from default (0x4 = 1.5μA) to max (0xF = 5.625μA)
• Works! Tested with all mounted GBTx chips thus far
• Jitter measured on 40 MHz output → 1 ps increase in RMS (negligible)

• We burn these settings into our GBTx chips.
• Solution suggested and approved by GBTx team at CERN (Many Thanks!)
Equalisation and Noise

- Noise is measured by counting the number of hits over threshold in a given time window (shutter)
- Equalisation is performed using a Global Threshold setting and a fine trim DAC setting
- Pixel data can be read over ECS link or DAQ links
- Noise data is taken in “ECS mode” over the control links.
Equalisation and Noise

- Double-peak structure over VeloPix
- Correlated with column number
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- Grossly affected by shutter length
- Proposed solution is to take noise data over high-speed links
  - This will remove the shutter open/close effect
Readout Cross-talk

- Observing on the Readout board - PCIe40
- Arria10 transceivers running at 5 Gb/s
- When all input links are ON, header is locked and stable. PRBS from VeloPix is good on all links.

header found “high” on all 6 links in bank
Readout Cross-talk

- Link often falsely detected when off (directly from xcvr)
  - Effect of Arria10 (not FE)
  - Even header patterns are found (0101 every 128b)
  - We mitigate this by looking for header trains in firmware
- However, these “false headers” give us a means to look at cross-talk on the incoming links
- See a high frequency of false headers when neighbouring links are activated
- Extensive PRBS and other HS tests are essential as we scale up

<table>
<thead>
<tr>
<th>GWT Activity</th>
<th>Start</th>
<th>Stop</th>
<th>Off</th>
<th>On</th>
</tr>
</thead>
<tbody>
<tr>
<td>Start</td>
<td>Off</td>
<td>Off</td>
<td>On</td>
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<td>Off</td>
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</table>

2 links random false headers found

header found only when other links on
Bandwidth saturation tests

- Use test-pulses to test the bandwidth of the VeloPix
- Put a test-pulse in the top row of pixels every N clock cycles
- Allow it to traverse the full column height to the end-of-column readout
- For a single link, below N = 32, we should see loss.
- This also puts the chip into its maximal power consumption state
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Conclusion

• Velo Module Production underway
• Successful beam test in 2018
• Solved several problems in full readout tests under vacuum
• Continuous development of suite of standard tests
• Good performance of high speed links with full module control and readout chain
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- Continuous development of suite of standard tests
- Good performance of high speed links with full module control and readout chain
- Testing of Pablo’s thesis that Santiago is the greatest city in the world for seafood - confirmed at 90% CL. (Further study expected...)
Backup
• GBT
• GBT-SCA
• PCIe40