FELIX: commissioning the new detector interface for the ATLAS trigger and readout system

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Outline

• Introduction
• FELIX Board Production
• FELIX Firmware
• FELIX Server & Software
• Software ROD/ROS
• Integration Tests
• Performance Studies
• Summary & Outlook
Introduction
Introduction
Introduction

Current

Phase I & II

On Detector

Service Cavern

Custom Electronics

Commercial computers

Frontend Electronics (FE)

Front End environment monitoring

Custom links

Readout Drivers (ROD)

S-link

Readout System (ROS)

Ethernet

Higher Level Trigger (HLT) & Data Storage

Configuration Control Monitoring

Detector Control System (DCS)

CANBUS

Custom Electronics

Commercial computers

GBT

FULL

FrontEnd Link eXchange (FELIX)

TTC

Higher Level Trigger (HLT) & Data Storage

Ethernet

Software ROD/ROS

Configuration Control Monitoring

Detector Control System (DCS)
Move to more commercially available components sooner in readout chain

The custom readout drivers become software on commercial PCs (“data handlers” in Phase II)
Reduces number of custom links needed to transmit data and timing signal, configure & control detector.

GBT (Gigabit transceiver): GBTx ASIC aggregates slow electrical links (E-links) from front end ASICs into fast optical link. Includes error correction for high radiation environment.
FELIX is always running, doesn’t touch the data format, doesn’t know about the status of the detector (like a switch that routes different data types)
Introduction
FELIX Board Production

**FELIX Host**
- FELIX Host
- FELIX Card
- Optical Receiver
- Timing Card
- FPGA
- Memory Buffers for e-links
- PCIe Gen-3
- CPU
- FELIX core sw
- DMA
- Custom device driver
- Network Interface Card

**BNL 712:**
Kintex Ultrascale FPGA
PCIe Gen 3x16 lanes
8 minipods
- 24 **4.8G** GBTx links,
- 12 **9.6G** links at PCIe limit
48 links as a TTC distributor

**FLX-709 (VC 709):**
- 4 10 Gbps links (4 SFP+)
- Virtex-7 X690T FPGA
- PCIe Gen 3x8 lanes
FELIX Pre-series

• Validated pre-series production of 23 FLX-712
  • 2 thermal cycles at 85°C, xray check of soldering, check voltage values
  • FPGA, FLASH and microcontroller programming, eyescans ($< 10^{-9}$) and BER ($< 10^{-12}$), functionality tests, 8 hour loop back tests, slow control adapter tests, trigger & timing tests, BUSY tests, jitter tests
  • Thermal testing on 8 cards to test 5 year lifetime = 50 cycles – passed functionality tests
  • ALL CARDS PASSED TESTS

FELIX Mass production for Phase I

• Launching production of 120 cards. Production in Fall and installation by mid-December
**GBT Mode:** 24 bi-directional radiation-hard, GBT links (4.8Gb/s – 3.2Gb/s with error correction)

**FULL Mode:** 12 links, custom lightweight protocol from front-end-path (9.6Gb/s – 7.68Gb/s with 8b/10b)
### FELIX Firmware

#### Configuration Options

<table>
<thead>
<tr>
<th></th>
<th>FLX-709 # chans</th>
<th>FLX-712 # chans</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>GBT dynamic</strong></td>
<td>4</td>
<td>4+4</td>
</tr>
<tr>
<td>- All combos of elinks (2,4,8) and modes (8b/10b, HDLC)</td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>GBT semi-static</strong></td>
<td>--</td>
<td>12+12</td>
</tr>
<tr>
<td>- Static &amp; configurable links</td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>FULL</strong></td>
<td>4</td>
<td>12+12</td>
</tr>
<tr>
<td>- 6+6 channel matches maximum PCIe bandwidth (x16 Gen3). 12+12 channel is lower bandwidth</td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>LTDB mode</strong></td>
<td>--</td>
<td>24+24 (LTDB)</td>
</tr>
<tr>
<td>- Only clock distribution, trigger, slow control/monitor (to DCS)</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### Chunksize and Rate Table

<table>
<thead>
<tr>
<th>Name</th>
<th>Chunksize (worst case)</th>
<th>Rate per channel</th>
<th>Channels per FELIX (worst case)</th>
<th>Total Chunkrate per FELIX</th>
<th>Total Datarate per FELIX</th>
</tr>
</thead>
<tbody>
<tr>
<td>GBT-Mode</td>
<td>40 Byte</td>
<td>100 kHz</td>
<td>384</td>
<td>38.4 MHz</td>
<td>15 Gbps</td>
</tr>
<tr>
<td>FULL-Mode</td>
<td>4800 Byte</td>
<td>100 kHz</td>
<td>12</td>
<td>1.2 MHz</td>
<td>46 Gbps</td>
</tr>
</tbody>
</table>
### FELIX Server & Software

![Diagram of FELIX system architecture]

#### Component Specification

<table>
<thead>
<tr>
<th>Component</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>Motherboard</td>
<td>Supermicro X10SRW-F</td>
</tr>
<tr>
<td>CPU</td>
<td>Intel(R) Xeon(R) CPU E5-1660 v4, 8 cores @ 3.20GHz <em>Intel Xeon Gold 5118 CPU (if more perf needed)</em></td>
</tr>
<tr>
<td>Memory</td>
<td>32 GB (4x8GB DIMMs for full memory bandwidth)</td>
</tr>
<tr>
<td></td>
<td>48 GB (6x8GB DIMMs) (if more perf needed)</td>
</tr>
<tr>
<td>Network Cards</td>
<td>Dual-port 100/25 GbE Mellanox ConnectX-5 EN</td>
</tr>
</tbody>
</table>

*FELIX PC from Action (Poland) will be ordered soon*
FELIX Software

- Access to the FELIX hardware controlled via device drivers
- Low Level software: basic configuration/monitoring (electrical link configuration, felix-monitoring)
- Higher Level Software: data rate and channel monitoring
- Subscription to electrical links is made from SW ROD
Software ROD/ROS

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<tr>
<td>Motherboard</td>
<td>Supermicro X10SRW-F</td>
</tr>
<tr>
<td>CPU</td>
<td>Dual Intel(R) Gold 5218 CPU @ 2.30 GHz</td>
</tr>
<tr>
<td></td>
<td>(16 cores)</td>
</tr>
<tr>
<td>Memory</td>
<td>96 GB ECC REG DDR4-2666</td>
</tr>
<tr>
<td>Network Cards</td>
<td>Mellanox MT27700/MT27800</td>
</tr>
</tbody>
</table>

Validated specifications depending on user needs

GBT Mode CPU Utilisation

- 75% of resources used

CPU Usage (%)

<table>
<thead>
<tr>
<th>Data Reading &amp; Aggregating</th>
<th>Custom Processing Simulation</th>
<th>HLT Request Handling</th>
</tr>
</thead>
<tbody>
<tr>
<td>TCP/IP</td>
<td>RDMA</td>
<td>Netio</td>
</tr>
</tbody>
</table>
Integration Tests

• Integration of all supporting systems in Laboratory with emulated FULL and GBT mode data

• Commissioning with different input of trigger & timing & testing back pressure
Integration Tests
Performance studies

- Measured FELIX performance (including FPGA temperature) under demanding operating conditions. Realistic traffic patterns (random trigger at different average rates, variable data size) were used.
Performance Studies

FELIX taking data in ProtoDUNE

ProtoDUNE uses FULL-mode FELIX. Firmware modified to support jumbo-blocks (4kB instead of 1kB). Up to 6 consecutive chunks of 464 Byte are merged, chunksize is 2784 Byte at a rate of 333 kHz.

Other experiments also considering FELIX
Summary & Outlook

• 23 pre-series FELIX board passed tests

• Firmware and software being finalized to user specifications

• FELIX shows good performance in lab tests as well as ProtoDUNE

• 120 FELIX boards with FELIX and SW ROD servers to be ordered soon and arrive in the fall for 2020 installation