The ATLAS Pixel Detector Upgrade at the High-Luminosity LHC

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• The Phase-2 Upgrade of the LHC
  → Requirements for the ATLAS Inner Tracker (ITk)
• The ITk pixel detector:
  – Layout
  – Sensors, FE chips, and Modules
  – Support Structures and Cooling
  – Electrical Services / Data Transmission
• Current Status and Near-Future Goals
• Summary
The LHC and ATLAS

Large Hadron Collider at CERN:
- 27km circumference
- protons and heavy ions
- 4 experiments

ATLAS:
- Layered multi-purpose detector: tracking, calorimetry, muon detection
“Phase-II” upgrade of ATLAS in ~2025. Upgraded tracker will need to cope with
- average 200 interactions per bunch crossing
  - Currently ~37
- x5 pileup
- x10 integrated luminosity → x10 radiation damage

much higher data rates and occupancies
The New Inner Tracker

- All-silicon
- Coverage up to $|\eta| < 4$
  - $\geq 13$ hits / track (barrel)
  - $\geq 9$ hits / track (forward)

Requirements for ITk pixel detector:

- Radiation hardness up to
  - $10$ MGy (TID)
  - $2 \times 10^{16} \, n_{eq}/cm^2$
- Track reconstruction efficiency
  - $> 99\%$ for muons
  - $> 85\%$ for electrons and pions
- Fake rate $< 10^{-5}$
- Occupancy $< 1\%$
- Robust against loss of $15\%$ of channels
- Readout rate 1-4 MHz
- Output bandwidth up to $5.12$ Gb/s per front-end chip
- Material budget $\sim 1.5$-2.0$\%$X0 per layer
Sensor choice is region-dependent:
- Innermost layer (“Layer 0”): 3D silicon
  - Higher radiation tolerance
  - Lower power consumption → easier servicing
  - Pixel size 50x50 \( \mu \text{m}^2 \) or 25x150 \( \mu \text{m}^2 \)
- Layer 1:
  - 100\( \mu \text{m} \) thick planar Si
  - Pixel size 50x50 \( \mu \text{m}^2 \) or 25x150 \( \mu \text{m}^2 \)
- Layers 2-4: 150\( \mu \text{m} \) thick planar Si, 50x50 \( \mu \text{m}^2 \) pixels
- Innermost two layers will be replaced at half-lifetime (~2000 fb\(^{-1}\))
The Front-End Chip

- Being developed by the RD53 collaboration
  - Joint ATLAS-CMS effort
    - Rad-hard chip design, software and prototypes
  - 65nm technology
  - Final chip will be
    - 400 x 384 (153,600) 50x50 µm$^2$ pixels
    - 2.0 x 2.1 cm$^2$
  - Trigger frequency up to 4 MHz
  - Shunt-LDO regulator for serial powering
- “RD53A” prototypes being tested:
  - Half size
  - Missing some features needed in production chips → RD53B
- RD53A-based ATLAS-pixel system tests planned for early 2020
  - On realistic local support structures

Hybrid Modules

- 1 or 4 FE chips bump-bonded to sensor
  - Single-chip modules in L0
  - “Quads” elsewhere (pictured above right)
  - Striving for a common design for layers 2-4:
    - envelope is defined that works for all subsystem geometries
- Cu-Kapton flex hybrid glued to sensor
  - Provides connection to power, slow controls and data distribution
  - Wire bonds to ASIC
    - Encapsulated as baseline
  - “pigtails” will be subsystem-specific
- Serially-powered to reduce cable mass
  - Up to 14 modules in a single power chain
  - Up to 7A per module
Support Structures

- Support structures are specialized by region:
- All structures are made of carbon-based materials...
  - Low mass, high stability, high thermal conductivity
- …and cooled by evaporative CO$_2$ in thin-walled Ti pipes
• Modules are glued to TPG tiles, which are then attached to supporting structures with integrated cooling pipes:
  – In the central (low-\(\eta\)) region modules are “flat”, on lightweight open structures called “longerons”; adjacent rows of modules overlap in \(\phi\)
  – In the mid-\(\eta\) region, novel inclined-module layout keeps modules ~normal to high-\(p_t\) tracks
  – Services (cooling and electrical) run along the longerons and the ring-support cylinder
Outer Endcap Supports

- Single rows of modules on half-rings ⊥ to beampipe:
  - 3 layers of half-rings loaded into half-cylinders
  - Rings are strategically placed in z to provide hermeticity in η
- Half-rings are C-foam / C-fibre “sandwiches” with embedded cooling pipe
- Cooling feed and exhaust lines, and electrical cables, run between outer rims of rings and inner surface of cylinder
The inner system will be contained inside an Inner Support Tube and will be replaced once (at ~2000 fb⁻¹)
- Short 2-layer flat barrel + long section of rings (3 types)
- Cooling feed/exhaust and cables run along the quarter shell
Electrical Services
(power, data, monitoring)

• Local supports hold “PP0”s with connections to modules
• “Type-I” cables carry services into / out of the detector
  – Twisted pairs for power and monitoring/interlocks
  – Data is on twin-ax cables inside the detector with electrical-to-optical conversion outside
    • Accessible, lower radiation
  – Extremely challenging to fit everything in the limited space (next slide)
• Successive steps of patch panels, thicker cables … up to services caverns

Outer-Endcap Type-0 are on the half-ring:
  • Bus tape
  • “EoS” card (PP0)
Type-I services (cooling pipes and cables) must fit between layers in very constrained spaces.

- Exacerbated by large number of data twin-ax cables
  - Each FE chip needs up to four 1.28 Gb/s output lines
  - No on-module aggregation
- Challenging!
  - Exploring ways to reduce number of cables e.g. RD53 uplink sharing
  - Also re-examining services engineering schemes

Inner system: services are routed in 5 types of cable trays around $\phi$. Preliminary CAD suggests it will fit.

Outer Endcaps: services are routed between half-rings and supporting cylinder. Most congested region is at highest-z Layer-2 ring: fits.

Outer Barrel: most problematic area is the end of the inclined units.
PP0 + Type-0 services from inclined unit, + Type-1 Services from flat section.
Work in progress.
Most activities are in mid-to-late R&D phase:

- Lots of ongoing work with prototypes:
  - Testbeams
  - Irradiation campaigns
  - Thermo-mechanical and electrical testing of supports and services
- Finalization of procurement and production procedures, quality assurance and quality control

- Modules, Services and Global Supports are preparing for Preliminary Design Reviews
- Sensors, FE chips, Local Supports are preparing for Final Design Reviews
- Some market surveys ongoing
The LHC → HL-LHC upgrade requires a new tracker (ITk) for ATLAS, with tough requirements.

Features of the ITk pixel detector:
- 5 layer coverage to $|\eta| < 4$
- New FE chip (RD53) and sensor (3D, planar) development
- serially-powered
- CO$_2$ cooled

Main challenges: Space and Time!

Most aspects currently preparing for Design Reviews
- Pre-production to follow