R&D Proposal
A demonstrator analog signal processing circuit in a radiation hard SOI-CMOS technology

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Abstract

It is proposed to develop a demonstrator integrated circuit for particle detector analog signal processing using the advanced 1.2 μm HSOI3-HD Silicon - On - Insulator (SOI) CMOS radiation hard technology of Thomson-TMS, which has become recently accessible for selected civilian applications. The characteristics announced for this process promise survivability after a total dose in excess of 10 Mrad (SiO₂) and 10¹⁴ to 10¹⁵ n cm⁻², which is probably satisfactory for applications in LHC detector systems. The properties of such a SOI process look promising, in particular regarding speed. In view of the special analog requirements in the particle physics environment one should verify the analog characteristics before and after irradiation by producing a demonstrator signal processing circuit which incorporates the most vital functional blocks. This demonstrator would consist of a low noise front-end amplifier, a comparator and an analog pipeline element with associated logic, following the scheme of the Hierarchical Analog Readout Pipelined Processor HARP, which has been developed in the framework of the CERN-LAA detector R&D project.

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1. Introduction.

It is obvious that specific, radiation hard electronics must be developed for those LHC particle detectors that are exposed to ionizing radiation and neutrons[1]. This concerns all equipment along the beam pipe, inside the central cavity and also electronics that might be positioned inside the calorimeter.

Several radiation tolerant and radiation hardened silicon integrated circuit technologies have been developed for military purposes, in the USA as well as in Europe. Only few of those have been accessible to civil applications. The SOS (Silicon - On - Saphire) technologies of ABB-HAFO and of Marconi are currently being investigated by experimental particle physics groups in Stockholm (T. Ekelöf, in collaboration with the LAA project [2]) respectively the Rutherford Appleton Laboratory (P. Sharp). The more recently developed SOI (Silicon - On - Insulator) technology [3] of Thomson Militaire et Spatiale (TMS) in Grenoble has been made accessible for selected civil applications only a few months ago.

Before decisions can be made on comprehensive prototype developments it is mandatory to implement in several of the available technologies a demonstrator chip with the vital elements for the circuits needed in the LHC environment, in order to evaluate the characteristics of the respective technologies. In this stage of the LHC preparation the cost and effort of such preliminary, parallel studies are minor compared to the overall development cost of the complicated electronic systems ultimately needed. Such preliminary studies will enable a well-founded choice of the manufacturing processes to be used in the next stage of electronics subsystem prototype development, while they can provide at the same time a very practical education of the particle physics community in the handling of the radiation hardness problems.

The HSOI3-HD process of TMS uses transistors with effective gate length of 1.2 μm and a special channel-stopped transistor structure, which eliminates essentially the lateral MOS leakage current. The characteristics announced for this process promise sufficiently high speed for the LHC and survival after a total dose in excess of 10 Mrad (SiO2) and $10^{14}$ to $10^{15}$ n cm$^{-2}$. A practical advantage of the TMS-SOI process lies in the fact that the design philosophy is similar to what is used in the standard CMOS processes. Therefore, it follows more easily the approach of designs in the 1.5 μm CMOS process of MIETEC N.V. that we have been using so far in the LAA R&D effort for the development of the HARP functional building blocks. Also the readout system for the tracker-preshower detector prototype [4] is currently designed in this 1.5 μm technology.

For the time being it is assumed that one or several of the mature rad-hard technologies will offer adequate analog capability, even though these technologies may have been intended primarily for digital circuits. This assumption may prove too optimistic, and it is certainly advisable already at this stage to explore in parallel some alternatives to the first order approach with existing rad-hard CMOS. Fortunately, research in this domain is conducted at BNL, aiming at JFET technology [5] for better noise performance. In addition a project [6] is under way to extend the SOI process with bipolar and JFET devices, involving a collaboration between CEN Saclay and LETI/CEA DAM.

2. Overview and milestones of the project.

The aim of the project is to produce a demonstrator circuit which comprises a number of vital functions to be used in the high radiation regions of a future high luminosity LHC detector. This demonstrator should show the feasibility of high speed analog and digital functions in the SOI technology and it should allow to measure the degradation of a device under the irradiation conditions expected in LHC.

The project is planned to be executed in several phases as is shown in table 1. The first and second phase should proceed within somewhat more than one year, and these phases are the subject of this R&D proposal. The first phase allows for engineering samples of the HSOI3-HD technology to be provided by TMS, characterization of these to be made by CERN in collaboration with TMS engineers and the feasibility parameters for a demonstrator circuit to be established. An essential aspect of this phase 1 is the development of a simulation model which represents the analog characteristics of this particular technology. Such a model is used subsequently for the analog circuit simulation work in phase 2.

Assuming that the feasibility study in phase 1 concludes with positive results, the second phase will then consist in the elaboration of the design of a demonstrator with an area of about 10 mm$^2$.
and the manufacturing of a small number of circuits. TMS will assist in the evaluation of these circuits.

Which functions exactly are to be implemented on the demonstrator chip can be decided only after the feasibility study, phase 1 of the project. It is our intention to include a low noise front-end amplifier, an analog pipeline element of the type already developed in the framework of the LAA project, a fast comparator and associated fast logic circuits for triggered data selection. Even though a 1.2 μm SOI-CMOS process allows high packing density, one may not expect the allowed area to be sufficient to realize a complete, multi-channel prototype. This would be the subject of the phase 3 if the demonstrator functions satisfactorily.

The timescale foresees 5 to 6 months for phase 1 and 9 - 12 months for phase 2, of which 5 months for the circuit manufacturing. The cost for these 2 phases specified in the formal contract proposition by Thomson TMS is FF 927 043 HT, subject to indexation. Consultancy from specialist third parties, inasmuch as allowed by the contract, is planned to be used, in particular for some of the noise evaluations and the radiation measurements. To cover the cost related to consultancy and external radiation testing, for travel expenses and for laboratory equipment an additional sum of 30 kSF is needed, which results in a total budget for 1991 of 290 kSF.

3. Documentation.

In fig.1 the principle of the basic SIMOX process for SOI wafer production is illustrated. In figs.2 and 3 SOI/CMOS is compared to bulk CMOS and SOS/CMOS. In figs. 4a and 4b the \( I_d - V_{gs} \) curves are shown for n channel resp. p channel transistors, for irradiation up to 20 Mrad(Si).

In figs 5a and 5b the threshold shifts for the front gate oxide, resp. the back gate oxide are given. It can be seen that only well beyond 10 Mrad appreciable changes occur. These graphs have been taken from a paper by J.L. Leray et al. of CEA, which has been submitted for publication in IEEE Trans. Nucl. Sc. (1990)[7].

The contract proposition by Thomson TMS and the related correspondence are appended to the original copy of this R&D proposal, but are not available for open distribution in view of commercial details.

4. Coordination with other research in rad-hard electronics.

Various initiatives for evaluation of rad-hard technologies have been mentioned before, namely those currently supported in Stockholm, in the Rutherford-Appleton Laboratory, in CEN-Saclay and in Brookhaven National Laboratory. A number of other efforts are being undertaken in the USA. Apart from the JFET development in BNL, all other US groups seem to use hardened bulk CMOS processes from various sources, e.g. UTMC, but as yet not from the main military contractors. The RICMOS process from Honeywell has been mentioned as an appropriate possible choice[8]. Contacts have been laid with the Sandia Laboratory, but to our knowledge no circuits have been made yet. In the USA no rad-hard SOI process is currently available for civil applications.

We keep close contact with these other research groups and it is our intention to exchange the conclusions of the technology evaluation inasmuch as this is compatible with the contractual and commercial confidentiality. It may also be useful to try to exchange some of the designs to be implemented on demonstrator circuits. However, the many differences between technologies render a full redesign practically obligatory in each case. Without such a redesign the performance of the circuit will certainly not be optimal, and this could obscure the real characteristics of the technology.
References

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PROPOSITIONS DE COLLABORATION

PHASE 1 : FAISABILITE (5 à 6 mois)
- Documentation
- Livraison d'échantillons
- Interprétation des résultats

PHASE 2 : DEMONSTRATEURS (9 à 12 mois)
- Définition et conception
- Fabrication et livraison des démonstrateurs
- Interprétation des résultats

PHASE 3 : PRODUITS POUR LHC (18 à 24 mois)
- Définition et conception
- Fabrication et livraison des premiers prototypes
- Évaluation des prototypes
- Reprise de la conception
- Validation des produits

PHASE 4 : INDUSTRIALISATION ET QUALIFICATION (= 6 mois)
- Industrialisation
- Qualification suivant normes CERN
- Début production
THE SIMOX MATERIAL

PRINCIPLE:

1) IMPLANTATION

- Dose $1-2 \times 10^{15}$
- Energy 200 Kev
- Implantation temperature 500°C - 700°C

MONOCRSTALLINE SILICON SUBSTRATE

2) ANNEAL

HIGH TEMPERATURE ANNEALING 1300°C - 1500°C

MONOCRSTALLINE SILICON

AN INSULATING BURIED LAYER IS FORMED BY OXYGEN ION IMPLANTATION AT HIGH DOSE IN SILICON WAFER

PROCESS ADVANTAGES:

- EASIEST PROCESS
- THE FULL WAFER IS FREE OF DEFECTS
- GOOD FLATNESS
- GOOD SI/SIO2 INTERFACE

REMARK: HIGH CURRENT OXYGEN IMPLANTES ARE NOW AVAILABLE

THOMSON COMPOSANTS MILITAIRES ET SPATIAUX DT 07 JUNE 1988

Fig.1
ADVANTAGES OF SOI/CMOS COMPARED TO BULK CMOS

- Higher speed
- Lower dynamic power consumption
- Higher packing density
- Higher tolerance to ionizing radiations
- Simpler fabrication process
- "Latch up" free

ELECTRICAL PERFORMANCES
(DESIGN RULES ASSUMED TO BE EQUIVALENT)

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<th>Substrate/Well Capacitance</th>
<th>Interconnect Capacitance</th>
<th>Carrier Mobility</th>
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*** Good
** Medium
* Poor
Fig. 5a

Front gate - correlated mode

Co60 - 1 krad(SiO2)/s

Irradiation bias: VgN +5V, VgP -5V

Fig. 5b

Back gate - correlated mode

Co60 - 1 krad(SiO2)/s

Irradiation bias: VBN 0V, VBP -5V

lot-to-lot variation