CIRCUITRY FOR COMPUTER CONTROL
OF FAST ELECTRONICS MODULES BY CAMAC

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With the present increase in the number of recording channels and the introduction of small computers, there is a growing trend towards the use of digitally controlled fast electronic modules in physics experiments /1-3/. The system of fast electronic modules developed at the JINR High-Energy Laboratory /4,5/ can be controlled electronically. An analog signal regulates the trigger thresholds, the length of the output signals and the modules' transmission coefficients. There are also special logic inputs for switching the circuits. The CAMAC modules are of double width and have room (for a second print-out unit) for a control digital-analog converter connected to the CAMAC dataway.

This report describes a special circuit designed to control the parameters of fast electronic modules. The circuit consists of four independent control channels. Each channel includes a digital-analog converter and an interlock flip-flop to store the control circuit's switching signal. Since an accuracy of 1 - 1.5% is sufficient for the control of the fast modules' parameters, the digital-analog converters each contain six binary bits. The converters do not have to operate very quickly because data have to be taken over a sufficiently long period at each point. In the case of single processes, one factor which limits the need for a fast response is the delay in the control-computer link interface which amounts to 10-15 µsec under optimum conditions.

A block diagram of the device is shown in fig. 1. In order to reduce the size and complexity of the device compared with earlier designs /6/, the digital-analog converters are based on the principle of the cyclic addition of six successive time intervals (fig. 2) of differing length. The circuit consists of a common pulse generator with a 25 nsec. period and a mark-space ratio of 2. A 5-bit binary synchronous counter is used to double the length of the periods. A system of "AND" circuits is used to select successive time intervals /A-F, fig. 2/, each twice the length of the last. Each of the four channels has OR circuits for selecting these intervals in accordance with the data recorded in the state registers (fig. 1 shows the registers for the first channel). The data are fed into the registers from the CAMAC data-
way along bus bars W1 - W6 and a check output is possible via bus bars R1 - R6. The selected time intervals are summed up along the "OR" conducting wire (fig. 2 shows the result for the code 101101). The "OR" circuit's cycle is determined by the period of the counter's most significant bit and is 0.8 \( \mu \text{sec} \). A series of pulses with this period and a controlled mark-space ratio is transmitted to a current gate (T3, T4) and then to a smoothing integrating circuit and level converter (T1, T2). The converter's output signal varies from -6V to 0. The integration constant is selected so that the noise at the output does not exceed one quarter of the channel width. In this case, the fall time of the output pulse is 8 \( \mu \text{sec} \). Fig. 3 shows the linearity plot of one of the converter's channels.

States are recorded in the flip-flops via bus bar W7 and are read out via bus-bar R7.

The generator, synchronous counter and interval separation circuits consist of integrated circuits; the state registers and CAMAC function decoder are made from TTL integrated circuits.
Characteristics in brief

The circuit consists of four independent control channels with subaddresses A(0) - A(3). Both ones and zeros are recorded in the state registers via busbars W.

Converters:

- Number of gradations: $2^6$
- Range of output levels: from $-6V$ to $0V$
- Permissible load resistance: not less than $750 \, \text{ohm}$
- Speed of response: not worse than $10 \, \mu\text{sec}$.
- Instability of output level setting: not more than $\pm 20 \, \text{mV}$
- Temperature drift of output level: not more than $0.7 \, \text{mV/°C}$
- Position for digital control: $W7 = 1$ - control circuit switched on

CAMAC functions

- $F(17)$ - record in state registers ($W_i = 1$ - record "1")
- $F(1)$ - read from state registers
- $Z$ - initialize
- $C$ - clear
- $Q$ - $Q$ - response

Circuit's power consumption

- $+24V$ - $90 \, \text{mA}$
- $-24V$ - $120 \, \text{mA}$
- $+6V$ - $350 \, \text{mA}$
- $-6V$ - $800 \, \text{mA}$.
This circuit may be used as a separate digital-analog converter. This type of circuitry is also convenient for constructing precision converters, since the time interval components are very accurately defined.

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Bibliography


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Fig. 1 Block diagram of digital-analog converter.
Fig. 2 Time diagram of digital-analog converter's cycle.
Fig. 3 Linearity plot for digital-analog converter.