Addendum to the CMS ECAL Technical Design Report

Changes to the CMS ECAL Electronics

1. Introduction

This addendum describes the changes to the ECAL electronics chain. The background to the changes has been given in a previous submission numbered CERN LHCC 2002-18.

The basic change has been to move upstream the trigger primitive generation (TPG) from the ‘off-detector’ ULR electronics onto the detector. This implies that the digitised data are read out only upon a Level-1 accept. This decreases the number of data links and the quantity of the off-detector electronics by a factor ~ 8 as well as reducing the overall complexity. The schematic of this new chain is shown in Fig 1.

The TPG and data storage on the detector will be implemented in a new 0.25μm CMOS chip, building on the experience gained in the CMS Tracker and Pre-shower projects. In addition, the revised ECAL system will use the data link technology and clock and control system developed for the CMS Tracker project. The estimated cost of the new electronics system is less than the cost ceiling of 36 MCHF, and includes contingency.

During the recent 2002 test beam campaign good data have been taken with the previous electronics chain albeit with a noisy FPPA. One hundred channels were equipped in module M0’. The chain consisted of APDs, FPPAs, AD9042 ADCs, Glink serializer, Spinner digital optical links and the ‘Rose’ Upper Level Readout boards. Furthermore final prototypes of the APD power supplies were used. The whole chain was operated successfully over two months. Much of the functionality of the ECAL electronics chain has therefore been tested.

2. The Proposed System

The proposed system (Fig. 1) takes advantage of the radiation hardness of 0.25μm CMOS technology that has been demonstrated in the CMS Tracker project. This allows the TPG, storage and clock and control functions to be performed on the detector. This concept is not new and had been considered earlier in the development of the ECAL project but not adopted due to the lack of proven, low cost radiation hard electronics technology.
Figure 1. Schematic of the front-end electronics

The Very Front-end Electronics (VFE) is reduced to an FPPA and ADC chip per crystal, and a new digital electronics board containing the Front-end Electronics (FE). On the FE board (Fig. 2) a new 0.25µm CMOS chip (FENIX) reads out a block of 5 crystals. The FENIX chip performs two functions, the storage of data until the receipt of a level 1 trigger accept, and the correction of pulse heights and summing of energy from 5 channels.

Every FE board has 5 FENIX chips to read out 25 crystals. In the ECAL Barrel, a trigger tower consists of the same 25 crystals and the output of the 5 FENIX chips is filtered by a sixth FENIX chip to provide the trigger tower energy and the fine grain bit described in the CMS trigger TDR. The trigger data is transmitted to the off-detector Trigger Concentrator Cards (TCC) by a GOL (Gigabit Optical Link) chip and trigger data digital serial link operating at 800Mb/sec. On receipt of the Level-1 trigger accept, the data for the triggered event that is stored in the memory of the 5 FENIX chips is transmitted to the off-detector Data Concentrator Cards (DCC) by a GOL chip under the control of a seventh FENIX chip and the DAQ digital serial link operating at 800 Mb/sec.

The functionality of the proposed system is exactly the same as the original system.

In the ECAL End-caps the trigger tower geometry is more complex since the trigger tower boundaries do not match the boundaries of the 25 crystal ‘Super-Crystals. In the present system only the partial sums from at most 5 crystals are performed on the detector and hence there will be more trigger data links on each of the FE boards. On average there are 10 crystals per trigger tower in the ECAL End-caps.
The proposed system (Barrel and End-caps) will have ~ 3000 DAQ data links, ~ 6500 Trigger links and ~ 3000 Clock and Control links compared to > 91000 links in the original system. There will be ~ 50 DCC boards, ~ 120 TCC boards and ~ 50 Front-end Control (CCS) boards compared to > 800 boards in the original system.

The FE board will also contain radiation hard voltage regulators (developed by RD 49) to provide local control of the LV supply. This will allow the ECAL project to benefit from the common CMS LV power supply system that transmits power to the detector at 400V AC. This will reduce the number of cables require from the control room to the periphery of the detector from ~ 1400 to ~ 10 with a corresponding reduction in cost, installation time and power dissipation.

The power dissipated in the detector has been reduced from ~ 2.3W / crystal to ~ 2W / crystal because although the voltage regulators dissipate a lot of power, the number of optical data links has been reduced by a factor of ~8.

![Diagram of the arrangement of the Front-end electronics into VFE and FE boards](image)

**Figure 2. The arrangement of the Front-end electronics into VFE and FE boards**
3 Project Management and Overall Project Plan

3.1 Project Management

Although the Front-End electronics is more complex than in the original design, the overall system will be much easier to implement because of the enormous reduction in the number of optical links and the simplification of the upper level readout. Nevertheless, the time available for undertaking this major redesign is very short. Thus there is a substantial risk to the project if significant delays are incurred. A late arrival of the electronics, combined with the unavailability of the SPS test beams in 2005, could jeopardise the program of pre-calibration of super-modules before their installation. Progress will therefore be closely monitored.

A formal project management structure has been implemented. A schematic is shown in Fig. 3. The Project has been partitioned into seven sub-projects each with a project manager and deputies. The Electronics Coordinator reports to the ECAL Project Manager and is assisted by an Advisory Group and a Project and Q/A Management Group. The Advisory group contains 8 persons including electronics experts from other CMS sub-detectors and members of the electron/photon physics group. The second group is led by S. Quinton from RAL who is an acknowledged expert in QA issues. The proposed system has been reviewed and has passed the ‘feasibility study’ phase, which delivered a detailed specification of the complete system, a detailed project plan, a complete staffing plan and the spend profile required to deliver the project plan.

The sub-projects are:
- Front-end Electronics
- Data Links
- Off-Detector Electronics
- Electronics Integration and Commissioning
- Power Systems
- Slow Controls
- Pre-shower Integration

The status of each of these sub-projects is considered in turn.

3.2 The Overall Project Plan

The detailed project plan is shown in figure 4. The major Level-2 milestones, common to all of the ECAL Electronics are:

- Electronics Systems Review of the Barrel ECAL Electronics system Sept 2003
- EB Off-detector electronics ESR Jan 2004
- FE Electronics delivered and tested for 12 Supermodules Apr 2004
- EB Front-End Electronics Production Complete Dec 2004
- EB Off-detector Electronics Complete Aug 2005
Electronics Systems Review of the End-Cap ECAL Electronics system  
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EE Off-detector electronics ESR  
EE Off-detector electronics production complete

Figure 3 : Project Management
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Figure 4b. ECAL Electronics Schedule (Production Phase)
4. The Front-end Electronics System.

4.1 Introduction

The feasibility study concluded that the front-end electronics system proposed by the review would meet the required performance.

The Very Front-End (VFE) board containing five FPPA (Floating Point PreAmplifier) chips and five ADCs (AD 9042), receives input signals from a row of five ‘capsules’ (each capsule has two APDs in parallel), and feeds the digitized outputs to a Front-end (FE) board (Figure 2). The FE board contains seven FENIX chips, which provide three functions within a single chip. The data from a row of five crystals are stored until required by a Level-1 Trigger accept (L1 accept), the pulse shape data from a row of five crystals are corrected and summed to produce a strip energy, and finally the sum of all strip energies is summed to produce the energy deposited in the trigger tower (25 crystals) and the fine grain bit as described in the CMS Trigger TDR.

The trigger data is transmitted to the off-Detector electronics through a serial digital data link consisting of a GOL serializer chip, a link system based on the CMS Tracker link technology, a digital receiver module and a deserializer.

Each of the links is operated at 800 Mb/s, which is sufficient to complete the transfer of trigger data every 25ns. On receipt of a L1 trigger accept, the data from the triggered event, that is stored in the memory of the five FENIX chips is transmitted to the Off-detector electronics through a separate serial data link also operated at 800 Mb/s. For every L1 accept, ten time slices of data are transmitted off-detector in 7.5 μsec.

The front-end electronics will be controlled by the CMS Tracker clock and control system. This system uses a 40MHz digital optical link system, controlled from the off-detector Front-end Control (CCS) boards, to distribute the control information to the FE board.

4.2 Status of the Front-end electronics system

- The Front-end electronics system has been specified.
- The final design review of the FPPA was successfully completed in June and the chip has been submitted for fabrication with the expectation that it will be returned at the end of November 2002.
- The AD 9042 ADC will be procured as soon as the FPPA has been successfully tested.
- The VHDL code that describes the required functionality of the FENIX chips has been completed and transferred to RAL who have started the design of the ASIC version of the FENIX chip which will be submitted for fabrication in December 2002.
- The design of the FPGA version of the FENIX chip has been completed and the FE board design that will support both versions of the FENIX chips has been completed by RAL. Fabrication of the FE board will be complete in October 2002.
The GOL chip is available in prototype quantities, the design of the Opto-Hybrid that houses the laser diodes has started and the Opto-Hybrid connector pin-out has been agreed between all parties.

The Front-end electronics for the ECAL End-cap will be identical with the ECAL Barrel with the exception of the number of trigger data links and an FPPA chip adapted to meet the requirements of reading out the VPTs used in the End-caps.

### 4.3 Project Plan

The original schedule produced for the Review continues to be realistic. The final design review of the FPPA was delayed in order to improve the noise performance of the amplifier and the bandwidth of the output stage. The chip has been much improved as a result of the delay. The schedule for the procurement of the ADCs will also be delayed, but will not impact upon the overall schedule. The major milestones for the front-end electronics are:

- **Final Design Review of FENIX ASIC**
- **400 Electronics Channels Test (FPGA)**
- **400 Final Electronics Channels Test (ASIC)**
- **EE Supercrystals Tested in Beam with EB-FPPA**

<table>
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<th>Task</th>
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<tr>
<td>Final Design Review of FENIX ASIC</td>
<td>Nov 2002</td>
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<tr>
<td>400 Electronics Channels Test (FPGA)</td>
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<td>400 Final Electronics Channels Test (ASIC)</td>
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<td>EE Supercrystals Tested in Beam with EB-FPPA</td>
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### 4.4 Staffing Plan

The team involved in the feasibility study of the front-end electronics (CERN, IC, LBL, LLR-Ecole Polytechnique, Lyon, Minnesota, RAL, ETHZ) will continue to be involved in the detailed design, prototyping and system test phases of the project.

- The detailed plans for the testing of the FPPA chips are under discussion, and will be the responsibility of the US groups. The process will deliver 5000 working chips each month.
- The University of Minnesota will perform the radiation qualification of batches of ADCs and the delivery rate from the manufacturers will be 7500 working chips each month.
- The VFE board will be designed by ETHZ and fabricated in industry.
- Test of completed VFE boards will be performed by five regional test centres. The first test centres will be established at Lyon and by ETHZ working at CERN, who will establish the techniques required for testing the prototype boards. Discussions to establish a test center at Torino and two other centres are continuing.
- The testing of the FE electronics board will be done at LLR. Discussions to establish test centres elsewhere are continuing. Each board test centre will need to maintain a testing rate of 15 boards a day.
4.5 Contingency Plans

Although there is every reason to believe, after the successful review in June 2002, that the submitted FPPA will meet to the required performance specification, this very demanding analogue electronics still represents the largest risk to the ECAL project. Contingency plans have therefore been approved to develop a backup 0.25µ CMOS amplifier and a low power 40Mhz, 12 bit ADC. Both designs will be ready for fabrication in December 2002 and available for testing in March 2003. The ADC development is done by a specialist commercial firm and will not interfere negatively with the baseline program. If successful, a VFE system in 0.25µ technology could be tested in Q2 2003.

5. The Data Link System.

5.1 Introduction

The feasibility study concluded that the Data Link system proposed by the review would meet the required performance.

The ECAL serial digital data links will be based on the technology developed for the CMS Tracker analogue links. The technology has been carefully qualified for operation in the Tracker environment that is more hostile than that found in the ECAL. The system is shown in figure 5. The system consists of a data serializer and laser driver chip, the GOL, a laser diode with attached fibre pigtail, a system of fibres and fibre interconnections and a receiver module. The data transfer from the super module/Dee to the off-detector electronics takes place on ruggedized trunk cables containing 8 * 12 way fibre ribbons. The laser diode, the fibres, all the interconnection system and the ruggedized cable are identical to those used for the Tracker links. Therefore only the opto-hybrids and the receiver module have to be developed specifically for the ECAL.

**Optical Links: Architecture**

*Figure 5  ECAL Data Link Architecture*
5.2 Status of the Data Link System

Prototype link systems have been tested at both 800 Mb/s and 1600 Mb/s using combinations of commercial components, which will approach the final system with time. The first tests used a GOL and laser diode mounted on an evaluation board driving a realistic fibre system into a Paroli receiver and Glink Deserializer. The second test replaced the Paroli receiver with an 8 channel NGK receiver module which is very similar to the final 12 channel NGK receiver.

In these tests 'eye diagrams' at 800 Mb/s, shown in figure 6, were observed. Similar 'eye diagrams' at 1600 Mb/s also show a good open diagram with a large stable region.

![Eye diagram for the ECAL Link system at 800 Mb/s](image)

**Figure 6** Eye diagram for the ECAL Link system at 800 Mb/s

Tests with the 8-channel NGK receiver have made good progress and are an invaluable aid to the understanding the problems involved in constructing a large system. The 12-channel NGK receiver is expected in September when tests will continue with the deserializer chips under evaluation. Full readout chain tests will begin in January 2003 in preparation for the system tests with the 400 channel Electronics Test in Mar. 2003.

A detailed specification of the data link system has been completed.

5.3 Project Plan

The project plan presented to the review continues to be realistic. The detailed plan is shown in figure 4. The major milestones for this project are:
5.4 Staffing Plan

The ECAL Data Link project builds on the successful development work completed for the CMS Tracker. The Tracker Link Group has been very helpful in integrating the Group from the University of Minnesota. This collaboration has very quickly demonstrated that the data links work in the ECAL configuration.

The Minnesota group has taken full responsibility for the development, procurement and testing of the ECAL Data Links.

6. Off-Detector Electronics System.

6.1 Introduction

The feasibility study concluded that the off-detector electronics system proposed by the review would meet the required performance with small changes to the architecture.

The architecture of the Off-detector electronics system is shown in figure 7.

Figure 7. The Architecture of the Off-Detector Electronics system
The Trigger data and the DAQ data are transmitted from the FE board in the front-end electronics system to the TCC (Trigger Concentrator Card) board and the DCC (Data Concentrator Card) board by independent serial data links.

- Synchronized trigger data is transmitted to the regional trigger system in the case of the ECAL Barrel. In the case of the ECAL End-caps, the strip sums transmitted from the front-end systems are summed into trigger tower energy sums on the TCC boards.
- The DCC receives data from the FE and reduces the volume of data transmitted to the DAQ system by using information from the TCC board.
- This trigger information from the TCC board is processed in the Selective Readout Processor (SRP) board which in turn transmits information to the DCC board in order to reduce the volume of data sent to the DAQ system.
- The control of the Front-end system and the synchronization of the Off-Detector electronics is performed by the CCS board. This module is based on the Tracker FEC board and ECAL will benefit from both the hardware and software development from the Tracker project.

6.2 Status of the Off-Detector Electronics System.

The team working on the off-detector electronics has previously developed the algorithms and prototype systems for the earlier architecture. The system shown in figure 7 has now been accepted and the partitioning of responsibilities has also been agreed. The algorithms are well developed and detailed design has started.

6.3 Project plan

The project plan presented to the review continues to be realistic. The detailed plan is shown in figure 4. The major milestones for this project are:

Pre-series system ready for the beam tests July 2003

6.4 Staffing Plan

The team involved in the feasibility study of the off-detector electronics will continue to be involved in the detailed design, prototyping and system test phases of the project. They will also be responsible for the procurement and testing of the system. This team includes Saclay, LLR, Lisbon, and CERN. Saclay will take responsibility for the SRP board, LLR for the TCC board, Lisbon for the DCC board, and CERN for the CCS system.
7. **Electronics Integration and System Commissioning**

7.1 **Introduction**

The feasibility study concluded that the electronics integration system proposed by the review would meet the required performance.

This project is responsible for mounting the front-end electronics on to the 'Super Modules' (SM) and the 'Endcap Dees' (Dee) and ensuring that the electronics is integrated with the cooling system, the data link system, and the low voltage power system. It is also responsible for ensuring that all the electronics is functioning to the required specification before a SM or a Dee is closed ready for calibration or tests in CERN-H4 beam area and subsequent installation into the detector.

The schedule constraints are such that it is essential that the electronics for all the SMs are produced in 2004 and for all the Dees in 2005. This implies that the required integration process must be able to install all of the embedded electronics systems and the cooling system into a SM in ~ 1 week. This in turn implies that the systems for an individual module should be installed in ~ 1 day. The design of the system must also meet these constraints.

7.2 **Status of the Electronics Integration and System Commissioning**

To reduce the physical constraints on the position of the VFE cards and to reduce the heat transfer from the cards into the crystal enclosure below the electronics, it was decided to couple the VFE board to the input socket with a flexible ribbon cable. It was also decided to mount the cards from two rows of input sockets onto a common cooling bar. A module has 10 cooling bars, and design options under consideration are to mount these bars individually or as one system for a complete module. One of these designs, based on the excellent thermal stability obtained with the M0’ prototype in H4 beam tests this Summer, is shown in figure 8.

The detailed design of the mounting of the VFE boards and the cooling, data link and LV systems is well advanced. In parallel with the preparation of detailed mechanical drawings for the fabrication of the final system, prototype test will be performed with dummy electronics that dissipate the same power as the real system, to ensure that everything fits together and that the cooling calculations are correct. In Q4 2002, a system with final electronics will be prepared, which will be the basis for the final system to be used in the tests in April 2003. The detailed specification of the system integration has been completed.
Figure 8. **A layout of the VFE boards mounted in a module**

### 7.3 Project Plan

The project plan presented to the review continues to be realistic. The detailed plan is shown in figure 4. The major milestones for this sub-project are:

- **Preliminary Cooling and Integration Review**: Nov 2002
- **EDR (EB Cooling and Integration)**: Jun 2003
- **Complete Preliminary Evaluation of dressed SM0**: Nov 2003
- **Progress Review of Integration of EB electronics**: Mar 2004

### 7.4 Staffing Plan

The team involved in the feasibility study of the electronics integration will continue to be involved in the detailed design, prototyping and system test phases of the project. An Electronics Integration Centre will be established at CERN by ETHZ, where all of the electronics from the regional test centers, previously tested, will be collected before mounting onto the SMs and Dees. This Integration Centre will require additional technician support, which will be provided by other institutes and any missing manpower.
will be hired. The estimated cost of this hired manpower is included in the latest Cost Estimate.

8. The Power System, Slow Control System and the Pre-shower Integration Project and the extension of the barrel systems into the End Cap.

8.1 Introduction

A good start has been made to all of these projects.

The power system required a decision from CMS on the proposal to develop a common LV system for the whole experiment based on power transmission to the experiment at 400 Hz and 400 V. Now that this decision has been made the design of the system that transmits power from the edge of the magnet to the SMs or Dees can continue. The baseline system under consideration uses local low voltage regulators. We are also following alternative developments done for the CMS Tracker using power supplies located at the edge of the magnet. The key milestone is that it has to be installed and commissioned by Oct 2005 and additional milestones will be defined in the coming year.

A draft of the specifications of the detector control system is under review. This system must be commissioned by October 2005. A new group from IHEP-Protvino has recently joined this project.

The integration of the preshower electronics system into the ECAL system required a more complete specification of the off-detector system, which now exists. The data link system and the control system used by the preshower will be the same as ECAL and there is now scope for further rationalization.

Although the end cap electronics system is part of the ECAL electronics system, it has a number of different constraints and will be delivered after the electronics for the barrel. The project plan (Fig. 4), shows tests of an E0’ module (4 Super Crystals), with barrel electronics in 2003 and with end-cap electronics in 2004. The motivation for these plans is to ensure that all system issues for the end-cap system have been resolved before production starts in 2005. The milestones for this part of the project are:

- E0’ pre-production mechatronics ready: Jul 2003
- E0’ beam-tested with EB FPPA’s: Sep 2003

9. Cost

The cost of the ECAL electronics system is being re-evaluated. The re-costing will be completed by the end of September 2002 and will be presented during the 2002 CMS Comprehensive Review. The costs for the Installation also have recently been updated. However an overall constraint is the capped total cost of the ECAL.
10. Conclusion

The Feasibility Study phase of the ECAL electronics systems has been successfully completed for the four major projects, and has been successfully started for the remaining three projects. The specifications of the ECAL electronics systems have been completed and detailed design has started. The project plan, the staffing plan and spend profiles have been completed. The ECAL electronics design and development is on schedule. There remains much work to be done, but there is every reason to believe that the system will be ready for an Electronics Systems Review in 3Q 2003 in preparation for the start of production of the electronics in Q4 2003.

GLOSSARY

APD    Avalanche Photodiode
CCS    Clock and Control System
DCC    Data Concentrator Card
ESR    Electronic Systems Review
FE     Front-End
FEC    Front-End Controller
FPGA   Field Programmable Gate Array
GOL    Gigabit Optical Link
HVPS   High Voltage Power System
LVPS   Low Voltage Power System
RCS    
SRP    Selective Readout Processor
TCC    Trigger Concentrator Card
TPG    Trigger Primitive Generation
TTC    Timing and Trigger Control
TTS    
ULR    Upper Level Readout (now Off-Detector Electronics)
VFE    Very Front-End
VPT    Vacuum PhotoTriode