A general purpose reflective memory board for accelerator data acquisition and control system applications

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Abstract

The demonstrator of a reflective memory board for accelerator data acquisition and control system applications is presented. The main building blocks of the reflective memory board are: a 32 bit x 66 MHz Master/Target PCI interface with DMA capabilities, a fiber optic full-duplex high-speed link and a 1 MByte Synchronous Static DPRAM. The reflective memory mechanism is implemented in a fully transparent way in both directions. A message passing and remote interrupt generation procedure from one PC to the other is implemented too.

I. OVERVIEW

The reflective memory board is designed to connect the accelerator control system hardware level to a concentrator PC to realize an accelerator state database. This parallel system is necessary to create a database without dropping supervisor level performance. The board connects DAQ PCs and concentrator through high speed optical fiber channel and interfaces PC motherboard through PCI bus 32 bit x 66 MHz. The board control system is implemented on FPGA device to realize a flexible and upgradable system [1].

II. BOARD ARCHITECTURE

The hardware is a PCI card with an Altera Acex device as board controller, a Texas Instruments serializer-deserializer device, an Agilent full-duplex optical transceiver and a 1 MB (256K x 32) Cypress DPRAM.

The controller implemented on FPGA is composed of three major functional blocks (see fig.2): SerDes interface controls data transmission (TX) and reception (RX), DPRAM interface controls data to and from memory and manages data packet protocols, the PCI interface is a PCI core IP that manages board – bus communication.

Three clock domains are present on the board: 66 MHz clock for PCI to card communications, 80 MHz quartz generated clock for data transmission and the recovered clock from data received. In present configuration the board acts as a master PCI device with DMA capabilities. A reflective memory system is implemented, it allows to create on a remote board DPRAM (receiver) an “image” of a local PC block memory (transmitter). An interrupt signal is generated on remote PC when a preselected DPRAM block is written.

A. Transmission

Data transmission is a DMA read transaction. A block of memory is read in burst mode and data goes to SerDes interface input (32 bit x 66 MHz). Inside this block, dual clock FIFOs based, data packet is assembled and transmission control signal are created. The output is a 16 bit x 80 MHz data stream. Serializer device provides serial data stream to send to transceiver.
B. Reception

In this case the transaction between bus and board is a DMA write transaction where data packet from fiber is written on host main memory. The data packet is 16-bit wide. Packet level protocol defines packet as two word header: start address and word number. These informations define a block where to write on remote DPRAM. A parity check system is implemented too (fig 3).

Figure 3: Data packet

III. PCB

The printed circuits board is designed to minimize cross-talk between signal lines and to ensure minimal signal reflection.

The board stack-up is 12 layers thick: 5 signal layers are present. Top and bottom layer are impedance controlled and designed to route high speed signals. Internal signal planes are near a GND or PWR reference plane.

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<thead>
<tr>
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<th>Dielectric Constant</th>
<th>Thickness</th>
<th>Material</th>
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<td>16.12</td>
<td>Copper 40</td>
<td>signal (contrast)</td>
</tr>
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<td>100</td>
<td>Copper 18</td>
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<td>signal (contrast)</td>
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</tbody>
</table>

Figure 4: PCB stackup

IV. Simulation and Implementation Data

In this section we report some simulation obtained from Mentor Graphics ModelSim 5.7 and some implementation data obtained from Altera Quartus II implementation software.

The control logic inside FPGA is designed to have maximum speed and timing performance. Fit on Acex device give:

- max PCI clk 80 MHz (requested 66 MHz)
- max TX clk 120 MHz (requested 80 MHz)
- max RX clk 105 MHz (requested 80 MHz)

timing data as tco and tsu are in request range. The computed band with 80 MHz quartz clock is 1.28 Gbps (peak).

Figure 6: Data transmission diagram with ModelSim 5.7: data to serializer

Transmission lines simulations performed by SpectraQuest tool showed good electrical performance of clock and high speed signal inside PCB.
The previous figure (Fig.9) shows the eye-diagram from SpectraQuest simulator, for high-speed signal from SerDes to optical transceiver.

V. CONCLUSION AND FUTURE DIRECTIONS

The card is completed and the windows software driver is in fast progress, we are running preliminary test. The card is highly flexible and upgradable: different network architectures are possible and different capabilities and features can be implemented, if required, on FPGA control device. The next step in this project is to realize an accumulator board. It will include four independent full-duplex optical fiber channels and will be necessary in prevision of DAQ PCs increasing number.

VI. REFERENCES

[1] Maurizio Sabene
Sviluppo di una scheda di comunicazione con interfaccia in fibra ottica per il sistema di controllo dell’acceleratore SPARC
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